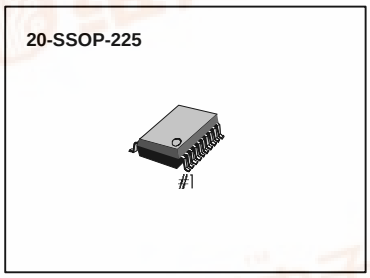
KS7221D VERTICAL DRIVER FOR CCD

GENERAL DESCRIPTION

The KS7221D is a Vertical CCD Driver LSI which is fabricated by CMOS process for high voltage



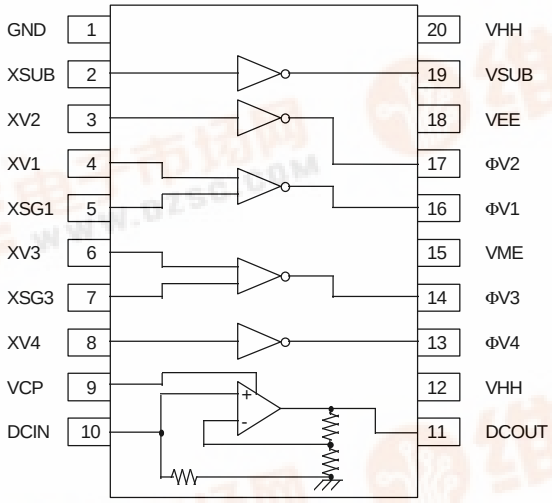
FEATURES

· Include voltage source circuit for CCD image sensor.
· Input voltage : 5V / 3.3V
· Package : 20 SSOP

ORDERING INFORMATION

Device	Package	Operating Temperature
KS7221D	20-SSOP-225	-20°C ~ + 85°C

BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN DESCRIPTION

Pin	Symbol	I/O	Description	Remark
1	GND	-	Ground control	
2	Xsub	I	Output Control (Vsub)	
3	XV2	I	Output Control (ΦV2)	
4	XV1	I	Output Control (ΦV1)	
5	XSG1	I	Output Control (ΦV1)	
6	XV3	I	Output Control (ΦV3)	
7	XSG3	I	Output Control (ΦV3)	
8	XV4	I	Output Control (ΦV4)	
9	VCP	I	Power of amp	
10	DCIN	I	OP-Amp input (internal pull-down resistor)	
11	DCOUT	O	OP-Amp output	
12	VHH	-	Power (15V)	
13	ΦV4	O	High Voltage Output (2 level :VME, VEE)	
14	ΦV3	O	High Voltage Output (3 level : VME, VEE, VHH)	
15	VME	-	Power (0V)	
16	ΦV1	O	High Voltage Output (3 level : VME, VEE, VHH)	
17	ΦV2	O	High Voltage Output (2 level : VME, VEE)	
18	VEE	-	Power (-8.5V)	
19	Vsub	O	High Voltage Output (2 level : VEE, VHH)	
20	VHH	-	Power (15V)	

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	VEE	0 ~ -10	V
	VHH	-0.3 ~ VEE +35	
	VME	VEE -0.3 ~ 3.0	
Input Voltage	VI	-0.3 ~ VHH +0.3	
	VCP	-0.3 ~ VEE+35	
Output Voltage	ΦV1, ΦV2, ΦV3, ΦV4, ΦVsub	VEE -0.3 ~ VHH +0.3	
OP-Amp output Current	I_{OUT}	±5	mA
Operating Temperature	T_{OPR}	-25 ~ +85	°C
Storage Temperature	T_{STG}	-45 ~ +120	

LOGIC FUNCTION TABLE

INPUT				OUTPUT		
XV1,3	XSG1,3	XV2,4	XSUB	ΦV1, 3	ΦV2, 4	VSUB
L	L	-	-	VHH	-	-
H	L	-	-	Z	-	-
L	H	-	-	VME	-	-
H	H	-	-	VEE	-	-
-	-	L	-	-	VME	-
-	-	H	-	-	VEE	-
-	-	-	L	-	-	VHH
-	-	-	H	-	-	VEE

AC CHARACTERISTICS

(VHH = 15V, VME = GND, VEE = - 8.5V ; Ta = 25°C)

Description	Symbol	Test Condition	Min	Typ	Max	Unit
DELAY TIME	TPLM	NO LOAD (*1)	10	40	70	ns
	TPMH	NO LOAD (*1)	10	30	70	
	TPLH	NO LOAD (*1)	10	40	100	
	TPML	NO LOAD (*1)	10	100	200	
	TPHM	NO LOAD (*1)	10	100	180	
	TPHL	NO LOAD (*1)	10	60	100	
RISING TIME	TTLM	VEE → VME (*1)	400	700	930	
	TTMH	VME → VHH (*1)	400	650	930	
	TTLH	VEE → VHH (*1)	10	50	100	
	TTML	VME → VEE (*1)	200	300	500	
	TTHM	VHH → VME (*1)	400	600	820	
	TTHL	VHH → VME (*1)	10	50	100	
OUTPUT NOISE VOLTAGE	VCLH, VCLL VCMH, VCML	(*2)	-	-	0.5	V

(*1) REFER TIMING DIAGRAM
(*2) REFER NOISE DIAGRAM

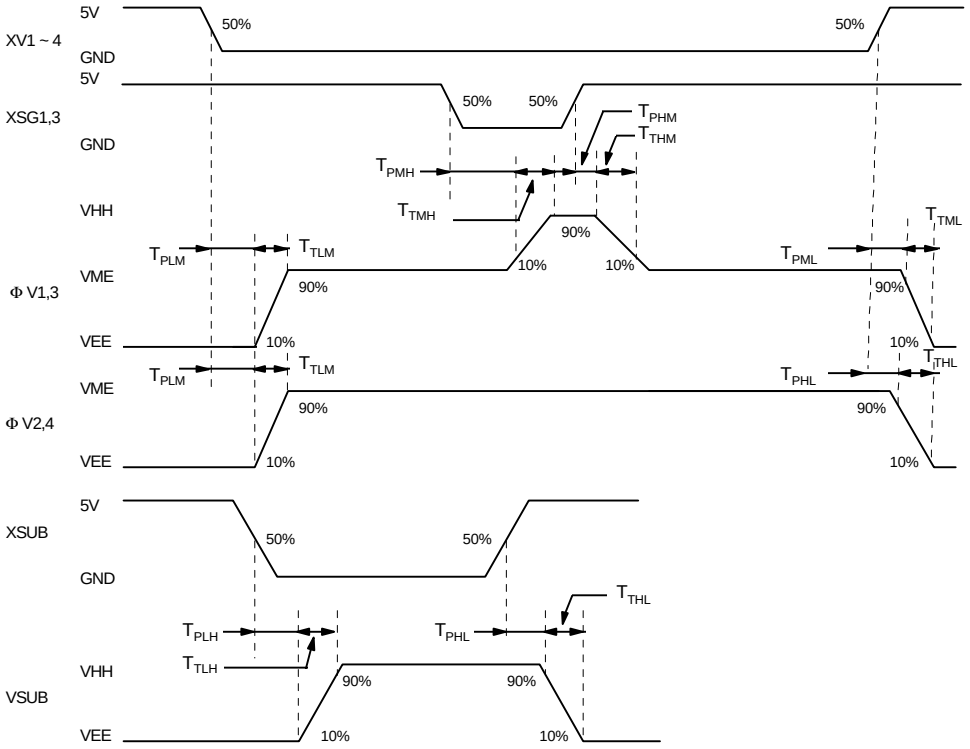
DC CHARACTERISTICS

(VHH = 15V, VME = GND, VEE = -8.5, VCP = 22V ; Ta = 25°C)

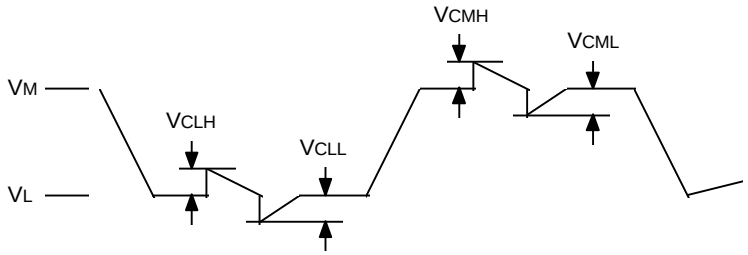
Description	Symbol	Test Conditon	Min	Typ	Max	Unit
Supply Voltage	VHH		14.5	15	15.5	V
	VEE		-9.5	-8.5	-7.5	
Input Voltage	VCP	When VCP is used	VHH	22	23.5	
High level input voltage	VIH	(*3)	2.3	-	-	
Low level input voltage	VIL	(*3)	-	-	1.2	
Input Current	II	VIN = 0~5V (*3)	-1.0	0.0	1.0	μA
	IDCIN	VDCIN = 1.0V	80	100	140	
Operation Current	IHH	(*1)	-	2.0	3.5	mA
	IME	(*1)	-	4.5	5.0	
	IEE	(*1)	-8.5	-6.5	-	
Output Current	IOL	ΦV1~4 = -8.0V	25	37	-	
	IOM1	ΦV1~4 = -0.5V	-	-15	-10	
	IOM2	ΦV1.3 = 0.5V	9	13.5	-	
	IOH	ΦV1.3 = 14.5V	-	-18	-12	
	IOSL	VSUB = -8.0V	12	18	-	
	IOSH	VSUB = 14.5V	-	-10.5	-7	
Op-Amp Gain	G	IOUT = -200μA	x 4.0	x 4.2	x 4.7	
Gain Variation	ΔG	Ta=-20 ~ 75°C (*2), Iout=-200μAVDCIN = 1.0 ~ 4.5V	-3	-	+3	%
Operation Current	IVCP	VDCIN = 1.0 ~ 4.5V IOUT = 0μA	0.08	-	1.0	mA

(* 1) : Refer the test circect. Shutter speed : 1/100000 SEC
(* 2) : Refer the characteristics of OP - AMP
(* 3) : XV1 ~ 4, XSG1, XSG3, XSUB PIN

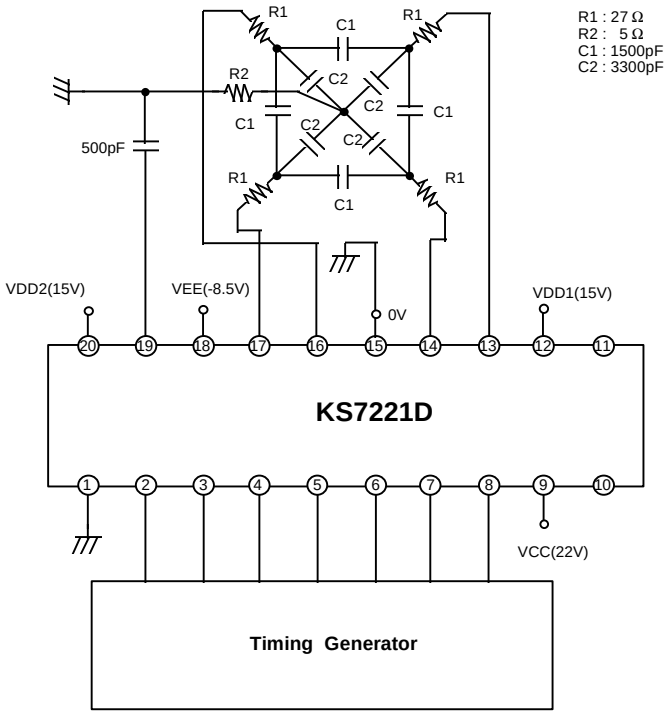
TIMING DIAGRAM



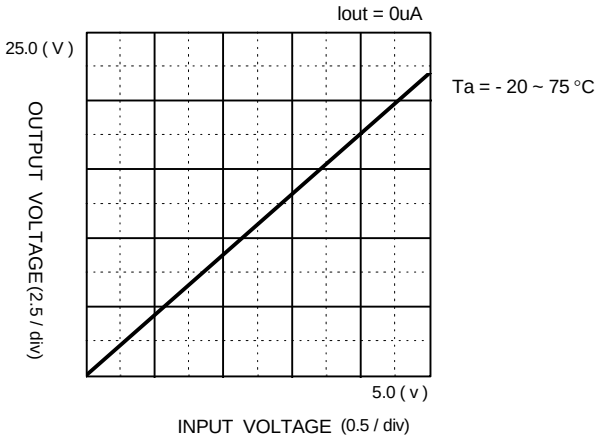
NOISE DIAGRAM



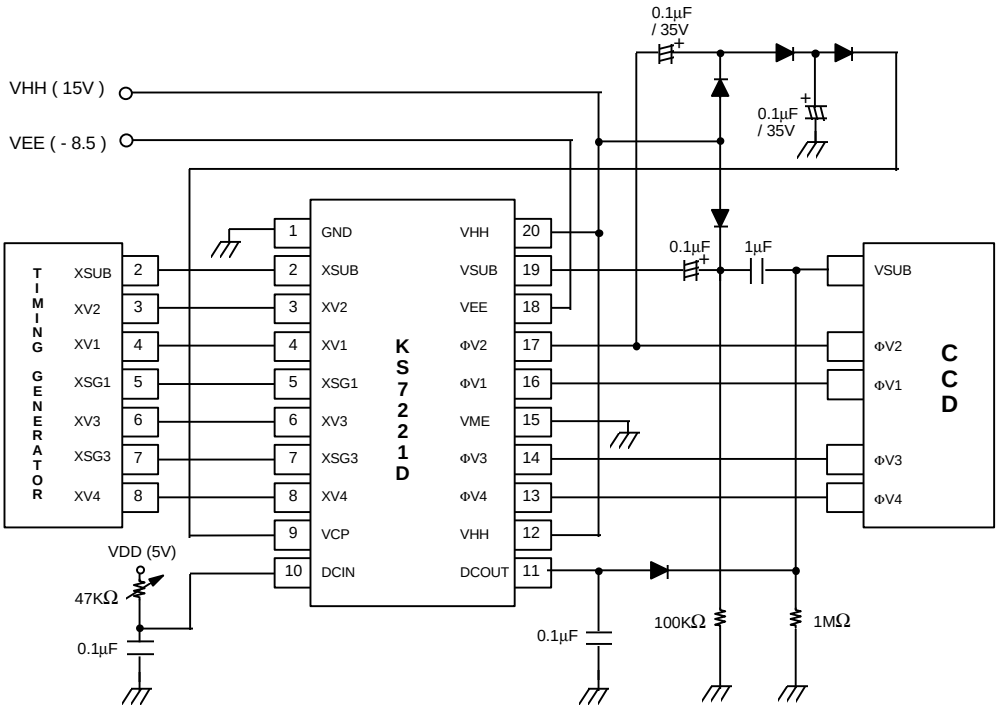
TEST CIRCUIT



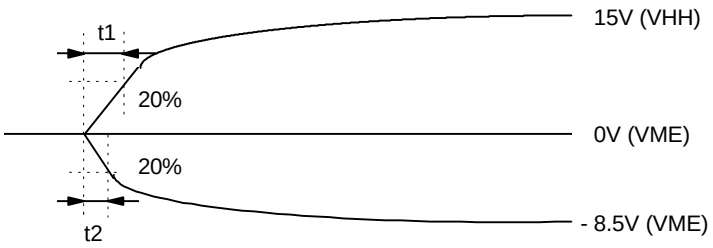
OP- AMP Gain Characteristics



APPLICATION CIRCUIT



* In case of DCOUT ≤ VHH - 1.0V , V_{CP} PIN connects with VHH.
Warning : When voltage is biased, You must keep this flow.
if you don`t this flow, Negative voltage is applied to CCD image sensor`s SUB.



* t1 ≥ t2 ≥ 10ms

PACKAGE DIMENSION

20-SSOP-225

unit : mm