

PHOTO-INTERRUPTER

KTIR0311S

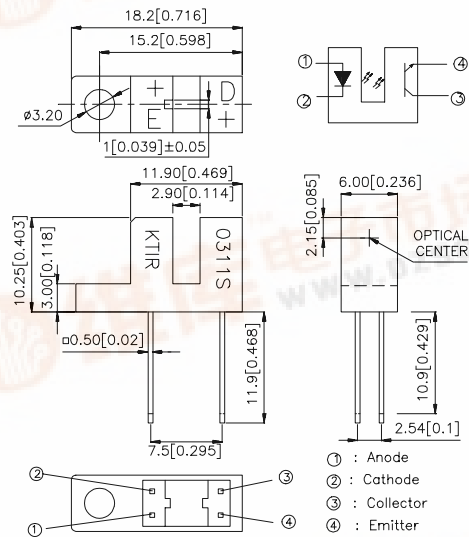
Features

- Ultra-small
- Minimal influence from stray light
- Low collector-emitter saturation voltage

Applications

- Optical control equipment.
- Cameras.
- Floppy disk drives.

Package Dimensions

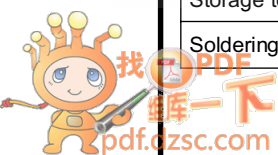


Notes:

1. All dimensions are in millimeters (inches).
2. Tolerance is ± 0.15 (0.006") unless otherwise noted.
3. Lead spacing is measured where the lead emerge package.
4. Specifications are subject to change without notice.

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	Reverse voltage	V_R	5	V
	Power dissipation	P	75	mW
Output	Collector-emitter voltage	V_{CEO}	30	V
	Emitter-collector voltage	V_{ECO}	5	V
	Collector current	I_C	20	mA
	Collector power dissipation	P_C	75	mW
Operating temperature		T_{opr}	-25~+85	$^\circ\text{C}$
Storage temperature		T_{stg}	-40~+100	$^\circ\text{C}$
Soldering temperature (1/16 inch from body for 5 seconds)		T_{sol}	260	$^\circ\text{C}$



Electro-optical Characteristics (T_a=25°C)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input	Forward voltage	V _F	I _F =20mA	—	1.2	1.5	V
	Reverse current	I _R	V _R =5V	—	—	10	μA
Output	Collector dark current	I _{CEO}	V _{CE} =20V	—	—	100	nA
Transfer characteristics	Collector-emitter saturation voltage	V _{CE(sat)}	I _C =1mA I _F =40mA I _F =40mA	—	—	0.4	V
	Current transfer ratio	CTR	V _{CE} =5V I _F =20mA	—	38	—	%
	Response time	Rise time	t _r	V _{CE} =2V I _C =2mA R _L =100Ω	—	5	25
Fall time		t _f	—		4	20	μsec

Fig.1 Forward Current vs. Forward Voltage

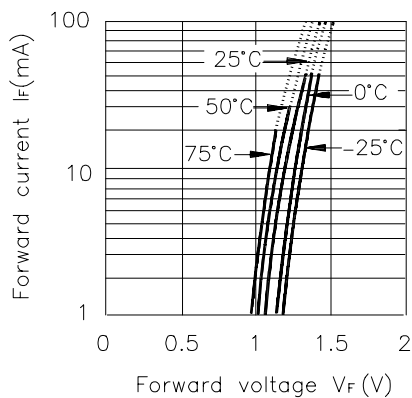


Fig.2 Collector Current vs. Forward Current

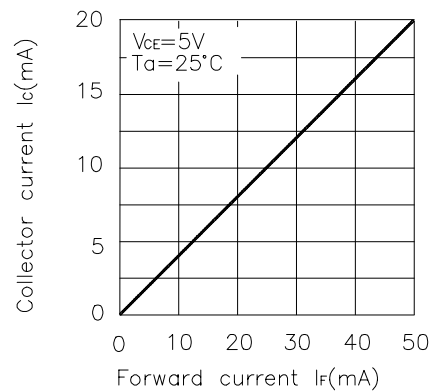


Fig.3 Collector Current vs. Collector-emitter Voltage

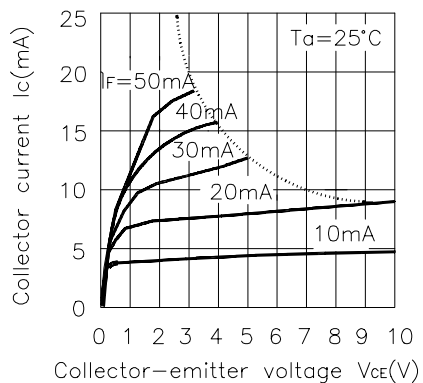


Fig.4 Collector Current vs. Ambient Temperature

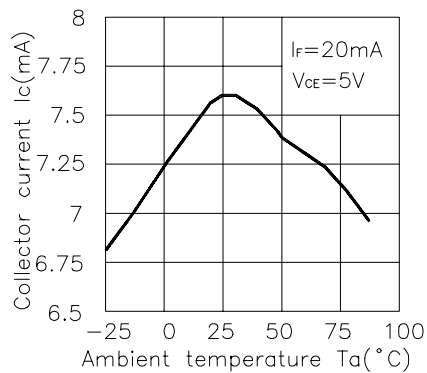


Fig.5 Collector-emitter Saturation Voltage vs. Ambient Temperature

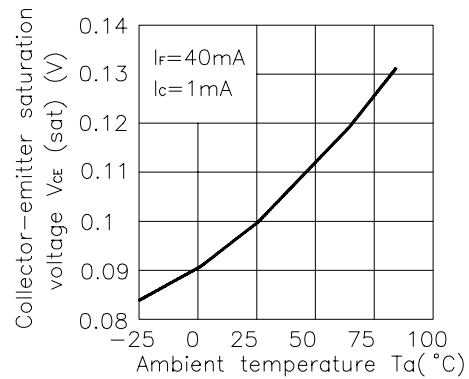


Fig.6 Relative Collector Current vs. Shield Distance(1)

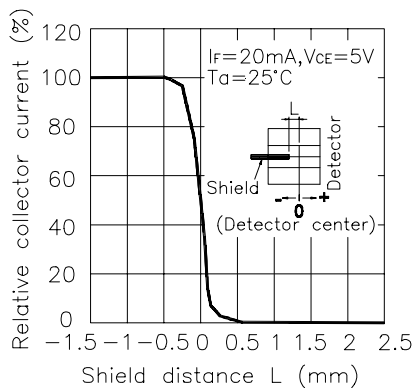


Fig.7 Relative Collector Current vs. Shield Distance(2)

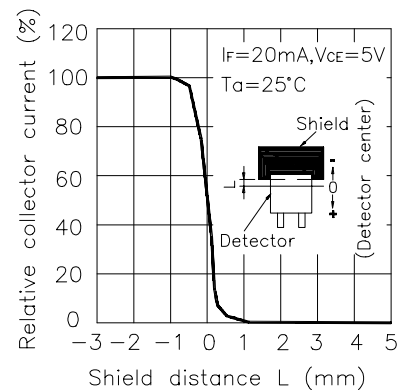
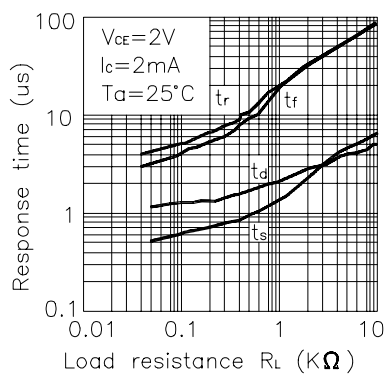


Fig.8 Response Time vs. Load Resistance



Test Circuit for Response Time

