查询BU7878KVT供应商



## ●Product outline

| | |
|---|---|
| ■Type | BU7878KVT |
| ■Function | 90MHZ 30BITS COLOR LVDS TRASMITTER |
| ■Package | TQFP64V |
| ■Supply voltage | 3.3V±0.3V |
| ■Temperature range | −20℃～85℃ |

## ●General Description

The BU7878KVT is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to WXGA resolutions.

The BU7878KVT converts 35bits of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed to use either rising edge or falling edge of pixel clock by a dedicated pin. By using 90MHz transmit clock rate, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE, CNTL1, CNTL2) are transmitted up to 630Mbps effective rate per LVDS channel.

## ●Feature

- ■Wide dot clock range: form 8MHz up to 85MHz for NTSC, VGA, SVGA, XGA, WXGA applications.
- ■Support spread spectrum clock generator.
- ■Clock edge selectable.
- ■Support reduced swing LVDS for low EMI.
- ■Power down mode.
- ■Low power signal 3.3V CMOS design.
- ■64pin TQFP package.
- ■30bit LVDS receiver is recommended to use BU7879KVT.

●Precaution

- ■This chip is not designed to protect from radioactivity.
- ■The chip is made strictly for the specific application or equipment.
  Then it is necessary that the unit is measured as needed.
- ■This document may be used as strategic technical data
  which subjects to COCOM regulations.

## ●Block Diagram

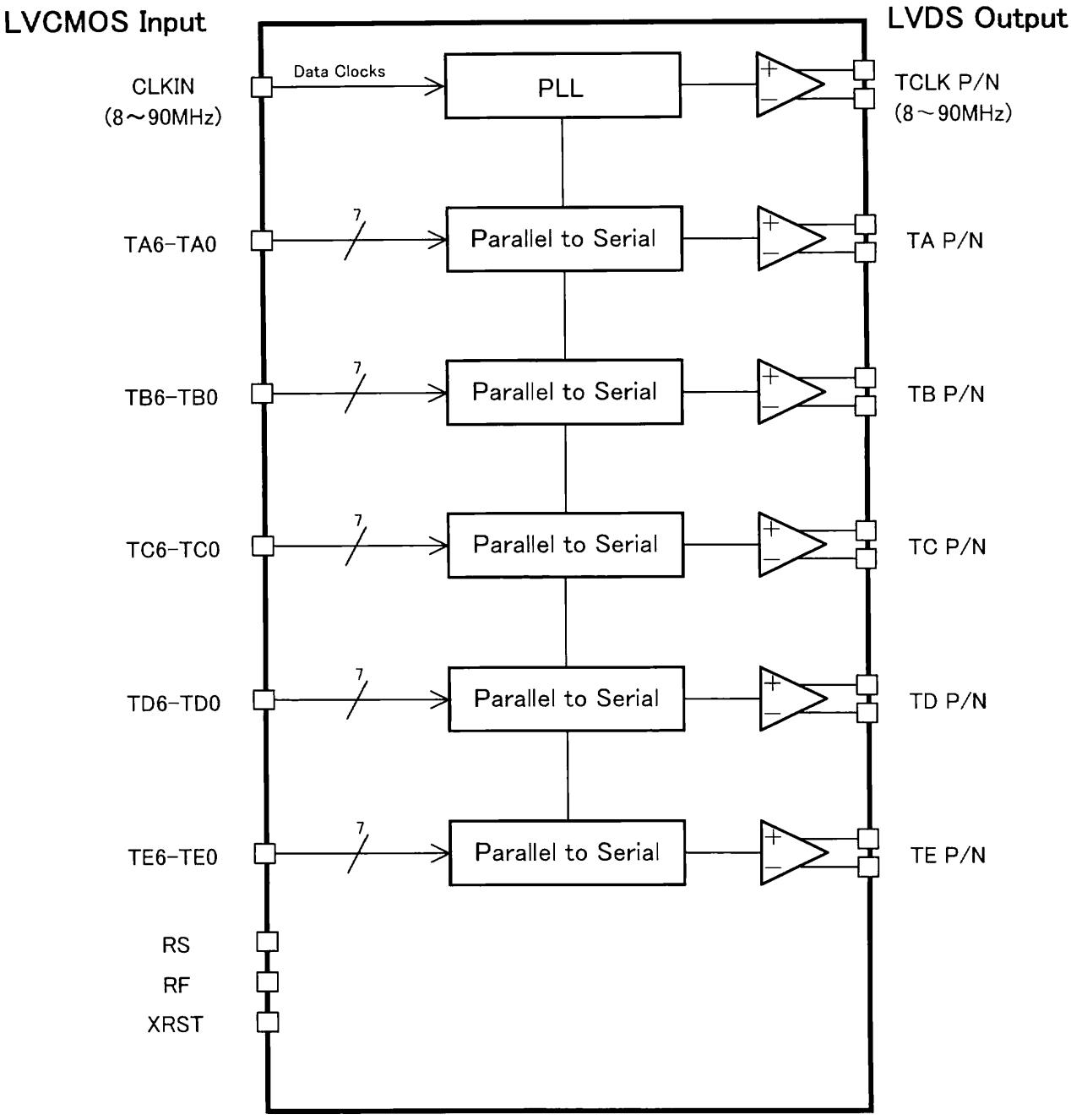



Figure-1 Block Diagram

## ●About the Power On Reset

**Power On Reset is not mandatory for this device.**
**(The PD pin should be set to high level when Power On Reset procedure is not used.)**

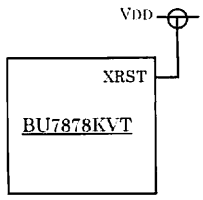



Figure-10 Terminal connection when Power On Reset is not used.

However, Power On Reset procedure is strongly recommend for internal logic initialization by following two methods.

① The method of using CR circuit.
② The method of using external specific IC.

It is recommend to do enough examination for target application.

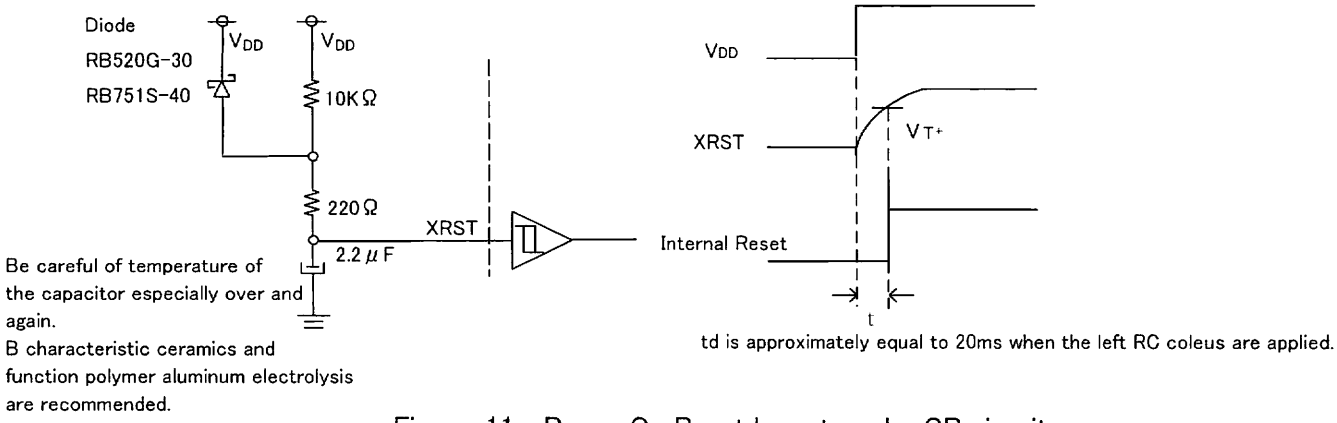



Figure-11 Power On Reset by external a CR circuit

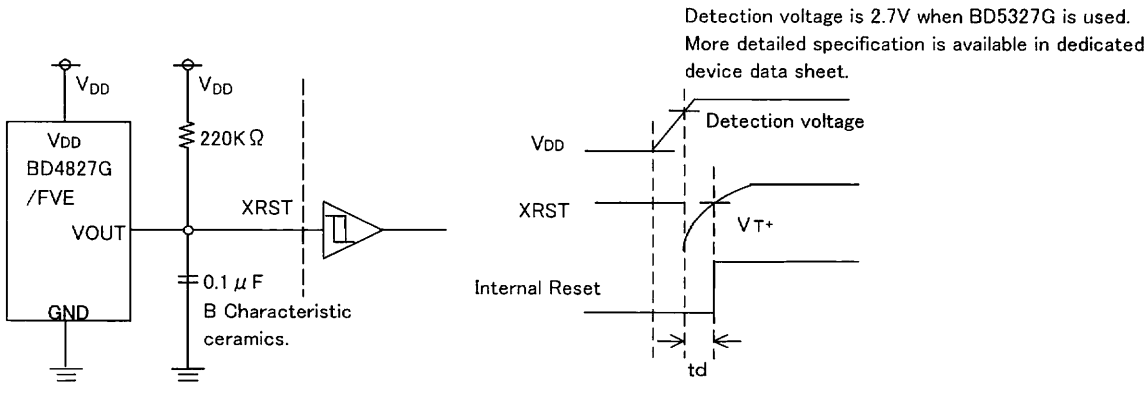
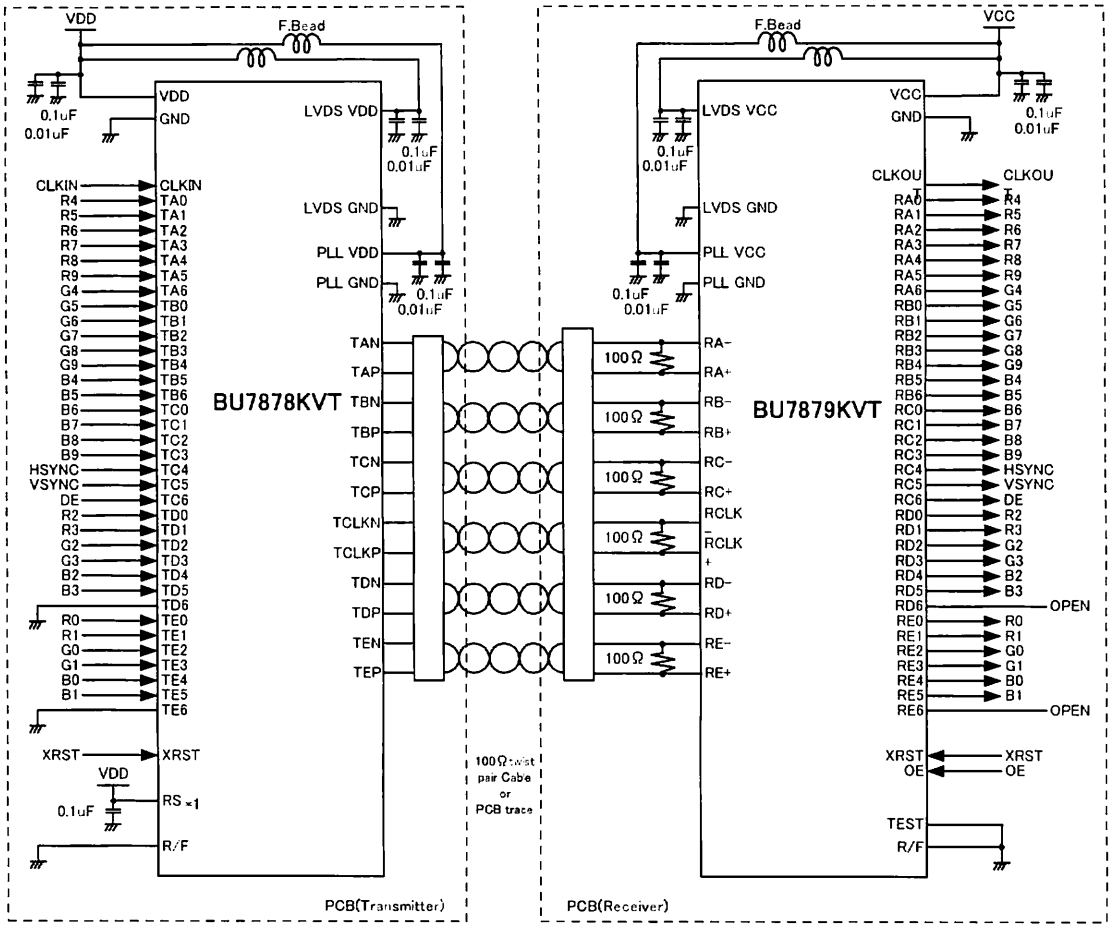



Figure-12 Power On Reset by specific IC

## ●10bit LVCMOS Level Input

Example:
BU7878KVT : LVCMOS level input/Falling edge/Normal swing
BU7879KVT : Falling edge




*1 : If RS pin is tied to VDD,LVDS swing is 350m V.
If RS pin is tied to GND,LVDS swing is 200m V.

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