M29KW032E

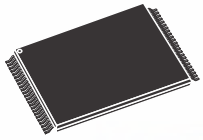
32 Mbit (2Mb x16, Uniform Block) 3V Supply LightFlash™ Memory

PRODUCT PREVIEW

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Read
  - V_{PP} = 11.4V to 12.6V for Program and Erase
- ACCESS TIME: 90, 110ns
- PROGRAMMING TIME
  - 9µs per Word typical
  - Multiple Word Programming Option (4s typical Chip Program)
- ERASE TIME
  - 21s typical factory Chip Erase
- UNIFORM BLOCKS
  - 16 blocks of 2 Mbits
- PROGRAM/ERASE CONTROLLER
  - Embedded Word Program algorithms
- 10,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code : 88ACh

Figure 1. Packages



TSOP48 (N)
12 x 20mm

TFBGA48 (ZA)
6 x 9mm

This is preliminary information on a new product now in development. Details are subject to change without notice.

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SUMMARY DESCRIPTION

The M29KW032E LightFlash™ is a 32 Mbit (2Mb x16) non-volatile memory that can be read, erased and reprogrammed. Read operations can be performed using a single low voltage (2.7 to 3.6V) supply. Program and Erase operations require an additional V_{PP} (11.4 to 12.6) power supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into 16 uniform blocks that can be erased independently so it is possible to preserve valid data while old data is erased (see Figures 2, Block Addresses). Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller (P/E.C.) simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The M29KW032E LightFlash™ features a new command, Multiple Word Program, used to program large streams of data. It greatly reduces the total programming time when a large number of Words are written to the memory at any one time. Using this command the entire memory can be programmed in 2s, compared to 9s using the standard Word Program.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP48 (12 x 20mm) and TFBGA48 (6 x 9mm, 0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

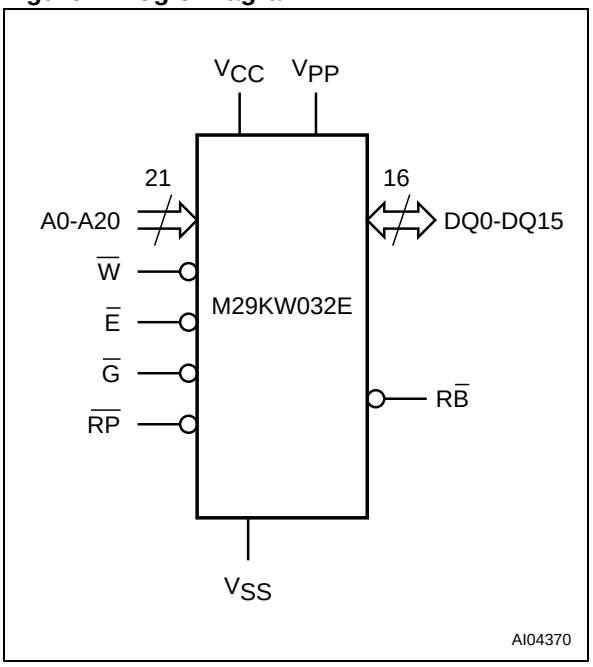


Table 1. Signal Names

A0-A20	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset
$R\overline{B}$	Ready/Busy Output
V_{CC}	Supply Voltage read
V_{PP}	Supply Voltage program erase
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TFBGA Connections (Top view through package)

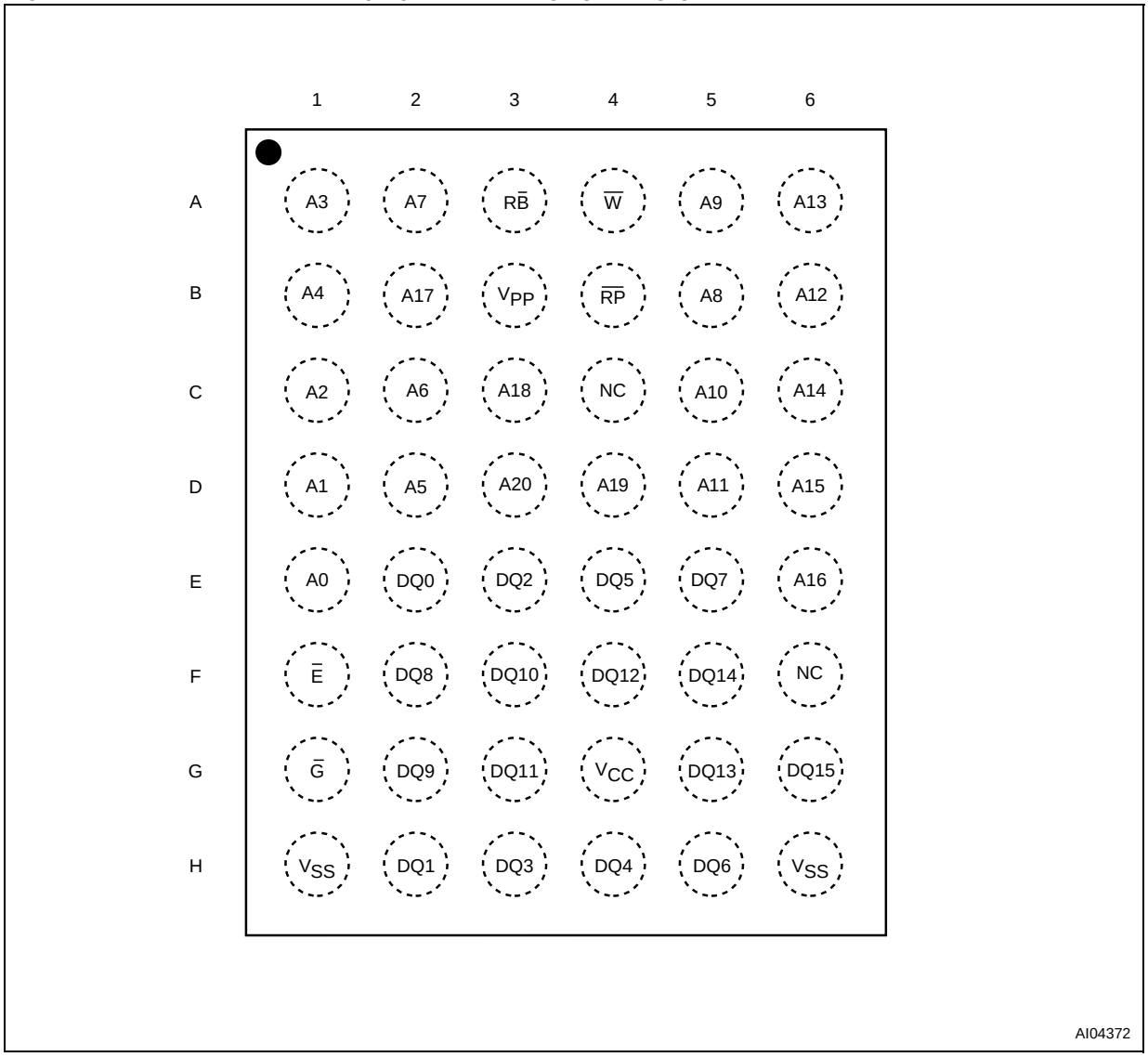


Figure 4. TSOP Connections

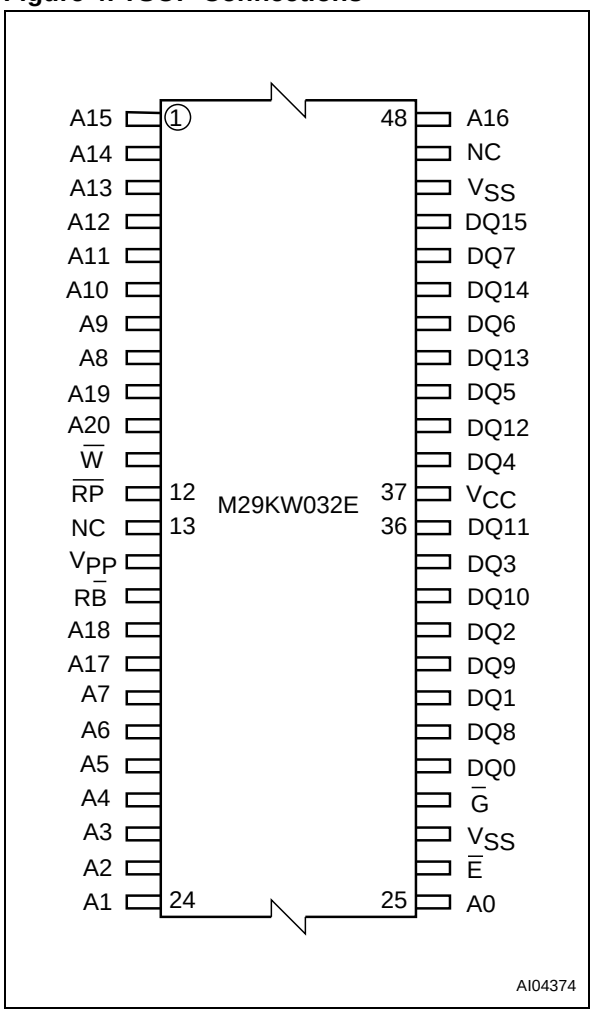


Table 2. Block Addresses

Block Number	Address Range
16	1E0000h-1FFFFFh
15	1C0000h-1DFFFFh
14	1A0000h-1BFFFFh
13	180000h-19FFFFh
12	160000h-17FFFFh
11	140000h-15FFFFh
10	120000h-13FFFFh
9	100000h-11FFFFh
8	0E0000h-0FFFFFh
7	0C0000h-0DFFFFh
6	0A0000h-0BFFFFh
5	080000h-09FFFFh
4	060000h-07FFFFh
3	040000h-05FFFFh
2	020000h-03FFFFh
1	000000h-01FFFFh

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A20). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

Data Inputs/Outputs (DQ0-DQ7). The Data Inputs/Outputs outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the Program/Erase Controller.

Data Inputs/Outputs (DQ8-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

Reset ($\overline{RP}$). The Reset pin can be used to apply a Hardware Reset to the memory.

A Hardware Reset is achieved by holding Reset Low, V_{IL}, for at least t_{PLPX}. After Reset goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See the Ready/Busy Output section, Table 16 and Figure 13, Reset AC Characteristics for more details.

Ready/Busy Output ($R\overline{B}$). The Ready/Busy pin is an open-drain output that can be used to identify when the memory array can be read. Ready/Busy is high-impedance during Read mode and Auto Select mode. After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See Table 16 and Figure 13, Reset AC Characteristics.

During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy will remain Low during Read/Reset commands or Hardware Resets until the memory is ready to enter Read mode.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for Read operations.

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC3}.

V_{PP} Program Supply Voltage. V_{PP} is both a power supply and Write Protect pin. The two functions are selected by the voltage range applied to the pin. The Supply Voltage V_{CC} must be applied before the Program Supply Voltage V_{PP}.

If V_{PP} is in the range 11.4V to 12.6V it acts as a power supply pin for program and erase operations. V_{PP} must be stable until the Program/Erase algorithm is completed.

If V_{PP} is kept in a low voltage range (0V to 3.6V) V_{PP} is seen as a Write Protect pin. In this case a voltage lower than V_{HH} gives an absolute protection against program or erase, while V_{PP} in the range of V_{HH} enables these functions (see Table 12, DC Characteristics for the relevant values).

Note that V_{PP} must not be left floating or unconnected as the device may become unreliable.

Vss Ground. The V_{SS} Ground is the reference for all voltage measurements.

BUS OPERATIONS

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby, Automatic Standby and Electronic Signature. See Tables 3, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 10, Read Mode AC Waveforms, and Table 13, Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 11 and 12, Write AC Waveforms, and Tables 14 and 15, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 12, DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3}, for Program or Erase operations until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Tables 3, Bus Operations.

Table 3. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{PP}	Address Inputs A0-A20	Data Inputs/Outputs DQ15-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	XX(4)	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{HH}(3)	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	X	Hi-Z
Standby	V_{IH}	X	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	XX	A0 = V_{IL}, A1 = V_{IL}, Others V_{IL} or V_{IH}	0020h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	XX	A0 = V_{IH}, A1 = V_{IL}, Others V_{IL} or V_{IH}	88ACh

Note: 1. X = V_{IL} or V_{IH}.
2. XX = V_{IL} , V_{IH} or V_{HH}
3. Not necessary for Auto Select or Read/Reset commands.
4. When reading the Status Register during Program or Erase operations, V_{PP} must be kept at V_{HH}.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

Refer to Tables 4 and 5, for a summary of the commands.

Read/Reset Command.

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset Command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. Once the program or erase operation has started the Read/Reset command is no longer accepted. The Read/Reset command is executed regardless of the value of V_{PP} (V_{IL}, V_{IH} or V_{HH}).

Auto Select Command.

The Auto Select command is used to read the Manufacturer Code and the Device Code. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until a Read/Reset command is issued, all other commands are ignored. The Auto Select command is executed regardless of the value of V_{PP} (V_{IL}, V_{IH} or V_{HH}).

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

Word Program Command.

The Word Program command can be used to program a Word to the memory array. V_{PP} must be set to V_{HH} during Word Program. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 6. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Multiple Word Program Command

The Multiple Word Program command can be used to program large streams of data. It greatly reduces the total programming time when a large number of Words are written to the memory at any one time. V_{PP} must be set to V_{HH} during Multiple Word Program. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode.

It has four phases: the Setup Phase to initiate the command, the Program Phase to program the data to the memory, the Verify Phase to check that the data has been correctly programmed and reprogram if necessary and the Exit Phase.

Setup Phase. The Multiple Word Program command requires three Bus Write operations to initiate the command (refer to Table 5, Multiple Word Program Command and Figure 5, Multiple Word Program Flowchart). The Status Register Toggle bit (DQ6) should be checked to verify that the operation has started and the Multiple Word Program bit (DQ0) checked to verify that the P/E.C. is ready for the first Word.

Program Phase. The Program Phase requires n+1 cycles, where n is the number of Words, to execute the programming phase (refer to Table 5, Multiple Word Program Command and Figure 5, Multiple Word Program Flowchart).

Three successive steps are required to issue and execute the Program Phase of the command.

1. The fourth Bus Write operation of the command latches the Start Address and the first Word to be programmed. The Status Register Multiple Word Program bit (DQ0) should be read to check that the P/E.C. is ready for the next Word.
2. Each subsequent Word to be programmed is latched with a new Bus Write operation. The address can remain the Start Address, be incremented or be any address in the same block, as the device automatically increments the address with each sucssesive Bus Write

cycle. If the command is used to program in more than one block then the address must remain in the starting block as any address that is not in the same block as the Start Address terminates the Program operation. The Status Register Multiple Word Program bit (DQ0) must be read between each Bus Write cycle to check that the P/E.C. is ready for the next Word.

3. Finally, after all Words have been programmed, write one Bus Write operation to any address outside the block containing the Start Address, to terminate the programming phase.

The memory is now set to enter the Verify Phase.

Verify Phase. The Verify Phase is similar to the Program Phase in that all Words must be resent to the memory for them to be checked against the programmed data. If the check fails the P/E.C will try to reprogram the correct data. The P/E.C will remain busy until the correct data has been successfully programmed. The Verify Phase is mandatory. If the Verify Phase is not executed the programmed data cannot be guaranteed.

Three successive steps are required to execute the Verify Phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first Word, to be verified. The Status Register Multiple Word Program bit (DQ0) should be read to check that the P/E.C. is ready for the next Word.
2. Each subsequent Word to be verified is latched with a new Bus Write operation. If any address that is not in the same block as the Start Address is given, the Verify operation terminates. The Status Register Multiple Word Program (DQ0) must be read to check that the P/E.C. is ready for the next Word.
3. Finally, after all Words have been verified, write one Bus Write operation to any address outside the block containing the Start Address, to terminate the Verify Phase.

Exit Phase . Read the Status Register to verify that DQ6 has stopped toggling. If the Verify Phase is successfully completed the memory returns to the Read mode. If the P/E.C. fails to reprogram a given location, the Verify Phase will terminate and Error bit DQ5 will be set in the Status Register. If the error is due to a V_{PP} failure DQ4 will also be set. If the operation fails a Read/Reset command must be issued to return the device to Read mode.

It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 6. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

Note that the Multiple Word Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Block Erase Command.

The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost.

V_{PP} must be set to V_{HH} during Block Erase. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode.

Six Bus Write operations are required to select the block . The Block Erase operation starts the Program/Erase Controller after the last Bus Write operation. The Status Register can be read after the sixth Bus Write operation. See the Status Register for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

During the Block Erase operation the memory will ignore all commands. Typical block erase times are given in Table 6. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Chip Erase Command.

The Chip Erase command can be used to erase the entire memory. It sets all of the bits in the memory to '1'. All previous data in the memory is lost.

V_{PP} must be set to V_{HH} during Chip Erase. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 6. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

Table 4. Standard Commands

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	555	90						
Word Program	4	555	AA	2AA	55	555	A0	PA	PD				
Block Erase	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal. The Command Interface only uses A0-A10 and DQ0-DQ7 to verify the commands; A11-A20, DQ8-DQ15 are Don't Care.

Table 5. Multiple Word Program Command

Phase	Length	Bus Write Operations													
		1st		2nd		3rd		4th		5th		Final -1		Final	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Program	3+n +1	555	AA	2AA	55	555	20	PA1	PD1	PA1	PD2	PA1	PAn	NOT PA1	X
Verify	n+1	PA1	PD1	PA1	PD2	PA1	PD3	PA1	PD4	PA1	PD5	PA1	PAn	NOT PA1	X

Note: A Bus Read must be done between each Write cycle where the data is programmed or verified, to Read the Status Register and check that the memory is ready to accept the next data. NOT PA1 is any address that is not in the same block as PA1. X Don't Care, n = number of Words to be programmed.

Table 6. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	Min	Typ (1)	Typical after 10k W/E Cycles (1)	Max	Unit
Chip Erase		21	25	120	s
Block Erase (128 KWords)		1.5		6	s
Program (Word)		9		250	µs
Chip Program (Multiple Word)		4		35	s
Chip Program (Word by Word)		18		35	s
Program/Erase Cycles (per Block)	10,000				cycles

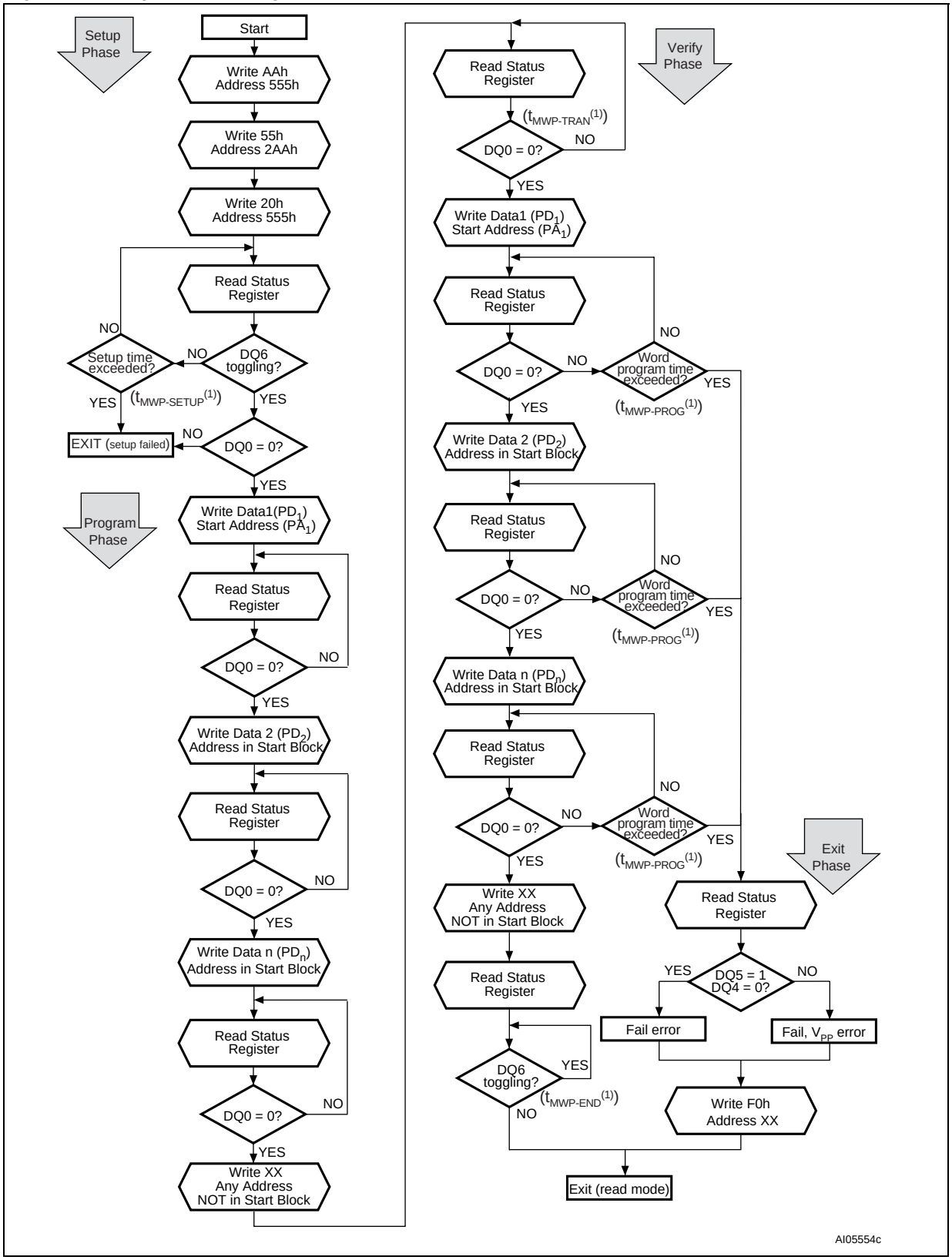
Note: 1. T_A = 25°C, V_{PP} = 12V.

Table 7. Multiple Word Program Timings

Symbol	Parameter	Min	Typ	Max	Unit
$t_{MWP-SETUP}$	MWP Setup time			500	ns
$t_{MWP-PROG}$	MWP Program Time		9	250	µs
$t_{MWP-TRAN}$	MWP Program to Verify transition	2	10	20	µs
$t_{MWP-END}$	MWP Verify to End transition		2	3	µs

Note: 1. MWP = Multiple Word Program.

Figure 5. Multiple Word Program Flowchart



Note: 1. Refer to Table 7, Multiple Word Program Timings, for the values.

STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program and Erase operations. The bits in the Status Register are summarized in Table 8, Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation. The Data Polling Bit is output on DQ7 when the Status Register is read.

During a Word Program operation the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Word Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement. The Data Polling Bit is not available during a Multiple Word Program operation.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

Figure 6, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

Figure 7, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Error Bit (DQ5). The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

V_{PP} Status Bit (DQ4). The V_{PP} Status Bit can be used to identify if any Program or Erase operation has failed due to a V_{PP} error. If V_{PP} falls below V_{HH} during any Program or Erase operation, the operation aborts and DQ4 is set to '1'. If V_{PP} remains at V_{HH} throughout the Program or Erase operation, the operation completes and DQ4 is set to '0'.

Erase Timer Bit (DQ3). The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to '1'. The Erase Timer Bit is output on DQ3 when the Status Register is read.

Alternative Toggle Bit (DQ2). The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Block and Chip Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations to any address. Once the operation completes the memory returns to Read mode.

If an Erase operation fails and the Error Bit is set, the Alternative Toggle Bit will continue to toggle with successive Bus Read operations to any address. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Multiple Word Program Bit (DQ0). The Multiple Word Program Bit can be used to indicate whether the Program/Erase Controller is active or inactive during Multiple Word Program. When the Program/Erase Controller has written one Word and is ready to accept the next Word, the bit is set to '0'.

Status Register Bit DQ1 is reserved.

Table 8. Status Register Bits

Operation	Condition	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ0	RB
Word Program	Any Address	$\overline{DQ7}$	Toggle	0	–	–	–	–	0
Word Program Error	$V_{PP} = V_{HH}$	$\overline{DQ7}$	Toggle	1	0	–	–	–	0
	$V_{PP} < V_{HH}$	$\overline{DQ7}$	Toggle	1	1	–	–	–	0
Block/ Chip Erase	Any Address	0	Toggle	0	–	1	Toggle(2)	–	0
Erase Error	$V_{PP} = V_{HH}$	0	Toggle	1	0	1	Toggle(2)	–	0
	$V_{PP} < V_{HH}$	0	Toggle	1	1	1	Toggle(2)	–	0
Multiple Word Program	P/E.C. active	–	Toggle	0	–	–	–	1	0
	P/E.C. inactive, waiting for next Word	–	Toggle	0	–	–	–	0	1
Multiple Word Program Error	$V_{PP} = V_{HH}$	–	Toggle	1	0	–	–	1	0
	$V_{PP} < V_{HH}$	–	Toggle	1	1	–	–	1	0

Note: 1. Unspecified data bits should be ignored.
2. DQ2 toggles on any address during Block or Chip Erase and after an Erase error.

Figure 6. Data Polling Flowchart

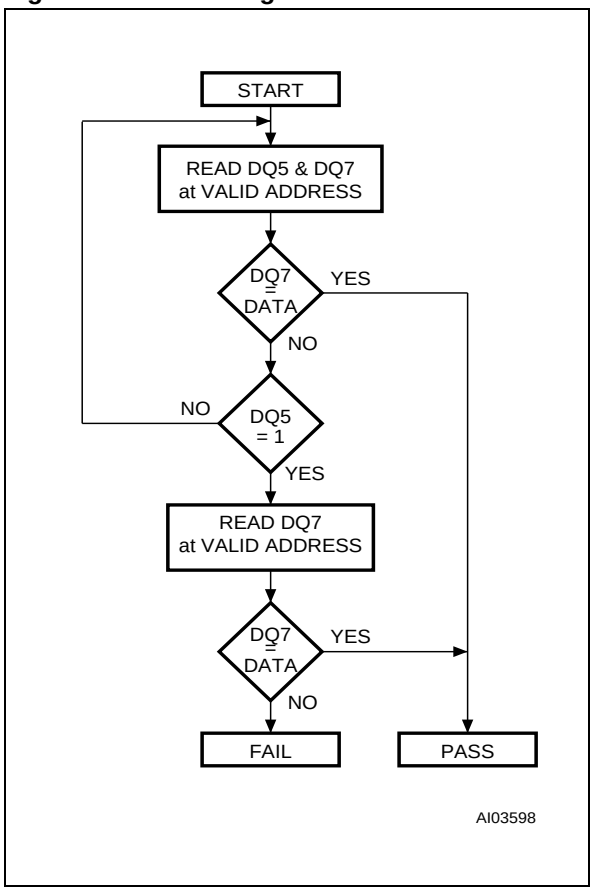
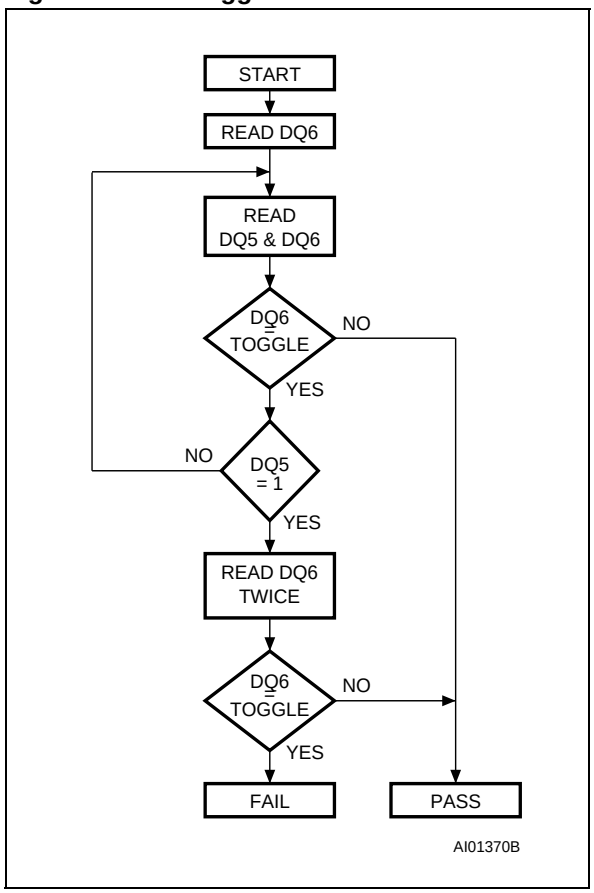


Figure 7. Data Toggle Flowchart



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output Voltage (1,2)	–0.6	V_{CC} +0.6	V
V_{CC}	Read Supply Voltage	–0.6	4	V
V_{PP}	Program/Erase Supply Voltage	–0.6	13.5	V

Note: 1. Minimum voltage may undershoot to –2V for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} +2V for less than 20ns during transitions.
3. Maximum voltage may overshoot to 14.0V for less than 20ns during transitions. V_{PP} must not remain at V_{HH} for more than a total of 80hrs.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 10, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 10. Operating and AC Measurement Conditions

Parameter	M29KW032E				Unit
	90		110		
	Min	Max	Min	Max	
V_{CC} Read Supply Voltage	2.7	3.6	2.7	3.6	V
V_{PP} Program/Erase Supply Voltage	11.4	12.6	11.4	12.6	V
Ambient Operating Temperature	0	70	0	70	°C
Load Capacitance (C_L)	30		30		pF
Input Rise and Fall Times		10		10	ns
Input Pulse Voltages	0 to V_{CC}		0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		$V_{CC}/2$		V

Figure 8. AC Measurement I/O Waveform

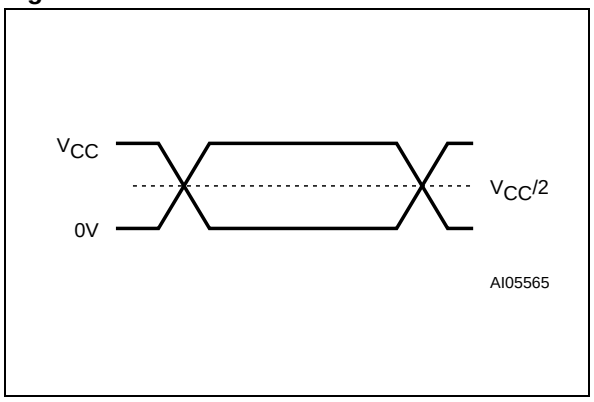


Figure 9. AC Measurement Load Circuit

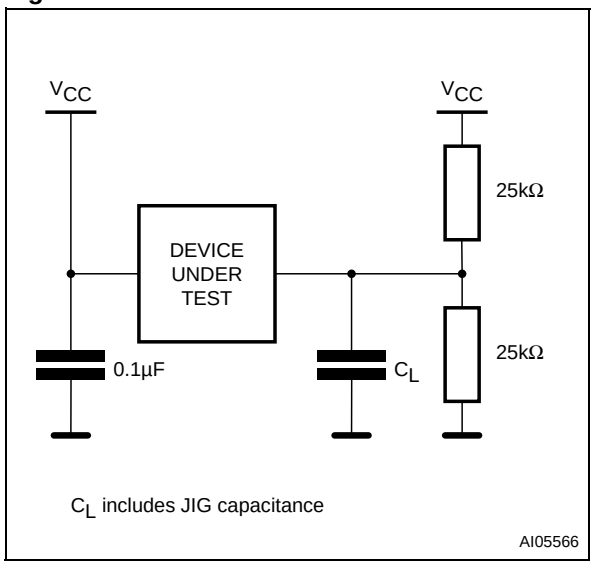


Table 11. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 12. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC2}	Supply Current (Standby)	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC3}	Supply Current (Program/Erase)	P/E.C. active		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	V_{CC} +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} –0.4		V
V_{HH}	V_{PP} Program/Erase Voltage		11.4	12.6	V
I_{HH1}	V_{PP} Current (Read/Standby)	$V_{PP} = V_{HH}$		100	µA
I_{HH2}	V_{PP} Current (Program/Erase)	P/E.C. Active		10	mA
V_{LKO}	Program/Erase Lockout Supply Voltage		1.8	2.3	V

Figure 10. Read AC Waveforms

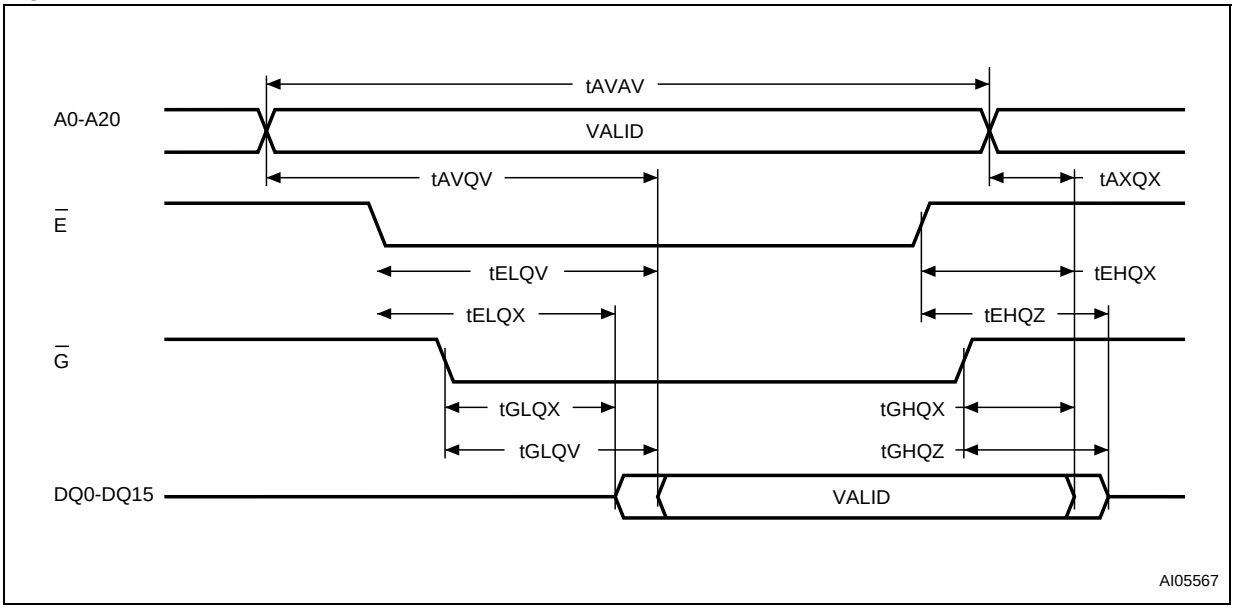


Table 13. Read AC Characteristics

Symbol	Alt	Parameter	Test Condition		M29KW032E		Unit
					90	110	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	90	110	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	90	110	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	90	110	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	35	35	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	30	30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	30	30	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns

Note: 1. Sampled only, not 100% tested.

Figure 11. Write AC Waveforms, Write Enable Controlled

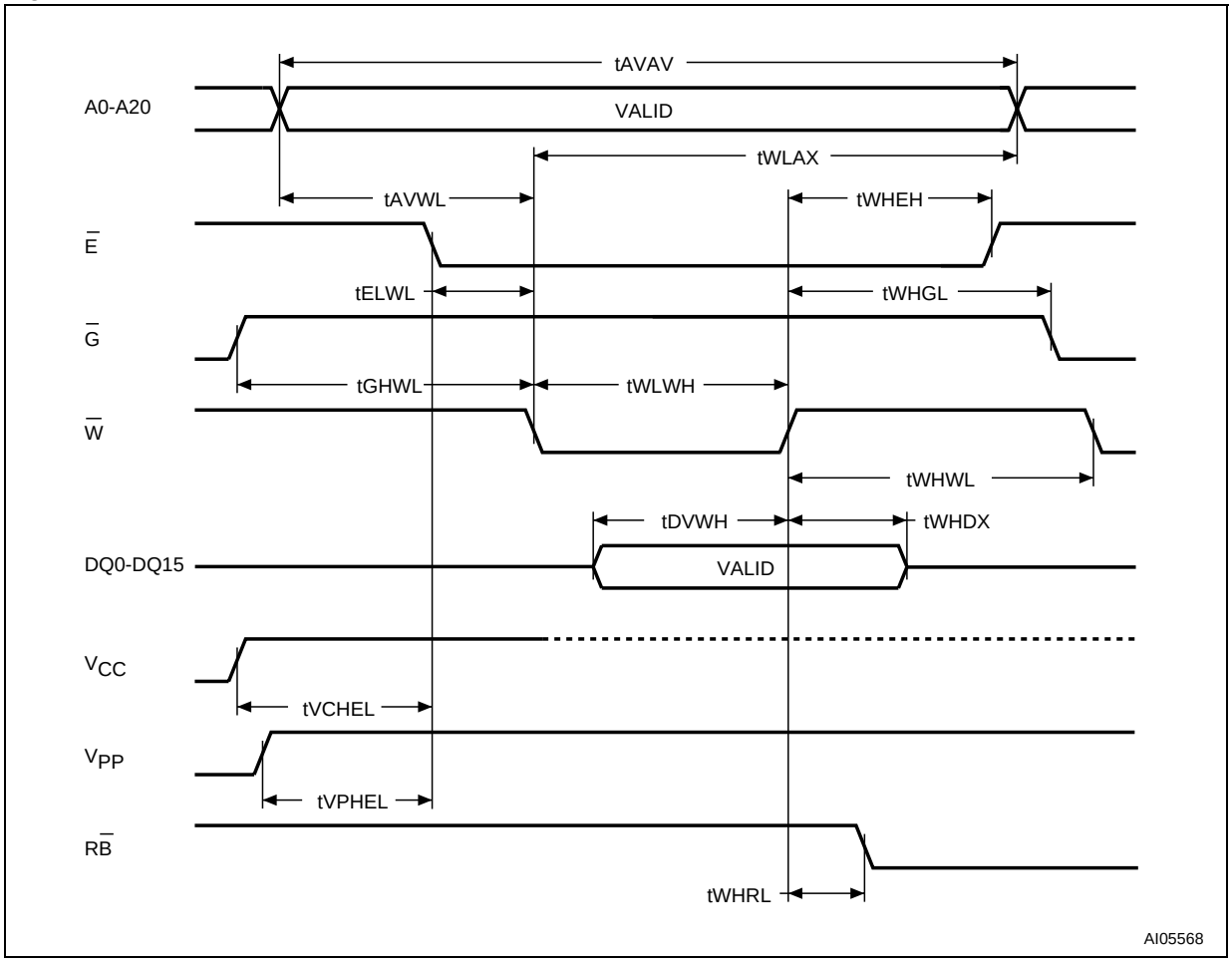


Table 14. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter			M29KW032E		Unit
					90	110	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid		Min	90	110	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low		Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		Min	35	35	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High		Min	35	35	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High		Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		Min	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low		Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		Min	45	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Read mode	Min	0	0	ns
			Read SR Toggle bits	Min	10	10	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Read mode	Min	0	0	ns
			Read SR Toggle bits in Multiple Word Program	Min	20	20	ns
			Read SR Toggle bits other operations	Min	30	30	ns
t_{WHRL} (1)	t_{BUSY}	Program/Erase Valid to $R\overline{B}$ Low		Max	35	35	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		Min	50	50	µs
t_{VPHEL} (2)	t_{VCS}	V_{PP} High to Chip Enable Low		Min	500	500	ns

Note: 1. Sampled only, not 100% tested.
2. Not required in Auto Select or Read/Reset command sequences.

Figure 12. Write AC Waveforms, Chip Enable Controlled

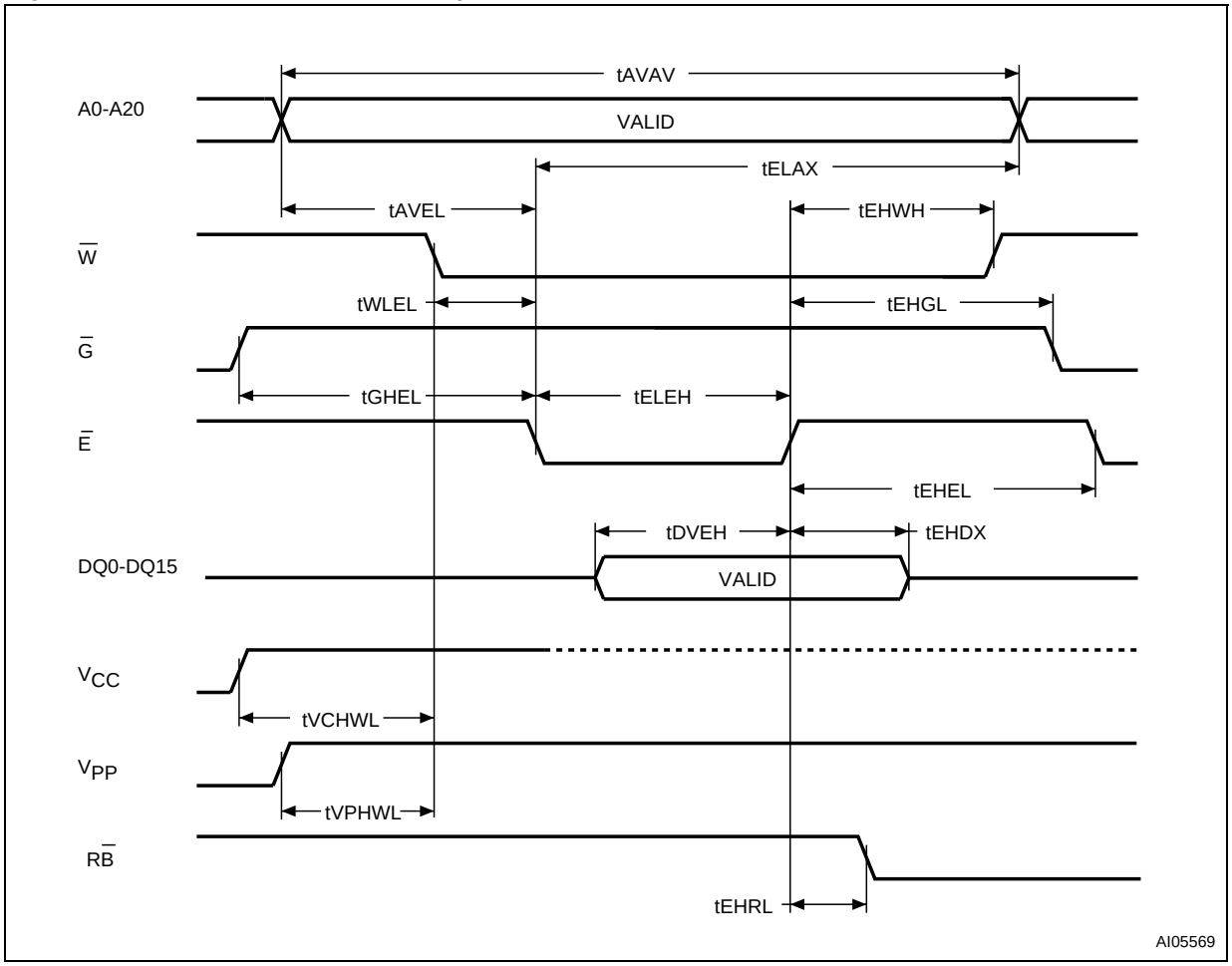


Table 15. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter			M29KW032E		Unit
					90	110	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid		Min	90	110	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low		Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High		Min	35	35	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High		Min	35	35	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High		Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low		Min	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		Min	45	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Read mode	Min	0	0	ns
			Read SR Toggle bits	Min	10	10	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Read mode	Min	0	0	ns
			Read SR Toggle bits in Multiple Word Program	Min	20	20	ns
			Read SR Toggle bits other operations	Min	30	30	ns
t_{EHRL} (1)	t_{BUSY}	Program/Erase Valid to $R\overline{B}$ Low		Max	35	35	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low		Min	50	50	µs
t_{VPHWL} (2)	t_{VCS}	V_{PP} High to Write Enable Low		Min	500	500	ns

Note: 1. Sampled only, not 100% tested.
2. Not required in Auto Select or Read/Reset command sequences.

Figure 13. Reset AC Waveforms

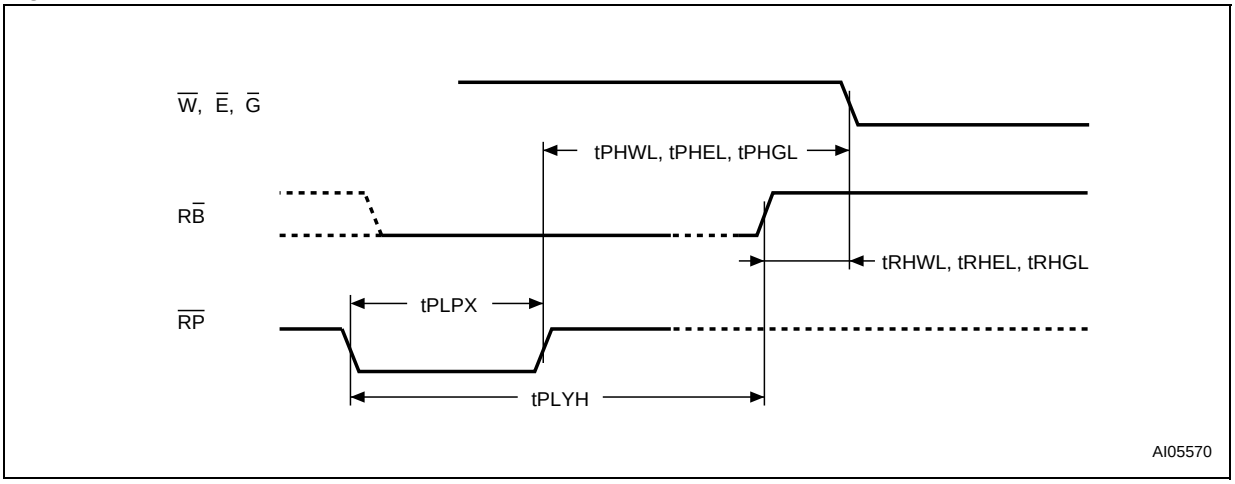


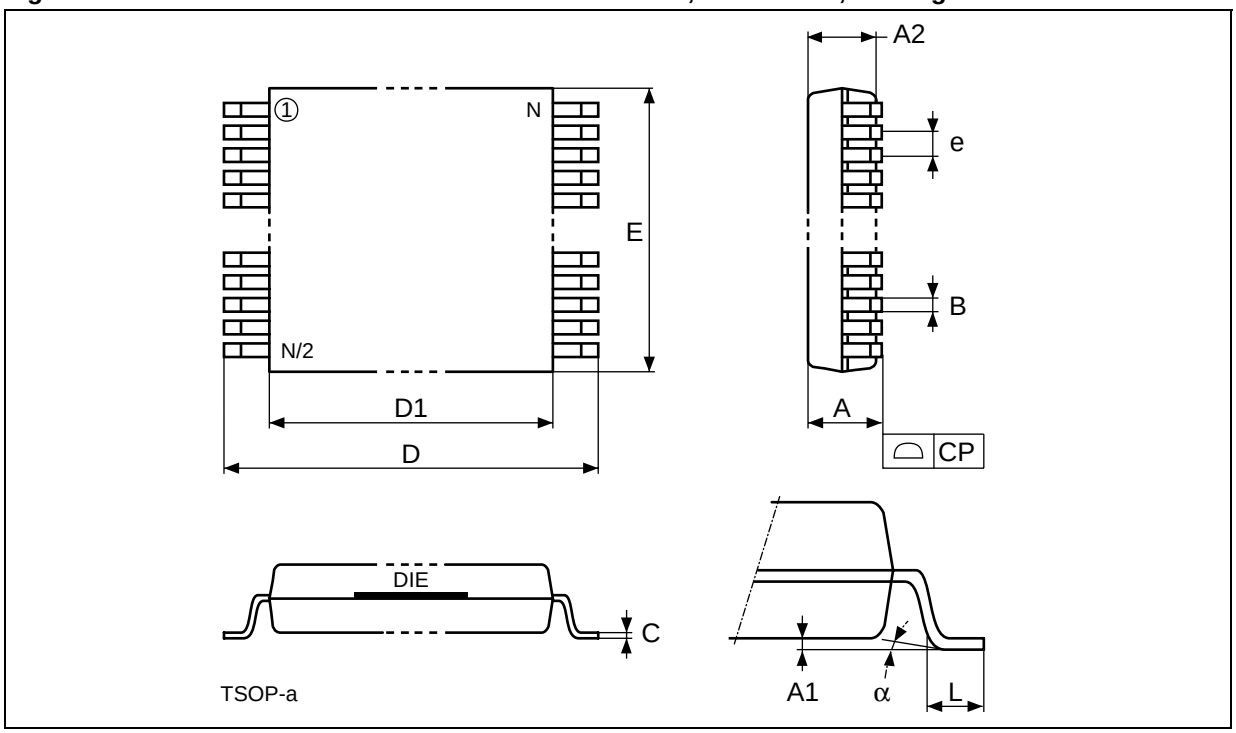
Table 16. Reset AC Characteristics

Symbol	Alt	Parameter		M29KW032E		Unit
				90	110	
t_{PHWL} (1) t_{PHEL} t_{PHGL} (1)	t_{RH}	RP High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	ns
t_{RHWL} (1) t_{RHEL} (1) t_{RHGL} (1)	t_{RB}	RB High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	ns
t_{PLPX}	t_{RP}	RP Pulse Width	Min	500	500	ns
t_{PLYH} (1)	t_{READY}	RP Low to Read Mode	Max	10	10	µs

Note: 1. Sampled only, not 100% tested.

PACKAGE MECHANICAL

Figure 14. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

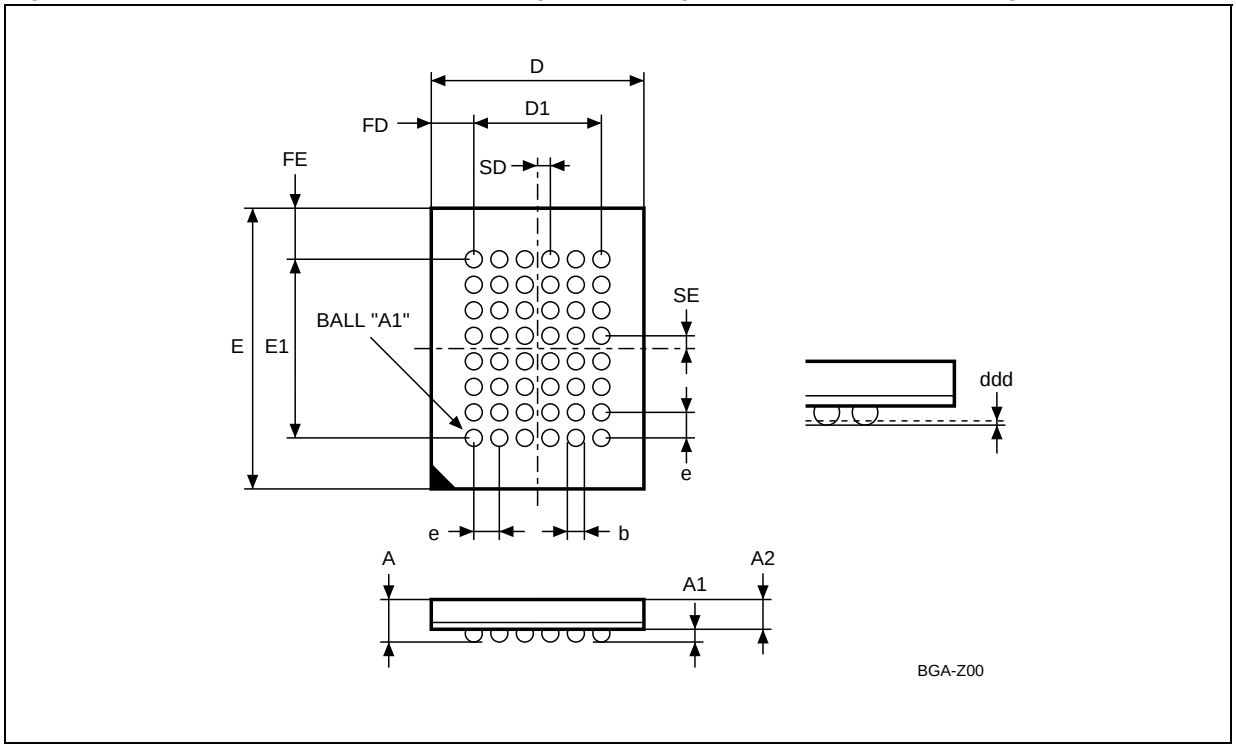


Note: Drawing is not to scale.

Table 17. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		11.90	12.10		0.4685	0.4764
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.0039

Figure 15. TFBGA48 6x9mm - 8x6 ball array, 0.80 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 18. TFBGA48 6x9mm - 8x6 ball array, 0.80 mm pitch, Package Mechanical Data

		millimeters			inches	
Symbol	**Typ**	**Min**	**Max**	**Typ**	**Min**	**Max**
A			1.200			0.0472
A1		0.200			0.0079	
A2			1.000			0.0394
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	4.000	–	–	0.1575	–	–
ddd			0.100			0.0039
E	9.000	8.900	9.100	0.3543	0.3504	0.3583
e	0.800	–	–	0.0315	–	–
E1	5.600	–	–	0.2205	–	–
FD	1.000	–	–	0.0394	–	–
FE	1.700	–	–	0.0669	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

Figure 16. TFBGA48 Daisy Chain - Package Connections (Top view through package)

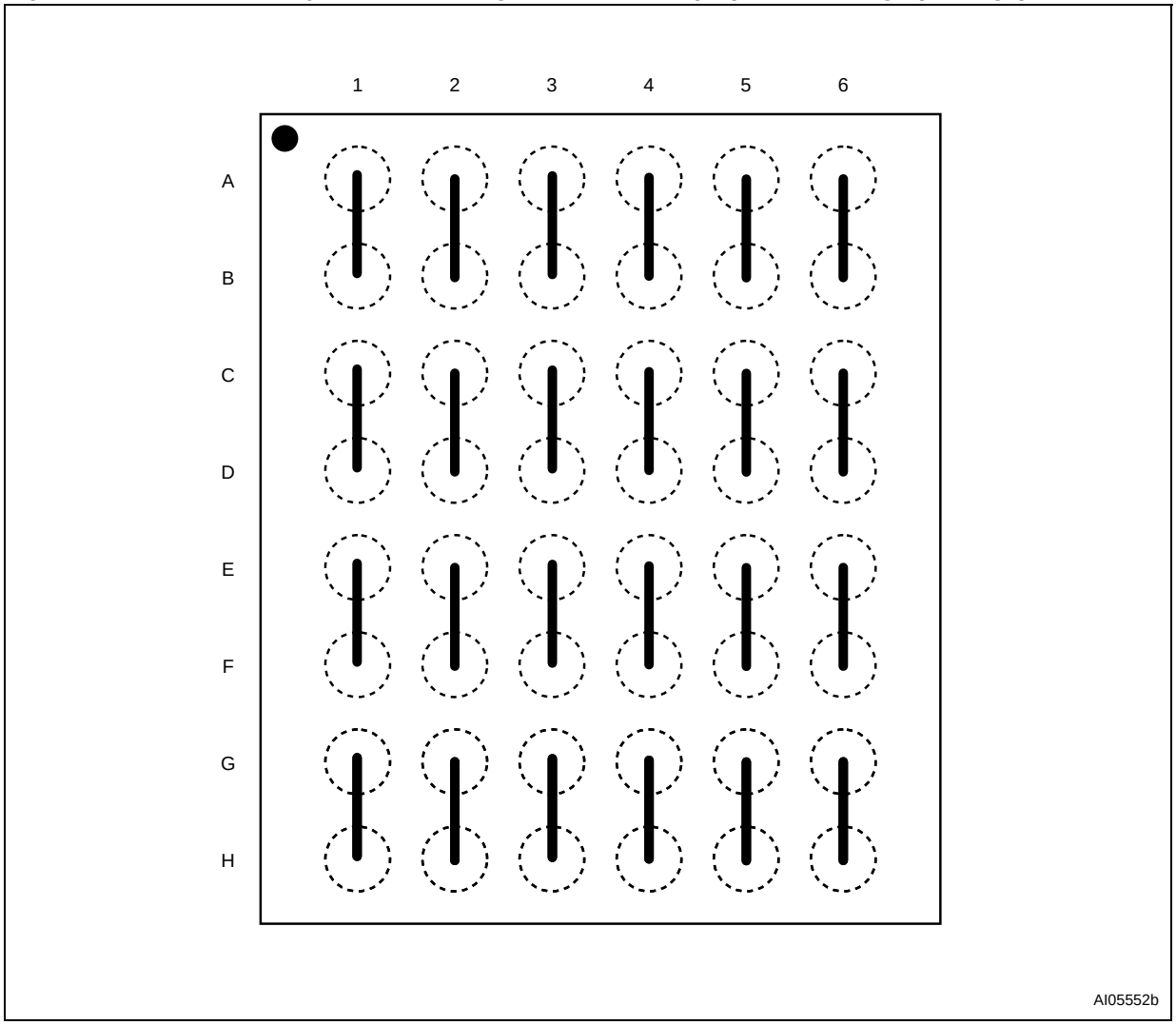
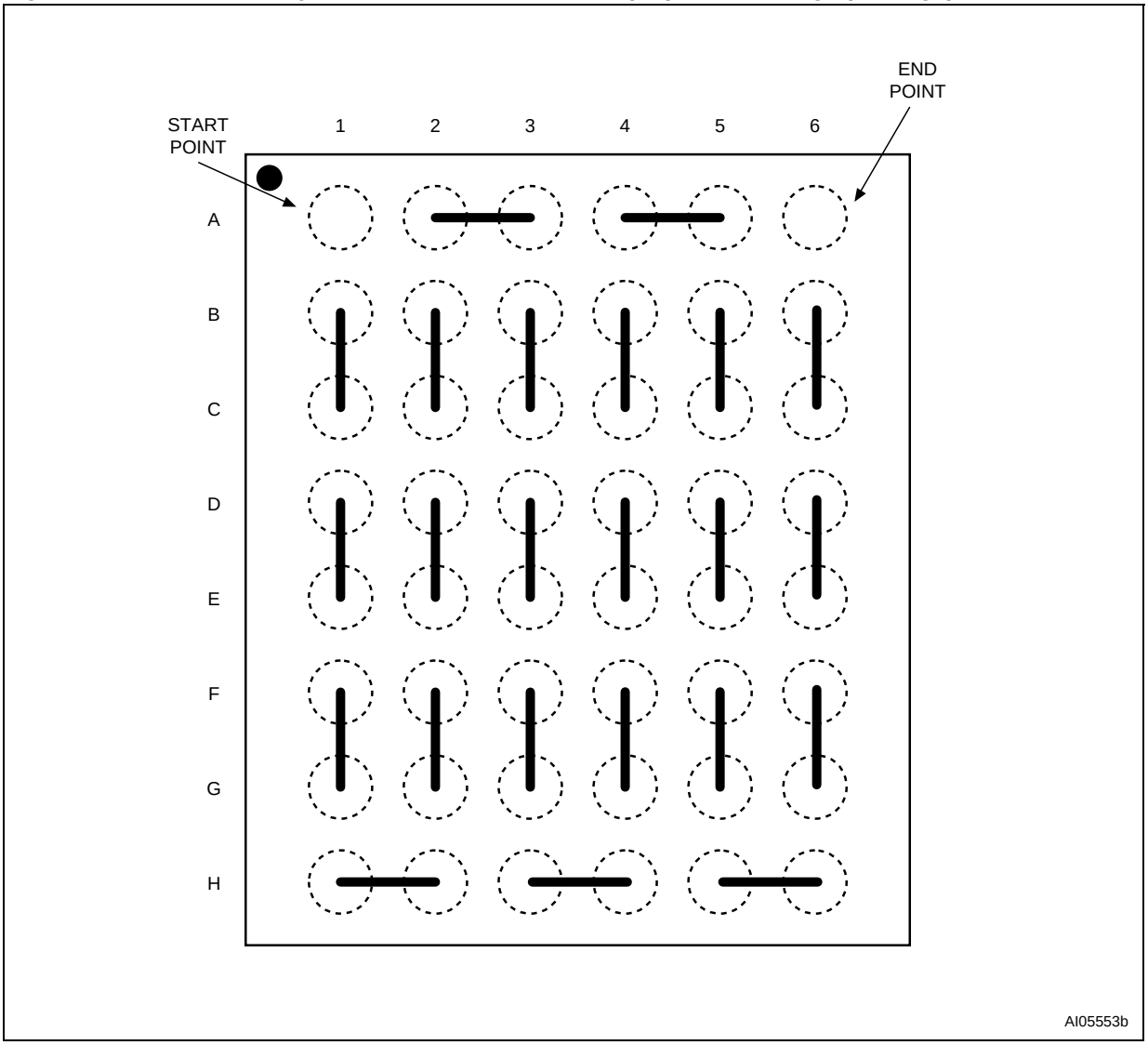


Figure 17. TFBGA48 Daisy Chain - PCB Connections (Top view through package)



PART NUMBERING

Table 19. Ordering Information Scheme

Example: M29KW032E 90 N 1 T

Device Type
M29K = LightFlash™

Operating Voltage
W = V_{CC} = 2.7 to 3.6V

Device Function
032E = 32 Mbit (x16)

Speed
90 = 90 ns
110 = 110 ns

Package
N = TSOP48: 12 x 20 mm
ZA = TFBGA48: 6 x 9mm - 0.80mm pitch

Temperature Range
1 = 0 to 70 °C

Option
T = Tape & Reel Packing

Table 20. Daisy Chain Ordering Scheme

Example: M29K DCL3-32 T

Device Type
M29K

Daisy Chain
DCL3-32 = Daisy Chain Level 3 for 32 Mbit parts

Option
T = Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 21. Document Revision History

Date	Version	Revision Details
09-Oct-2001	-01	First Issue
07-May-2002	-02	LFBGA changed to TFBGA package. Write AC Characteristics t_{WLWH}, t_{DVWH}, t_{WLAX}, t_{GHWL}, t_{WHGL}, t_{ELEH}, t_{DVEH}, t_{ELAX}, t_{GHEL} and t_{EHGL} modified. Typical Chip Program and Erase times modified, Multiple Word Program description and flowchart clarified, Alternative Toggle Bit DQ2 description clarified, Status Register Bits Table modified. Document classed as Product Preview.
12-Jul-2002	-03	Figure 7 modified.
23-Jul-2002	3.1	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot. (revision version 03 becomes 3.0). Figure 5, Multiple Word Program Flowchart, modified; Table 7, Multiple Word Program Timings, added.