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Agilent Technologies

# Small Outline, 5 Lead, High Speed Optocouplers

## Technical Data

**HCPL-M452**
**HCPL-M453**

### Features

- **Surface Mountable**
- **Very Small, Low Profile JEDEC Registered Package Outline**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **Very High Common Mode Transient Immunity: 15000 V/µs at $V_{CM}$ = 1500 V Guaranteed (HCPL-M453)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Guaranteed AC and DC Performance over Temperature: 0°C to 70°C**
- **Open Collector Output**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltage of 3750 Vac, 1 Minute**
- **Lead Free Option**

### Description

These small outline high CMR, high speed, diode-transistor opto-couplers are single channel devices in a five lead miniature footprint. They are electrically equivalent to the following Agilent optocouplers:

| SO-5 Package | Standard DIP | SO-8 Package |
|---|---|---|
| HCPL-M452 | HCPL-4502 | HCPL-0452 |
| HCPL-M453 | HCPL-4503 | HCPL-0453 |

(Note: These devices equivalent to 6N135/6N136 devices but without the base lead.)

The SO-5 JEDEC registered (MO-155) package outline does not require “through holes” in a PCB. This package occupies approximately one-fourth the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

These diode-transistor optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times

*CAUTION: The small device geometries inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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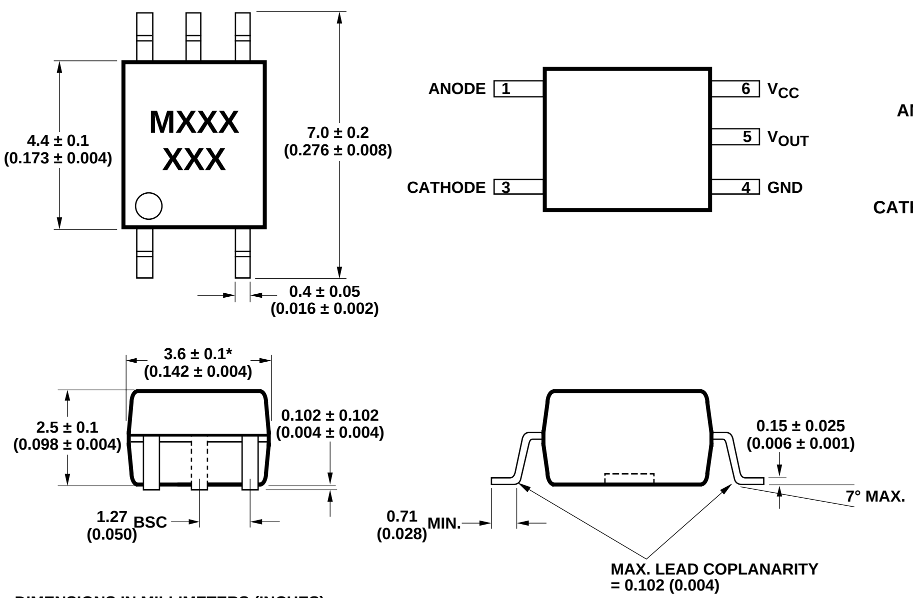
over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The HCPL-M452 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the HCPL-M452 is 19% minimum at $I_F$ = 16 mA.

The HCPL-M453 is an HCPL-M452 with increased common mode transient immunity of 15,000 V/µs minimum at $V_{CM}$ = 1500 V guaranteed.

## Outline Drawing (JEDEC MO-155)

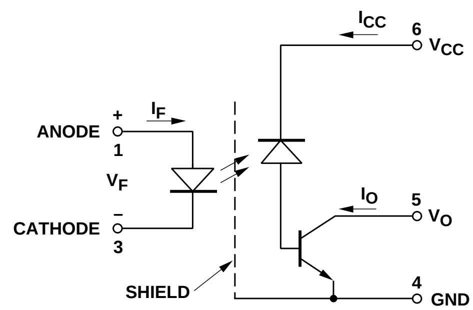



DIMENSIONS IN MILLIMETERS (INCHES)

* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

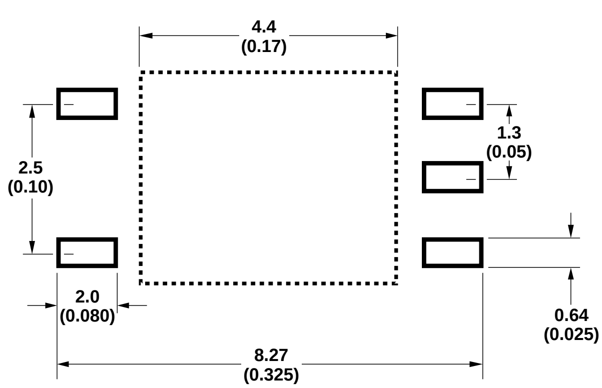
## Schematic




## Applications

- **Line Receivers -** High common mode transient immunity (>1000 V/µs) and low input-output capacitance (0.6 pF).
- **High Speed Logic Ground Isolation - TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.**
- **Replace Slow Phototransistor Optocouplers**
- **Replace Pulse Transformers -** Save board space and weight
- **Analog Signal Ground Isolation -** Integrated photon detector provides improved linearity over phototransistor type.

## Land Pattern Recommendation



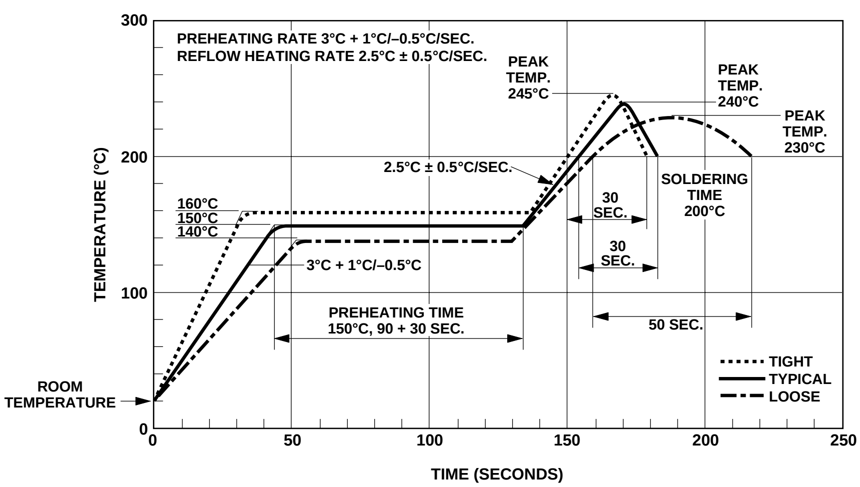

DIMENSIONS IN MILLIMETERS AND (INCHES)

## Absolute Maximum Ratings

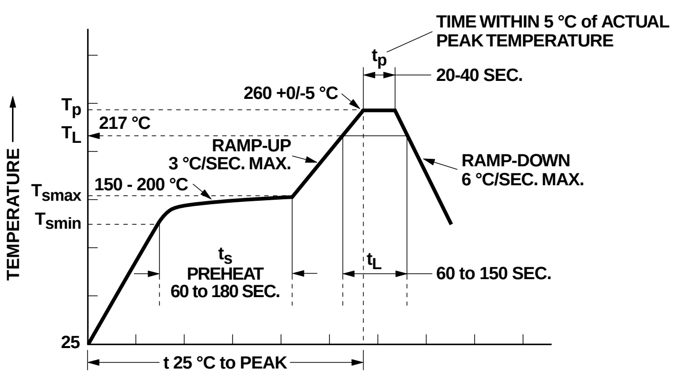
(No Derating Required up to 85°C)

Storage Temperature ................................................ -55°C to +125°C
Operating Temperature ........................................... -55°C to +100°C
Average Input Current - $I_F$ ................................................... 25 mA[1]
Peak Input Current - $I_F$ ......................................................... 50 mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current - $I_F$ ............................................ 1.0 A
(≤1 µs pulse width, 300 pps)
Reverse Input Voltage - $V_R$ (Pin3-1) .............................................. 5 V
Input Power Dissipation ....................................................... 45 mW[3]
Average Output Current - $I_O$ (Pin 5) .......................................... 8 mA
Peak Output Current .............................................................. 16 mA
Output Voltage - $V_O$ (Pin 5-4) ....................................... -0.5 V to 20 V
Supply Voltage - $V_{CC}$ (Pin 6-4) ..................................... -0.5 V to 30 V
Output Power Dissipation .................................................. 100 mW[4]
Infrared and Vapor Phase Reflow Temperature ................. see below

## Solder Reflow Thermal Profile




## Recommended Pb-Free IR Profile




NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
$T_{smax}$ = 200 °C, $T_{smin}$ = 150 °C

## Insulation Related Specifications

| Parameter | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Min External Air Gap (Clearance) | L(IO1) | ≥ 5 | mm | Measured from input terminals to output terminals |
| Min. External Tracking Path (Creepage) | L(IO2) | ≥ 5 | mm | Measured from input terminals to output terminals |
| Min. Internal Plastic Gap (Clearance) | | 0.08 | mm | Through insulation distance conductor to conductor |
| Tracking Resistance | CTI | 175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group (per DIN VDE 0109) | | IIIa | | Material Group DIN VDE 0109 |

## Electrical Specifications

Over recommended temperature ($T_A$ = 0°C to 70°C) unless otherwise specified. (See note 11.)

| Parameter | Symbol | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Current Transfer Ratio | CTR | 20 | 24 | 50 | % | $T_A$ = 25°C, $V_O$ = 0.4 V; $V_{CC}$ = 4.5 V, $I_F$ = 16 mA | 1, 2, 4 | 5 |
| | | 15 | 25 | | % | $V_O$ = 0.5 V; $V_{CC}$ = 4.5 V, $I_F$ = 16 mA | | |
| Logic Low Output Voltage | $V_{OL}$ | | 0.1 | 0.4 | V | $T_A$ = 25°C, $I_O$ = 3.0 mA; $V_{CC}$ = 4.5 V, $I_F$ = 16 mA | | |
| | | | | 0.5 | V | $I_O$ = 2.4 mA; $V_{CC}$ = 4.5 V, $I_F$ = 16 mA | | |
| Logic High Output Current | $I_{OH}$ | | 0.003 | 0.5 | µA | $T_A$ = 25°C, $V_O$ = $V_{CC}$ = 5.5 V; $I_F$ = 0 mA | 7 | |
| | | | 0.01 | 1 | µA | $T_A$ = 25°C, $V_O$ = $V_{CC}$ = 15.0 V; $I_F$ = 0 mA | | |
| | | | | 50 | µA | $I_F$ = 0 mA | | |
| Logic Low Supply Current | $I_{CCL}$ | | 50 | 200 | µA | $I_F$ = 16 mA, $V_O$ = Open, $V_{CC}$ = 15 V | | 11 |
| Logic High Supply Current | $I_{CCH}$ | | 0.02 | 1 | µA | $T_A$ = 25°C, $I_F$ = 0 mA, $V_O$ = Open, $V_{CC}$ = 15.0 V | | 11 |
| | | | | 2 | µA | $I_F$ = 0 mA, $V_O$ = Open, $V_{CC}$ = 15.0 V | | |
| Input Forward Voltage | $V_F$ | | 1.5 | 1.7 | V | $T_A$ = 25°C, $I_F$ = 16 mA | 3 | |
| | | | | 1.8 | V | $I_F$ = 16 mA | | |
| Input Reverse Breakdown Voltage | $BV_R$ | 5 | | | V | $I_R$ = 10 µA | | |
| Temperature Coefficient of Forward Voltage | $\Delta V_F/\Delta T_A$ | | -1.6 | | mV/°C | $I_F$ = 16 mA | | |
| Input Capacitance | $C_{IN}$ | | 60 | | pF | f = 1 MHz, $V_F$ = 0 | | |
| Input-Output Insulation | $V_{ISO}$ | 3750 | | | $V_{RMS}$ | RH ≤ 50%, t = 1 min., $T_A$ = 25°C | | 6, 7 |
| Resistance (Input-Output) | $R_{I-O}$ | | $10^{12}$ | | Ω | $V_{I-O}$ = 500 $V_{DC}$ | | 6 |
| Capacitance (Input-Output) | $C_{I-O}$ | | 0.6 | | pF | f = 1 MHz | | 6 |

## Switching Specifications

Over recommended temperature ($T_A$ = 0°C to 70°C) $V_{CC}$ = 5 V, $I_F$ = 16 mA unless otherwise specified.

| Parameter | Symbol | Device | Min. | Typ.* | Max. | Units | Test Conditions | | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low at Output | $t_{PHL}$ | | | 0.2 | 0.8 | μs | $T_A$ = 25°C | $R_L$ = 1.9 kΩ | 5, 6, 10 | 9 |
| | | | | | 1.0 | | | | | |
| Propagation Delay Time to Logic High at Output | $t_{PLH}$ | | | 0.6 | 0.8 | | $T_A$ = 25°C | $R_L$ = 1.9 kΩ | 5, 6, 10 | 9 |
| | | | | | 1.0 | | | | | |
| Common Mode Transient Immunity at Logic High Level Output | $\lvert CM_H \rvert$ | HCPL-M452 | | 1 | | kV/μs | $V_{CM}$ = 10 $V_{p-p}$ | $I_F$ = 0 mA, $T_A$ = 25°C, $R_L$ = 1.9 kΩ | 11 | 8, 9 |
| | | HCPL-M453 | 15 | 30 | | | $V_{CM}$ = 1500 $V_{p-p}$ | | | |
| Common Mode Transient Immunity at Logic Low Level Output | $\lvert CM_L \rvert$ | HCPL-M452 | | 1 | | | $V_{CM}$ = 10 $V_{p-p}$ | $I_F$ = 16 mA, $T_A$ = 25°C, $R_L$ = 1.9 kΩ | 11 | 8, 9 |
| | | HCPL-M453 | 15 | 30 | | | $V_{CM}$ = 1500 $V_{p-p}$ | | | |
| Bandwidth | BW | | | 3 | | MHz | $R_L$ = 100 Ω, See Test Circuit | | 8, 9 | 10 |

All typicals at $T_A$ = 25°C.

**Notes:**

1. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.
2. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.
3. Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, $I_O$, to the forward LED input current, $I_F$, times 100.
6. Device considered a two terminal device: pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 $V_{RMS}$ for 1 second (leakage detection current limit, $I_{I-O}$ ≤ 5 μA).
8. Common transient immunity in a Logic High level is the maximum tolerable (positive) $dV_{CM}/dt$ on the rising edge of the common mode pulse, $V_{CM}$, to assure that the output will remain in a Logic High state (i.e., $V_O$ > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) $dV_{CM}/dt$ on the falling edge of the common mode pulse signal, $V_{CM}$ to assure that the output will remain in a Logic Low state (i.e., $V_O$ < 0.8 V).
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
11. Use of a 0.1 μF bypass capacitor connected between pins 4 and 6 is recommended.

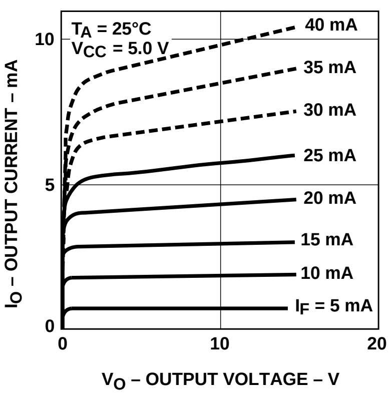



**Figure 1. dc and Pulsed Transfer Characteristics.**

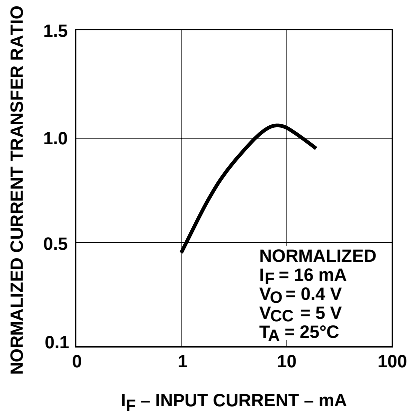



**Figure 2. Current Transfer Ratio vs. Input Current.**

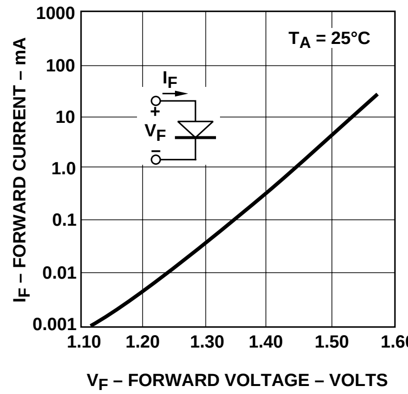



**Figure 3. Input Current vs. Forward Voltage.**

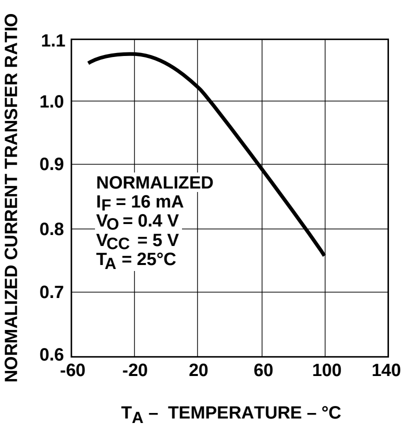



**Figure 4. Current Transfer Ratio vs. Temperature.**

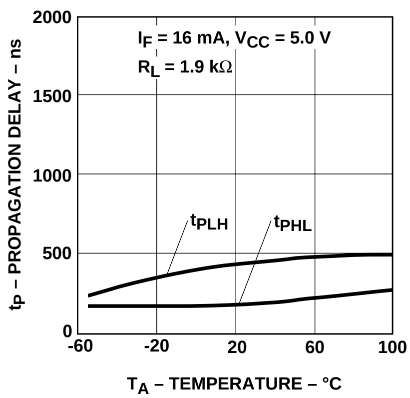



**Figure 5. Propagation Delay vs. Temperature.**

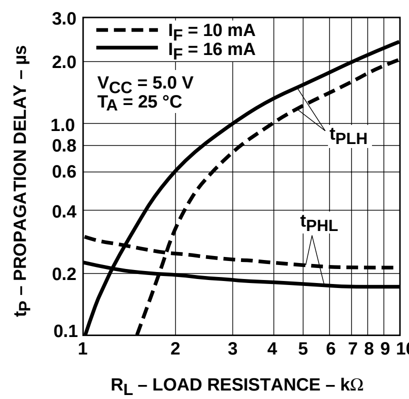



**Figure 6. Propagation Delay Time vs. Load Resistance.**

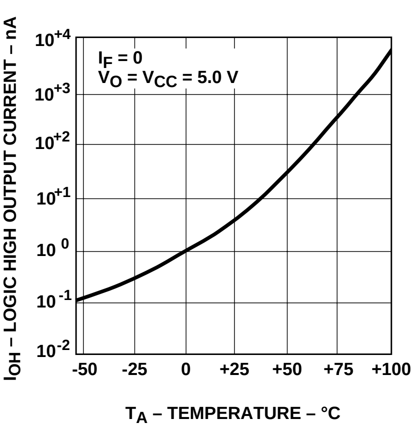



**Figure 7. Logic High Output Current vs. Temperature.**

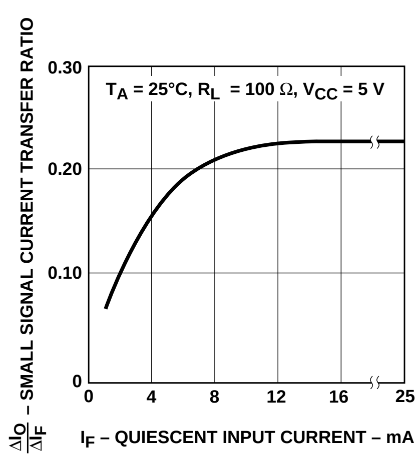



**Figure 8. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.**

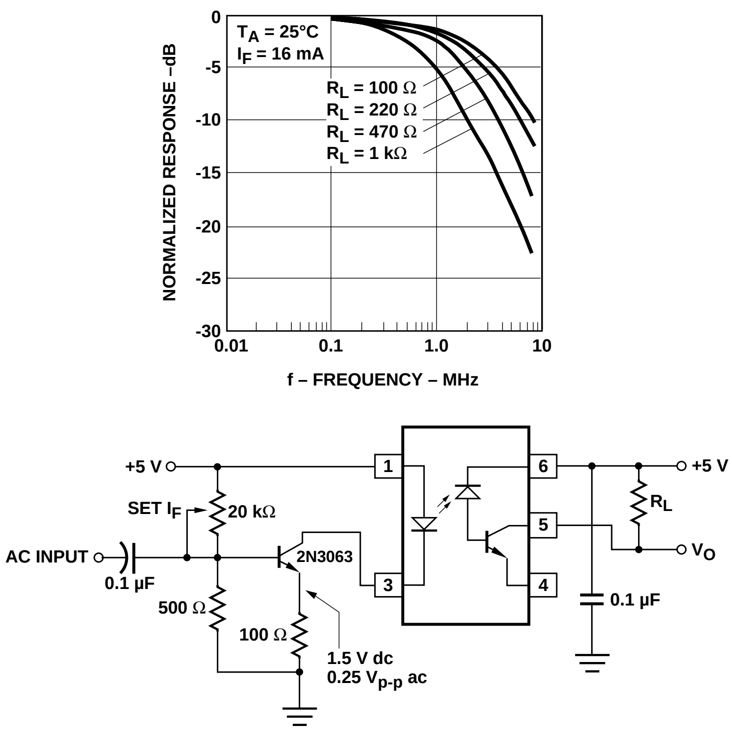



Figure 9. Frequency Response.

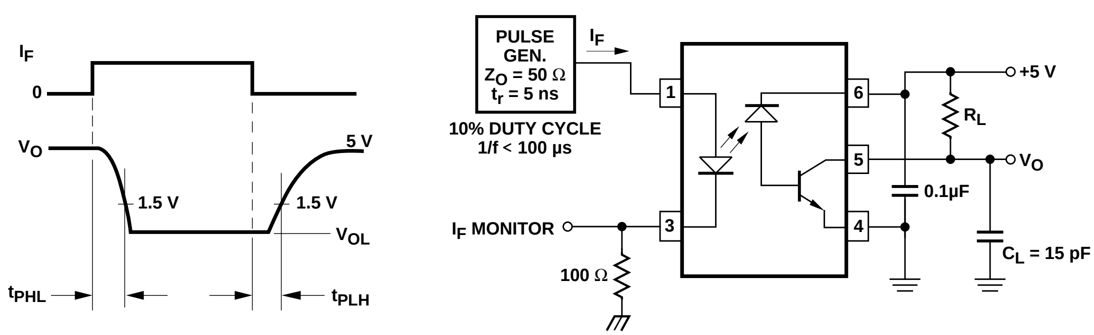



Figure 10. Switching Test Circuit.

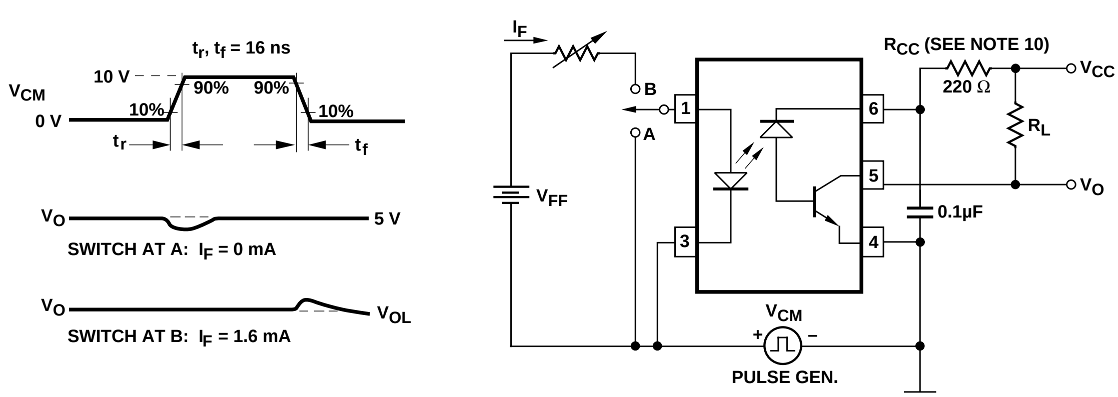



Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

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Obsoletes 5989-0792EN
December 28, 2004
5989-2117EN