Dual Input Ultra Low Dropout Voltage Regulator (ULDO)

L1581 Series TO-252

GENERAL DESCRIPTION

The L1581 is a positive and very low dropout voltage regulator with 5A output current capability. When supplying 2.5V or 2.8V on Motherboards or VGA Card where both 5V and 3.3V supplies are available, the superior dropout characteristics of the L1581 result in reduced heat dissipation compared to regular LDOs, thus allowing heat sink reduction. The adjustable version requires only two external resistors to set the output. The L1581 features a low dropout of less than 600mV and offers fast transient response, remote sense, internal limiting, thermal shutdown and operating area protection of the output device.

The L1581 is a five terminal adjustable voltage regulator available in the popular 5 pin TO-252 packages.

FEATURES

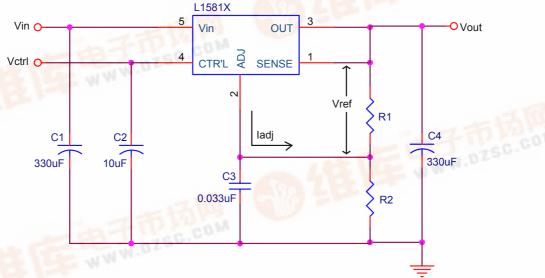
- Low dropout voltage 600mV at rated load current
- Remote sense operation
- Fast transient response
- 0.5% voltage reference initial accuracy
- Standard 5 terminal, Low cost TO-252 packages

APPLICATIONS

- 3.3V to 2.8V or 2.5V for Motherboards or VGA Card
- Spilt plane microprocessor supplies
- Post regulator for switching supplies

TYPICAL APPLICATION

Adjustable Output Parts⁽²⁾



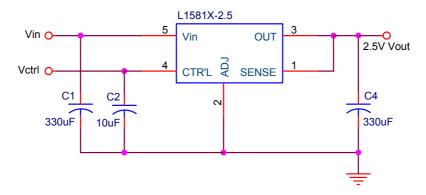
Vo = Vref (1+R2/R1) + ladj x R2

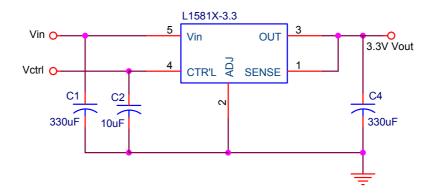


Dual Input Ultra Low Dropout Voltage Regulator (ULDO)

L1581 Series TO-252

Fixed Output Parts





NOTES:

- (1) If the same voltage is input to both INPUT and CONTROL, then the dropout voltage will become 1.3V maximum.
- (2) A small (~0.033uF) capacitor can be used to bypass the ADJUST pin to improve transient response, if needed.
- (3) Capacitor values are for reference only. Good quality, low ESR tantalum or aluminum electrolytic capacitors should be used. Increasing the value of the output capacitor will improve the overall transient response.

2

Dual Input Ultra Low Dropout Voltage Regulator (ULDO)

L1581 Series TO-252

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}
 Control Input Voltage, V_{CTRL}
 Internally

Power Dissipation, P_D
 Internally Limited

Thermal Resistance
 Junction to Case, θ_{JC}

 Thermal Resistance Junction to Ambient, θ_{JA} Operating Junction Temperature Range, T_J
 Storage Temperature

Range, T_J 0 to 125 °C

 Storage Temperature Range, T_{STG}

-40 to 150 °C

 Lead Temperature, T_{LEAD} (Soldering, 10 Seconds)

260 °C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{out} = V_{sns}$, $V_{adj} = 0V$,

3 °C/W

60 °C/W

$$C_{ctl} = C_{in} = C_{out} = 10 \text{ uF}, T_J = 25 \text{ °C})$$

Parameter	Symbol	Test Conditions	Typical	Limits	
Reference Voltage ⁽¹⁾	V_{REF}	◆V _{CTRL} =4.5V, V _{IN} =2.05V, I _{OUT} =10mA		◆1.237V~1.263V	
(Adj. Voltage Versions)		$V_{CTRL} = 4.5V$, $10mA < I_{OUT} < 5A$, $V_{IN} = 2.05V$	1.25V	◆1.231V~1.269V	
Dropout Voltage ^{(1) (2)} Minimum V _{IN}	V _I - V _O	V _{CTRL} = 4.75V, I _{OUT} = 5A	0.54V	0.62V (Max)	
Output Voltage ⁽¹⁾ (Fixed Voltage Versions)	V _{OUT}	\bullet V _{CTRL} = 5V, V _{IN} = V _{OUT} + 0.8V, I _{OUT} =10mA	V	± 1%	
		\bullet V _{CTRL} = 5V, 10mA < I _{OUT} < 5A, V _{IN} = V _{OUT} + 0.8V	V _{OUT}	± 1.5%	
Line Regulation ⁽¹⁾	REG _(LINE)	V_{CTRL} = 4.5V to 12V, V_{IN} = (V_{OUT} + 0.8V) to 5.5V, I_{OUT} = 10mA	1.0mV	3.0mV	
Load Regulation	REG _(LOAD)	V_{CTRL} = 4.5V, V_{IN} = (V_{OUT} + 0.8V), I_{OUT} = 10mA ~ 5A	1.0mV	5.0mV	
Thermal Regulation ⁽⁶⁾	REG _(Thermal)		0.002	0.02% / W	
			% / W		
Minimum Load Current ⁽⁴⁾	Io	V_{CTRL} = 5V, V_{IN} = V_{OUT} + 0.8V	5mA	10mA	
Adjust Pin Current	I _{ADJ}	V_{CTRL} = 4.5V, V_{IN} = V_{OUT} + 0.8V, I_{OUT} = 10mA	50μΑ	120μΑ	
Control Pin Current ⁽³⁾	I _{CTRL}	V_{CTRL} = 4.5V, V_{IN} = V_{OUT} + 0.8V, I_{OUT} = 5A	33mA	120mA	
Current Limit	I _{CL}	V_{CTRL} = 4.5V, V_{IN} = V_{OUT} + 0.8V ΔV_{OUT} = 100mV		5.1A (Min)	

3

Dual Input Ultra Low Dropout Voltage Regulator (ULDO)

L1581 Series TO-252

Ripple Rejection Ratio ⁽⁵⁾	R _A	$V_{CTRL} = V_{IN} = 5V$, $I_{OUT} = 5A$	80dB	60dB (Min)
---------------------------------------	----------------	---	------	------------

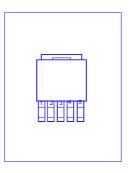
NOTE:

- (1) Low duty cycle pulse testing with Kelvin connections required.
- (2) Minimum input to output voltage differential required to maintain 1% regulation.
- (3) Current used to drive the output section.
- (4) Required to maintain regulation. Resistor divider R1, R2 is usually utilized for minimum load current.
- (5) VRIPPLE = 1VPK-PK, 120Hz.
- (6) 30ms.

DEVICE SELECTION GUIDE

Device	L1581D	L1581D-2.5	L1581D-3.3		
Package	TO-252	TO-252	TO-252		
Marking	L1581D	L1581D-2.5	L1581D-3.3		

PIN CONFIGURATIONS



Pin#	Function			
1	Sense			
2	Adjust			
3	Output			
4	Control			
5	Input			

Note: TAB is Output Pin

Dual Input Ultra Low Dropout Voltage Regulator (ULDO)

L1581 Series TO-252

PIN FUNCTIONS

NO	FUNCTION	DESCRIPTION
1	Sense	This pin is the positive side of the reference voltage for the device. With this pin it is possible to Kelvin sense the output voltage at the load.
2	Adjust	This pin is the negative side of the reference voltage for the device. Transient response can be improved by adding a small bypass capacitor from the adjust pin to ground.
3	Output	This is the power output of the device, and is electrically connected to the TAB.
4	Control	This pin is the supply pin for the control circuitry for the device. The current flow into this pin will be approximately 1% of the output. For the device to regulate, the voltage at this pin must be between 1.0V and 1.3V greater than the output voltage (see dropout specifications).
5	Input	This is the collector input to the power device of the L1581. The output load current is supplied through this pin. For the device to regulate, the voltage on this pin must be between 0.1V and 0.7V greater than the output, depending upon load current (see dropout specifications).

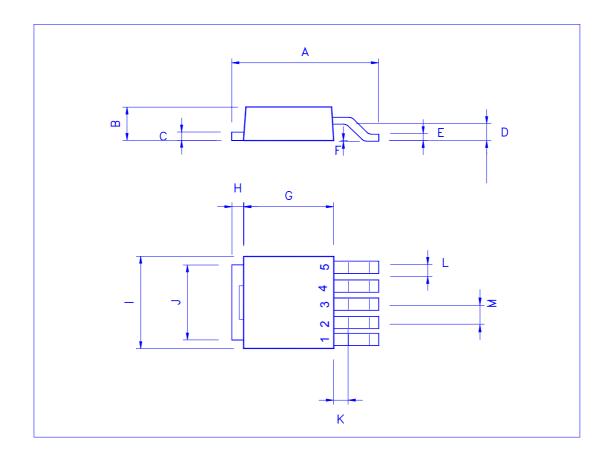
5

Dual Input Ultra Low Dropout Voltage Regulator (ULDO)

L1581 Series TO-252

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			D'	mm		
	Min.	Тур.	Max.	Dimension	Min.	Тур.	Max.
Α		9.7		Н	0.89		2.03
В	2.19		2.38	I	6.35		6.73
С	0.46		0.58	J	5.21		5.46
D	0.89		1.27	K			
Е	0.46		0.53	L	0.64		0.89
F	0.00		0.13	М		1.27BSC	
G	3.04		5.33	N			



6