2.5V LCD Panel Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 15dB of EMI suppression.
- Generates a low EMI spread spectrum clock of the input frequency.
- Input frequency range: 30MHz to 75 MHz.
- Optimized for 32.5MHz, 54MHz, and 65MHz.
- Internal loop filter minimizes external components and board space.
- Selectable spread deviation.
- SSON# control pin for spread spectrum enable and disable options.
- Low cycle-to-cycle jitter.
- 2.5V or 3.3V operating voltage range.
- TTL or CMOS compatible outputs.
- Ultra-low power CMOS design.
- Supports most mobile graphic accelerator and LCD timing controller specifications.
- Available in 8-pin SOIC and TSSOP.

Product Description

The L2042A is a versatile spread spectrum frequency modulator designed specifically for digital falt panel applications. The L2042A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The L2042A allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

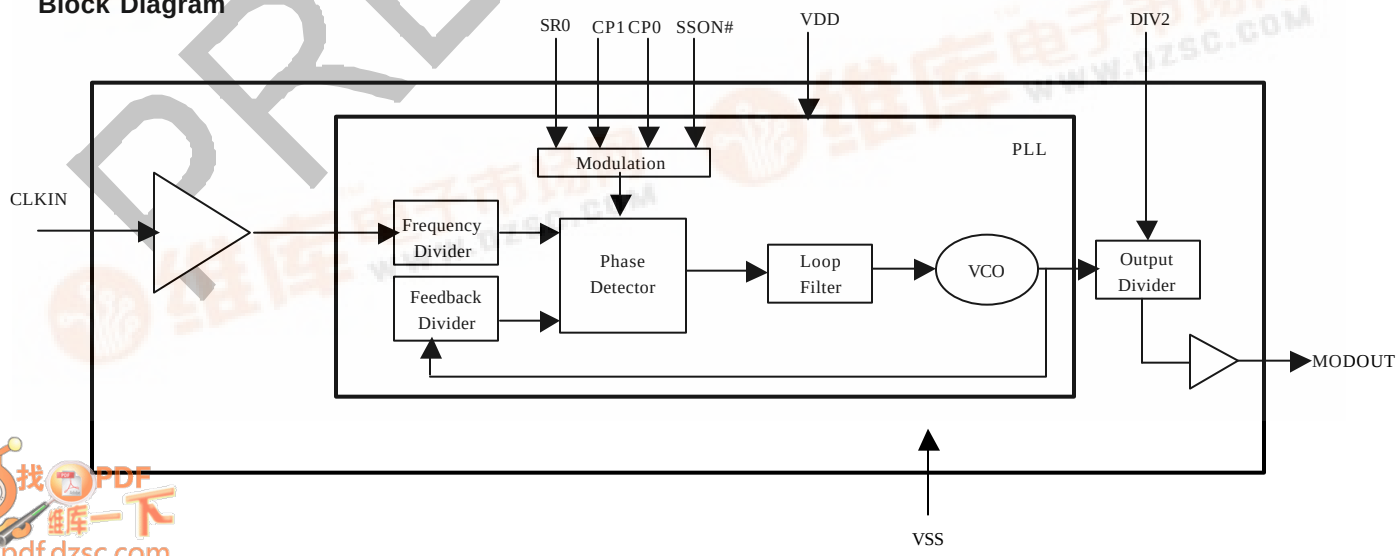
The L2042A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The L2042A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

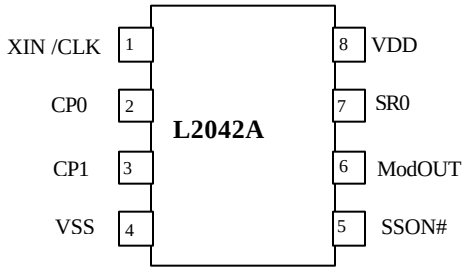
Applications

The L2042A is targeted towards digital flat panel applications for Notebook PCs, Palm-size PCs, office automation equipment, and LCD monitors.

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLK IN	I	External reference frequency input. Connect to an externally generated reference signal.
2	CP0	I	Digital logic input used to select charge pump current. *Refer Modulation Selection Table.* This pin has an internal pull-up resistor.
3	CP1	I	Digital logic input used to select charge pump current. *Refer Modulation Selection Table.* This pin has an internal pull-up resistor.
4	VSS	P	Ground to entire chip. Connect to system ground.
6	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull-low resistor.
7	ModOUT	O	Spread spectrum clock output.
5	SR0	I	Digital logic input used to select Spreading Range *Refer Modulation Selection Table*. This pin has an internal pull-up resistor.
8	VDD	P	Power supply for the entire chip (+2.5V or 3.3V)

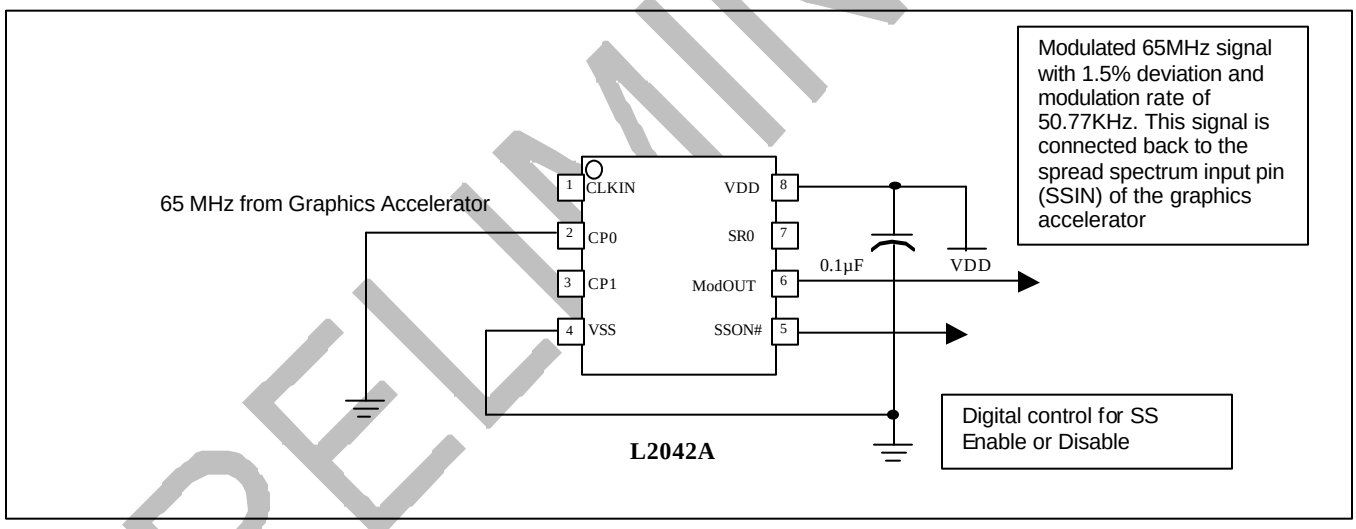
Modulation Selection Table

CP0	CP1	SR0	Spreading Range (± %)				Modulation Rate
			32.5MHz	54MHz	65MHz	70MHz	
0	0	0	0.49	0.92	0.88	0.87	(F_{IN}/40) * 62.49 KHz
0	0	1	1.71	1.48	1.37	1.32	
0	1	0	1.2	0.92	0.88	0.84	
0	1	1	1.69	1.48	1.37	1.33	
1	0	0	1.09	0.71	0.58	0.42	
1	0	1	1.68	1.14	0.9	0.73	
1	1	0	0.8	0.4	0.3	0.25	
1	1	1	1.29	0.62	0.48	0.37	

Spread Spectrum

The *Modulation Selection Table* illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: The center frequency is the frequency of the external reference input on CLKIN, Pin1).

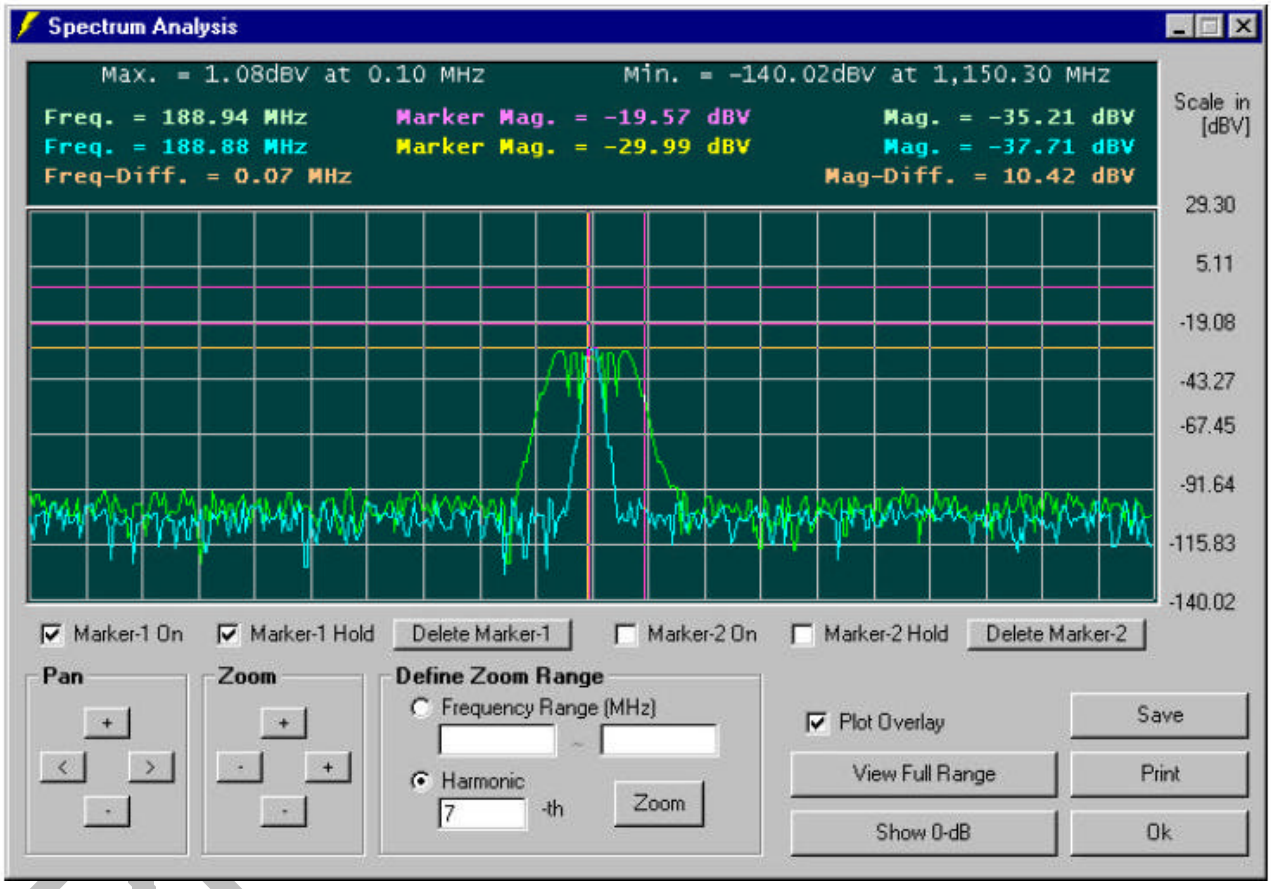
Example:
The L2042A is designed for high-resolution flat panel applications and is able to support panel frequencies from 30 to 75 MHz. For a 65MHz pixel clock frequency, a spreading selection of CP0=0 and CP1=1 and SR0=1 gives a percentage deviation of TBD%. *Refer Modulation Selection Table.* This results in frequency on ModOUT being swept from TBD to TBD MHz. This particular example (See figure below) given here is a common EMI reduction method for notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.



EMC Software Simulation

By using Alliance's proprietary EMC simulation software – EMI-Lator®, radiated system level EMI analysis can be made easier, allowing quantitative measure on the benefits of Alliance's EMI reduction products. The simulation engine of this EMC software has already been characterized to correlate with the electrical characteristics of Alliance EMI reduction ICs. The figure below is an illustration of this simulation result.

Please visit our website at www.alsc.com for information on how to obtain a free copy and demonstration of EMI-Lator ®.



Simulation results From EMI-Lator®

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to + 7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to 70	°C
Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.			

DC Electrical Characteristics

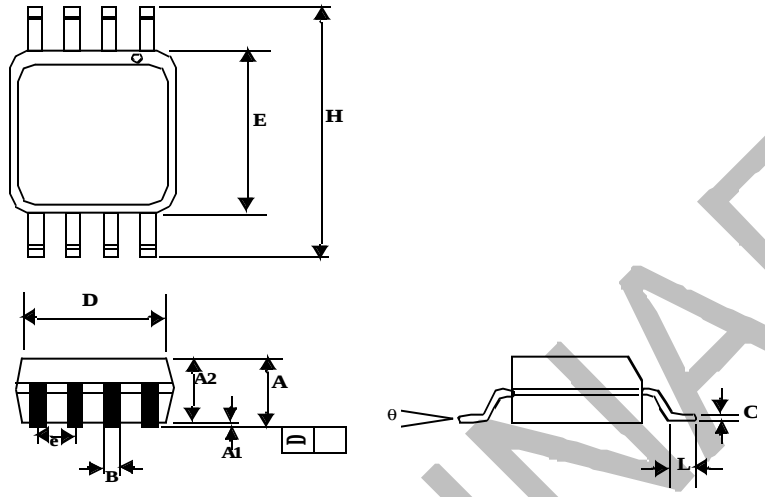
Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND – 0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	V_{DD} + 0.3	V
I_{IL}	Input low current (pull-up resistors on inputs SR0, SR1, CP0 and CP1)	-	-	-35	µA
I_{IH}	Input high current (pull-down resistor on input SSON#)	-	-	35	µA
V_{OL}	Output low voltage (V_{DD} = 3.3V, I_{OL} = 20mA)	-	-	0.4	V
V_{OH}	Output high voltage (V_{DD} = 3.3V, I_{OH} = 20mA)	2.5	-	-	V
I_{CC}	Dynamic supply current normal mode (2.5V, and 15pF loading)	TBD @ 30MHz	-	TBD @70MHz	mA
I_{DD}	Static supply current standby mode	-	0.6	-	mA
V_{DD}	Operating voltage	2.25	2.85	3.7	V
t_{ON}	Power up time (first locked clock cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock output impedance	-	50	-	

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency	30	-	75	MHz
f_{OUT}	Output frequency	30	-	75	MHz
t_{LH}*	Output rise time (measured at 0.8V to 2.0V)	0.7	0.9	1.1	ns
t_{HL}*	Output fall time (measured at 2.0V to 0.8V)	0.6	0.8	1.0	ns
t_{JC}	Jitter (cycle to cycle)	-	-	360	ps
t_D	Output duty cycle	40	50	55	%
*t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

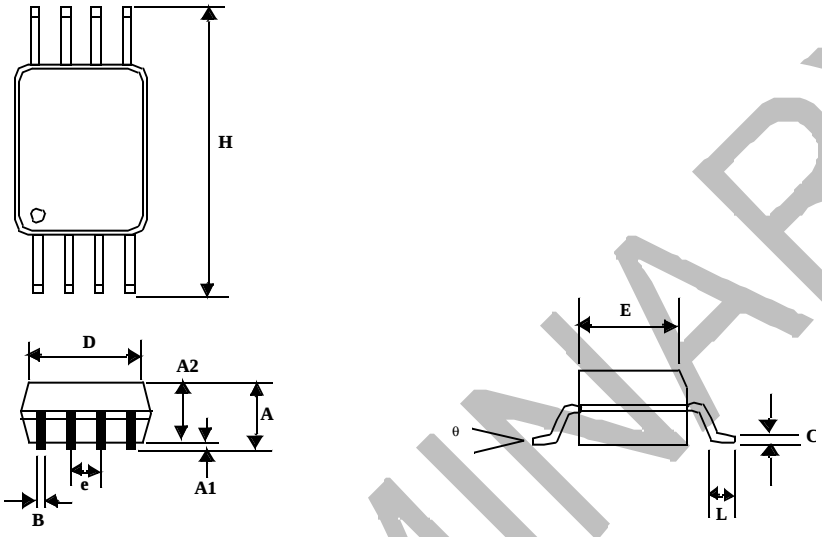
Package Information

8-Pin SOIC



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.057	0.071	1.45	1.80
A1	0.004	0.010	0.10	0.25
A2	0.053	0.069	1.35	1.75
B	0.012	0.020	0.31	0.51
C	0.004	0.01	0.10	0.25
D	0.186	0.202	4.72	5.12
E	0.148	0.164	3.75	4.15
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.70	6.30
L	0.012	0.028	0.30	0.70
è	0°	8°	0°	8°

8-Pin TSSOP



	Dimensions in inches		Dimensions in millimeters	
Symbol	**Min**	**Max**	**Min**	**Max**
A	0.047			1.10
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.244	0.260	6.20	6.60
L	0.018	0.030	0.45	0.75
è	0°	8°	0°	8°

rev 1.0

Ordering Codes

Part Number	Marking	Package type	Qty/reel	Temperature
L2042A-08ST	L2042A	8 PIN SOIC, TUBE		0°C To 70°C
L2042A-08SR	L2042A	8-PIN SOIC, TAPE AND REEL	2,500	0°C To 70°C
L2042A-08TT	L2042A	8-PIN TSSOP, TUBE		0°C To 70°C
L2042A-08TR	L2042A	8-PIN TSSOP, TAPE AND REEL	2,500	0°C To 70°C

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Preliminary Information
Part Number: L2042A
Document Version: v1.0