



# L4903

## DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

PRELIMINARY DATA

- OUTPUT CURRENTS :  $I_{O1} = 50\text{mA}$   
 $I_{O2} = 100\text{mA}$
- FIXED PRECISION OUTPUT VOLTAGE  
 $5\text{V} \pm 2\%$
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN  $1\mu\text{A}$  AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

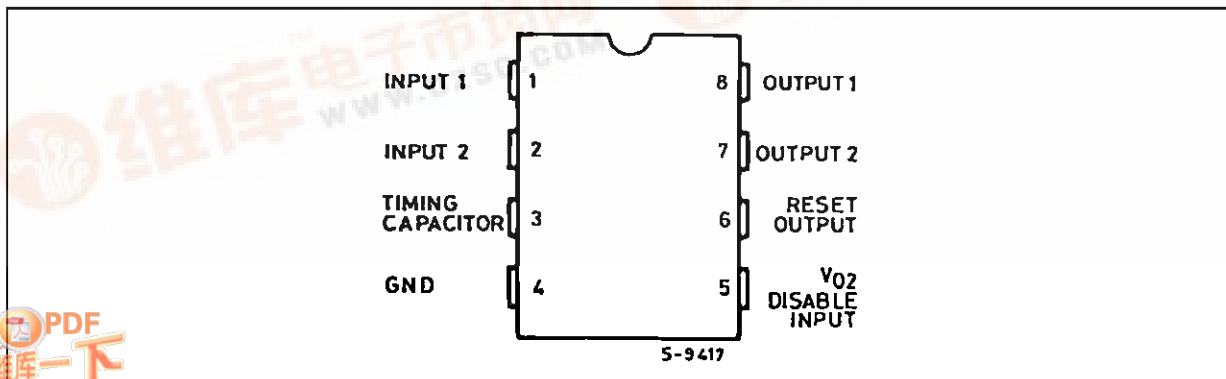


### DESCRIPTION

The L4903 is a monolithic low drop dual 5 V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.

### PIN CONNECTION

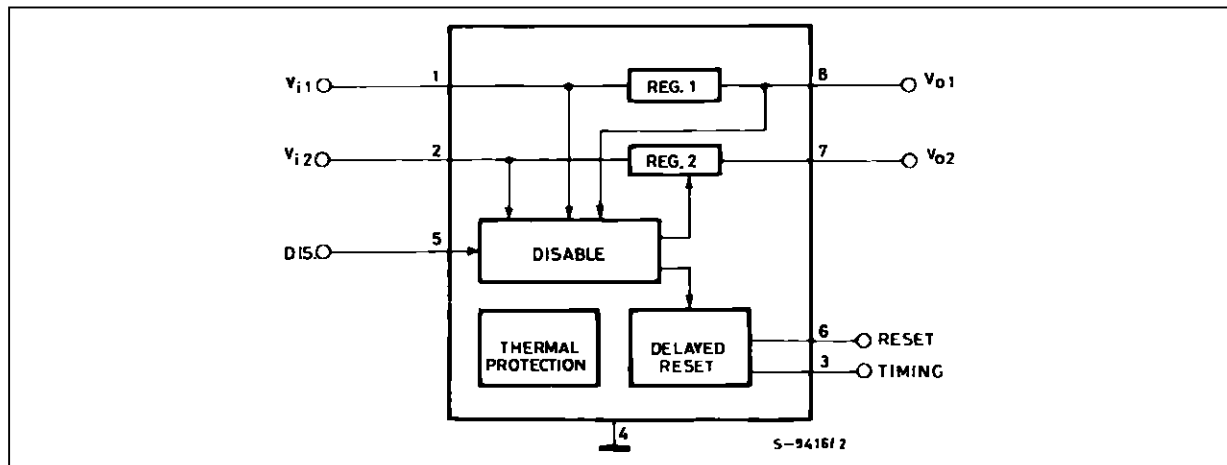


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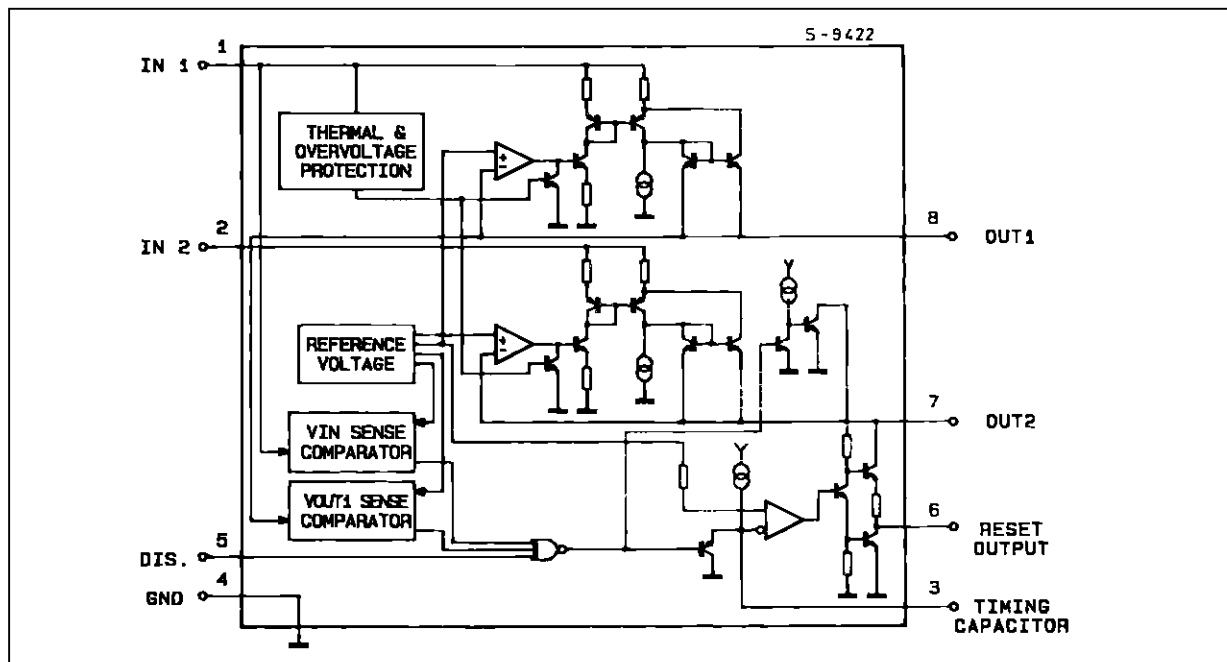
## PIN FUNCTIONS

N°	Name	Function
1	Input 1	Low Quiescent Current 50mA Regulator Input
2	Input 2	100mA Regulator Input.
3	Timing Capacitor	If Reg. 2 is switched-ON the delay capacitor is charged with a 10µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common Ground
5	Disable Input	A high level (> V <sub>DT</sub> ) disables output Reg. 2.
6	Reset Output	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$ ; $t_{RD} \text{ (ms)} = C_t \text{ (nF)}$ .
7	Output 2	5V – 100mA Regulator Output. Enabled if $V_o 1 > V_{RT}$ . DISABLE INPUT < V <sub>DT</sub> and V <sub>IN2</sub> > V <sub>IT</sub> . If Reg. 2 is switched-OFF the C <sub>O2</sub> capacitor is discharged.
8	Output 1	5V – 50mA regulator output with low leakage in switch-OFF condition.

## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{IN}$	DC Input Voltage	24	V
$V_t$	Transient Input Overvoltage (t = 40ms)	60	V
$P_{tot}$	Power Dissipation at $T_{amb} = 50^\circ\text{C}$	1	W
$T_{stg}, T_j$	Storage and Junction Temperature	- 40 to 150	$^\circ\text{C}$

**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{th(j-pin)}$	Thermal Resistance Junction-pin 4	Max. 70	$^\circ\text{C/W}$
$R_{th(j-a)}$	Thermal Resistance Junction-ambient	Max. 100	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 14.4\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_i$	DC Operating Input Voltage				20	V
$V_{O1}$	Output Voltage 1	R Load 1k $\Omega$	4.95	5.05	5.15	V
$V_{O2H}$	Output Voltage 2 HIGH	R Load 1k $\Omega$	$V_{O1} - 0.1$	5	$V_{O1}$	V
$V_{O2L}$	Output Voltage 2 LOW	$I_{O2} = -5\text{mA}$		0.1		V
$I_{O1}$	Output Current 1 max. (*)	$\Delta V_{O1} = -100\text{mV}$	50			mA
$I_{LO1}$	Leakage Output 1 Current	$V_{IN} = 0, V_{O1} \leq 3\text{V}$			1	$\mu\text{A}$
$I_{O2}$	Output Current 2 max. (*)	$\Delta V_{O2} = -100\text{mV}$	100			mA
$V_{IO1}$	Output 1 Dropout Voltage (*)	$I_{O1} = 10\text{mA}$ $I_{O1} = 50\text{mA}$		0.7 0.75	0.8 0.9	V V
$V_{IT}$	Input Threshold Voltage		$V_{O1} + 1.2$	6.4	$V_{O1} + 1.7$	V
$V_{ITH}$	Input Threshold Voltage Hyst.			250		mV
$\Delta V_{O1}$	Line Regulation 1	$7\text{V} < V_{IN} < 18\text{V}, I_{O1} = 5\text{mA}$		5	50	mV
$\Delta V_{O2}$	Line Regulation 2	$7\text{V} < V_{IN} < 18\text{V}, I_{O2} = 5\text{mA}$		5	50	mV
$\Delta V_{O1}$	Load Regulation 1	$V_{IN1} = 8\text{V}, 5\text{mA} < I_{O1} < 50\text{mA}$		5	20	mV
$\Delta V_{O2}$	Load Regulation 2	$V_{IN1} = 8\text{V}, 5\text{mA} < I_{O2} < 100\text{mA}$		10	50	mV
$I_Q$	Quiescent Current	$I_{O1} = I_{O2} \leq 5\text{mA}$ $0 < V_{IN} < 13\text{V}$ $7\text{V} < V_{IN} < 13\text{V} V_{O2} \text{ LOW}$ $7\text{V} < V_{IN} < 13\text{V} V_{O2} \text{ HIGH}$		4.5 2.7 1.6	6.5 4.5 3.5	mA
$I_{Q1}$	Quiescent Current 1	$6.3\text{V} < V_{IN1} < 13\text{V}, V_{IN2} = 0$ $I_{O1} \leq 5\text{mA}, I_{O2} = 0$		0.6	0.9	mA
$V_{RT}$	Reset Threshold Voltage		$V_{O2} - 0.04$	4.7	$V_{O2} - 0.02$	V
$V_{RTH}$	Reset Threshold Hysteresis		30	50	80	mV
$V_{RH}$	Reset Output Voltage HIGH	$I_R = 500\mu\text{A}$	$V_{O2} - 1$	4.12	$V_{O2}$	V
$V_{RL}$	Reset Output Voltage LOW	$I_R = -5\text{mA}$		0.25	0.4	V
$t_{RD}$	Reset Pulse Delay	$C_t = 10\text{nF}$	3	5	11	ms
$t_d$	Timing Capacitor Discharge Time	$C_t = 10\text{nF}$			20	$\mu\text{s}$
$V_{DT}$	$V_{O2}$ Disable Threshold Voltage			1.25	2.4	V
$I_D$	$V_{O2}$ Disable Input Current	$V_D \leq 0.4\text{V}$ $V_D \geq 2.4\text{V}$		-150 30		$\mu\text{A}$ $\mu\text{A}$
$\frac{\Delta V_{O1}}{\Delta T}, \frac{\Delta V_{O2}}{\Delta T}$	Thermal Drift	$-20^\circ\text{C} \leq T_{amb} \leq 125^\circ\text{C}$		0.3 -0.8		mV/ $^\circ\text{C}$
SVR1	Supply Voltage Rejection	f = 100Hz, $V_R = 0.5\text{V}, I_o = 50\text{mA}$	50	84		dB
SVR2	Supply Voltage Rejection	f = 100Hz, $V_R = 0.5\text{V}, I_o = 100\text{mA}$	50	80		dB
$T_{JSD}$	Thermal Shut Down			150		$^\circ\text{C}$

\* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25 mV under constant output current condition.

## L4903

### TEST CIRCUIT

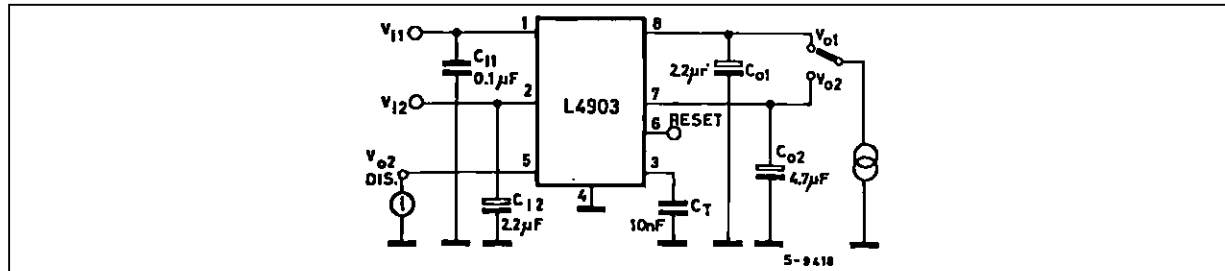
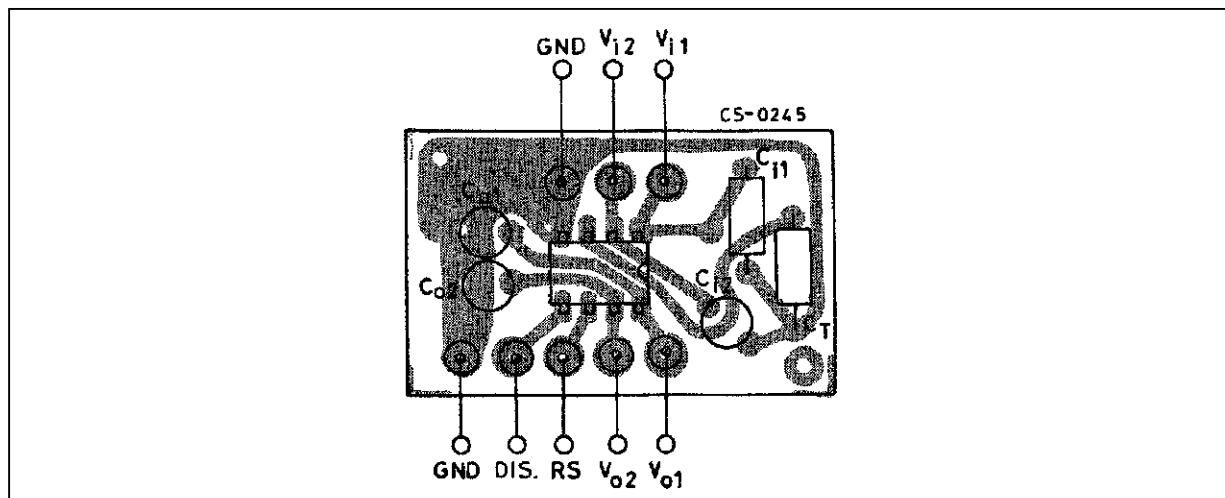


Figure 1 : P.C. Board and Components Layout of the Test Circuit



### APPLICATION INFORMATION

In power supplies for  $\mu$ P systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments ; it provides two voltage regulators (both 5 V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

### CIRCUIT OPERATION (see Figure 2)

After switch on Reg. 1 saturates until  $V_{01}$  rises to the nominal value.

When the input 2 reaches  $V_{IT}$  and the output 1 is higher than  $V_{RT}$  the output 2 ( $V_{02}$  and  $V_R$ ) switches on and the reset output ( $V_R$ ) goes low after a programmable time  $T_{RD}$  (timing capacitor).

$V_{02}$  is switched at low level and  $V_R$  at high level when one of the following conditions occurs ;

- a high level ( $> V_{DT}$ ) is applied on pin 5 ;
- an input overvoltage ;
- an overload on the output 1 ( $V_{01} < V_{RT}$ ) ;
- a switch off ( $V_{IN} < V_{IT} - V_{ITH}$ ) ;

and they start again as before when the condition

is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The  $V_{01}$  output features :

- 5 V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power conditions.

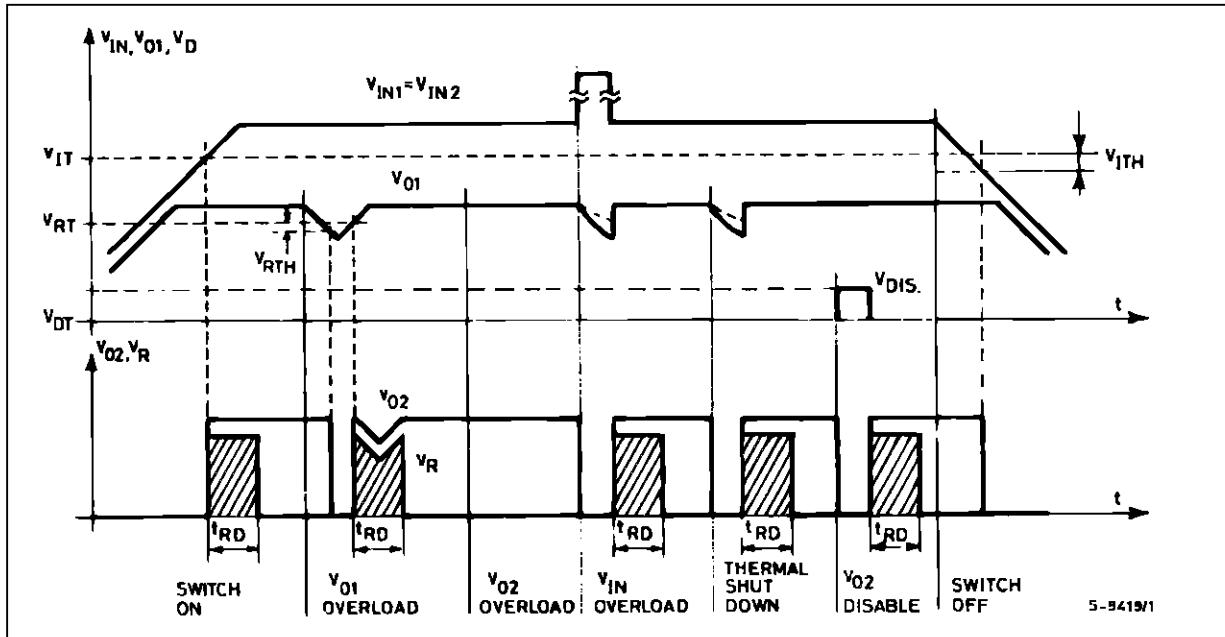
This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

The  $V_{02}$  can supply other non essential 5 V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the  $V_{02}$  output.

Figure 2



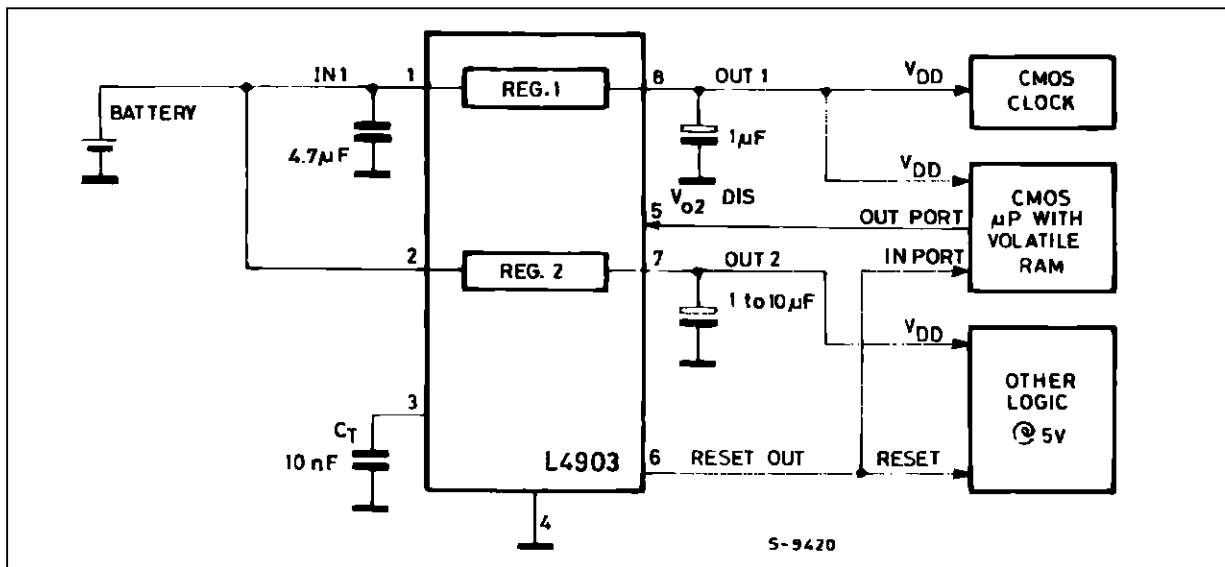
**APPLICATION SUGGESTION**

Figure 3 illustrates how the L4903's disable input may be used in a CMOS  $\mu$ Computer application. The  $V_{01}$  regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS computer chip with volatile memory.  $V_{02}$  output,

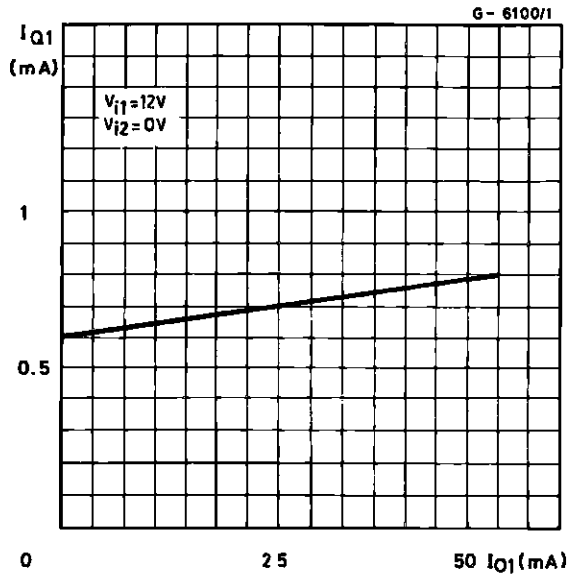
supplying non-essential circuits, is turned OFF under control of a  $\mu$ P unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

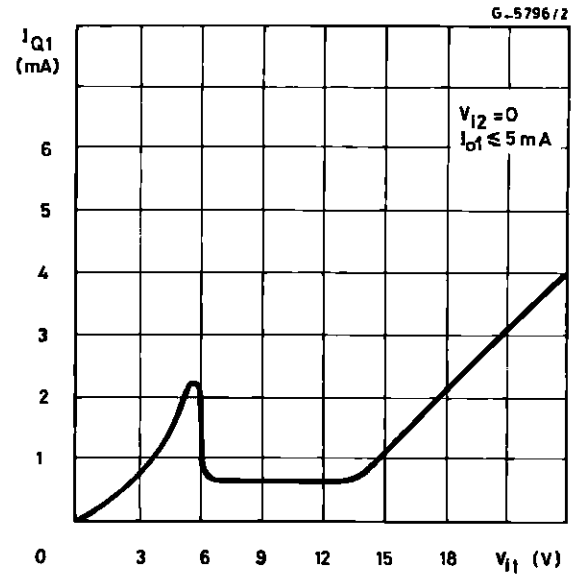
Figure 3



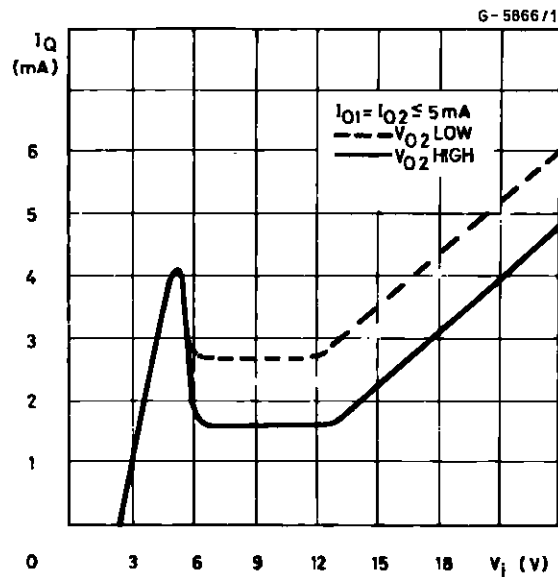
**Figure 4 :** Quiescent Current (reg. 1) versus Output Current



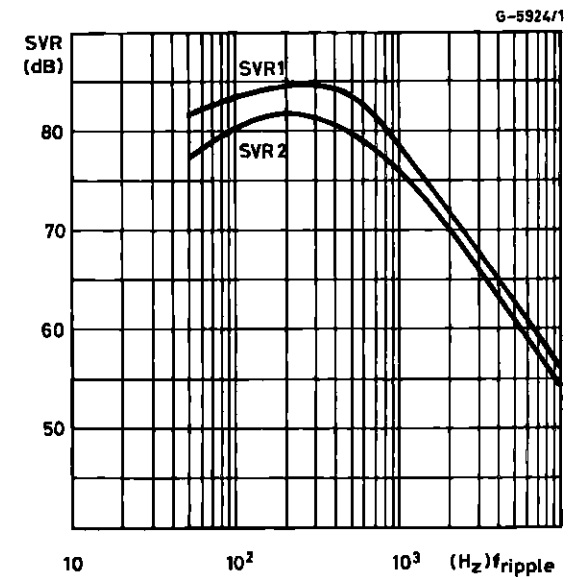
**Figure 5 :** Quiescent Current (reg. 1) versus Input Voltage



**Figure 6 :** Total Quiescent Current versus Input Voltage

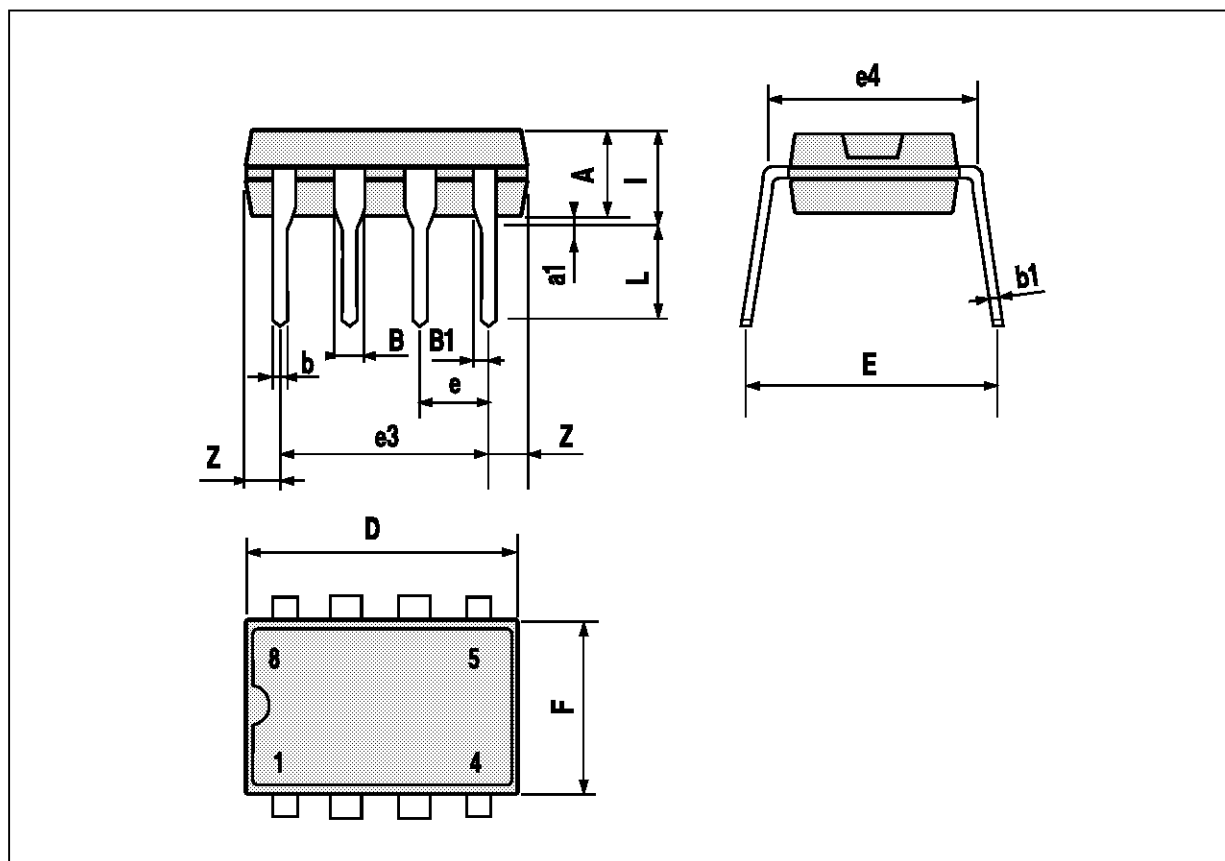


**Figure 7 :** Supply Voltage Rejection Regulators 1 and 2 versus Input Ripple Frequency



## MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



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