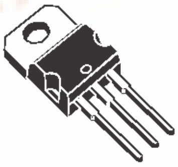
L4945

5V VERY LOW DROP VOLTAGE REGULATOR

- 5V ± 4% PRECISE OUTPUT VOLTAGE OVER FULL TEMPERATURE RANGE (– 40 / 125 °C)
- VERY LOW VOLTAGE DROP (0.75Vmax) OVER FULL TEMPERATURE RANGE
- OUTPUT CURRENT UP TO 500mA
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTIONS
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



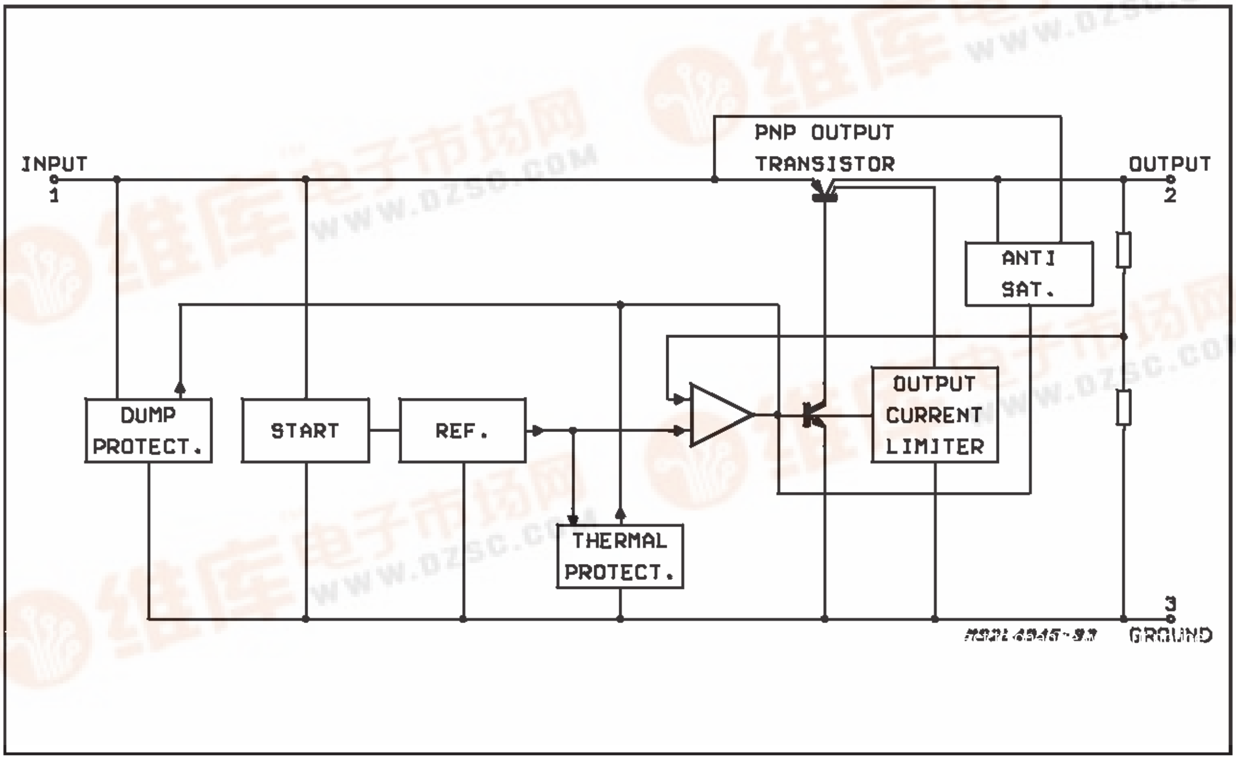
TO220

ORDERING NUMBER: L4945

DESCRIPTION

The L4945 is a monolithic integrated circuit in Versawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to their very low voltage drop, in automotive applications the devices can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, they incorporate a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car.

BLOCK DIAGRAM

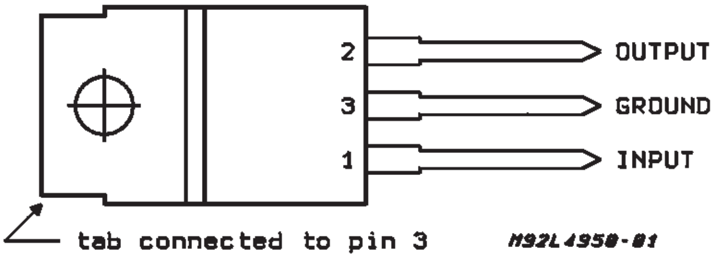


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	V
	DC Reverse Input Voltage	– 18	V
	Transient Input Overvoltages :	80	V
	Load Dump :		
	$5ms \leq t_{rise} \leq 10ms$		
	τ_f Fall Time Constant = 100ms		
	$R_{SOURCE} \geq 0.5\Omega$	– 80	V
	Field Decay :		
	$5ms \leq t_{fall} \leq 10ms$, $R_{SOURCE} \geq 10\Omega$		
	τ_r Rise Time Constant = 33ms	± 100	V
	Low Energy Spike :		
	$t_{rise} = 1\mu s$, $t_{fall} = 500\mu s$, $R_{SOURCE} \geq 10\Omega$		
	f_r Repetition Frequency = 5Hz		
T_J	Junction Temperature Range	– 40 to 150	°C
T_{OP}	Operating Temperature Range	– 40 to 125	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

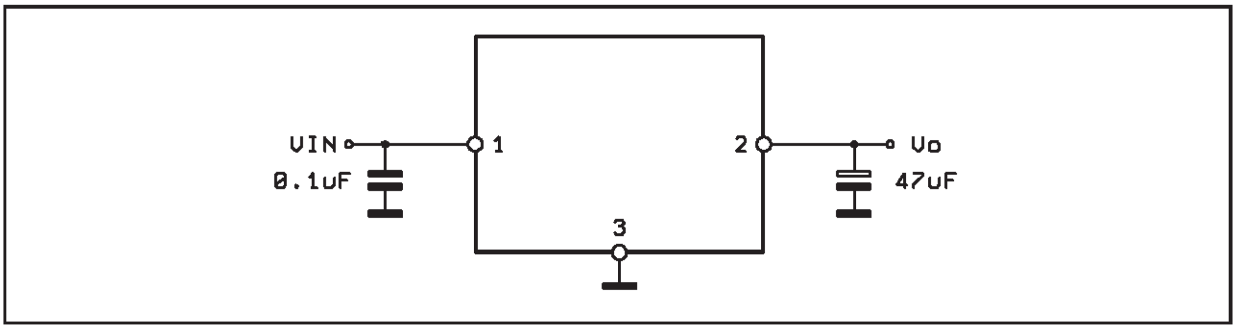
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14. 4V, C_o = 47µF, ESR < 10Ω, R_p = 1KΩ, R_L = 1KΩ, –40°C ≤ T_J ≤ 125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 0mA to 500mA Over Full T Range	4.80	5.00	5.20	V
		T_j = 25°C	4.90	5.00	5.10	V
V_i	Operating Input Voltage	I_o = 0mA to (*) 500mA	6		26	V
ΔV_o	Line Regulation	V_i = 6V to 26V ; I_o = 5mA		2	10	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA		15	60	mV
$V_i - V_o$	Dropout Voltage	I_o = 500mA, T_J = 25°C Over Full T Range		0.40	0.55 0.75	V V
I_q	Quiescent Current	I_o = 0mA, T_J = 25°C I_o = 0mA Over Full T I_o = 500mA Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; V_i = 12V ± 5V_{pp}	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A

(*) For a DC voltage 26 < V_i < 37V the device is not operating

FUNCTIONAL DESCRIPTION

The block diagram shows the basic structure of the devices : the reference, the error amplifier, the driver, the power PNP, the protection and reset functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at T_J = 25°C, max. 750mV over the full temperature range @ I_O = 500mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500mA.

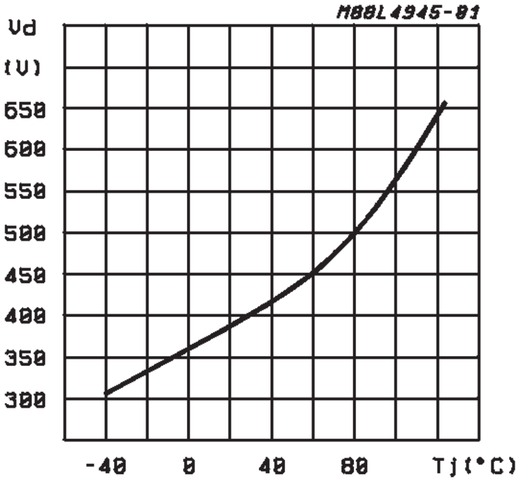
The current consumption of the devices (quiescent current) are maximum 10mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{omin} = 20µF) to guarantee the global stability of the system.

Load dump and field decay protections (± 80V, t = 300ms), reverse voltage (– 18V) and short circuit protection, thermal shutdown are the main features that make the devices specially suitable for applications in the automotive enviroment.

Figure 1: Typical Dropout Voltage vs. T_j (I_o = 500mA).



EXTERNAL COMPENSATION

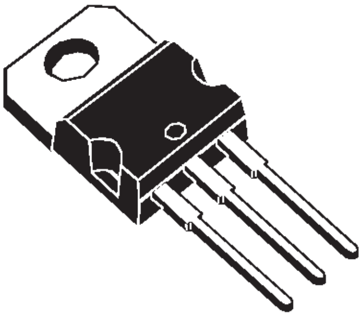
Since the purpose of a voltage regulator is to supply and load variations, the open loop gain of the regulators must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shift due to other poles at the unity gain frequency. The lower the frequency of these others poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be capacitor esed to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequencybtoo low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

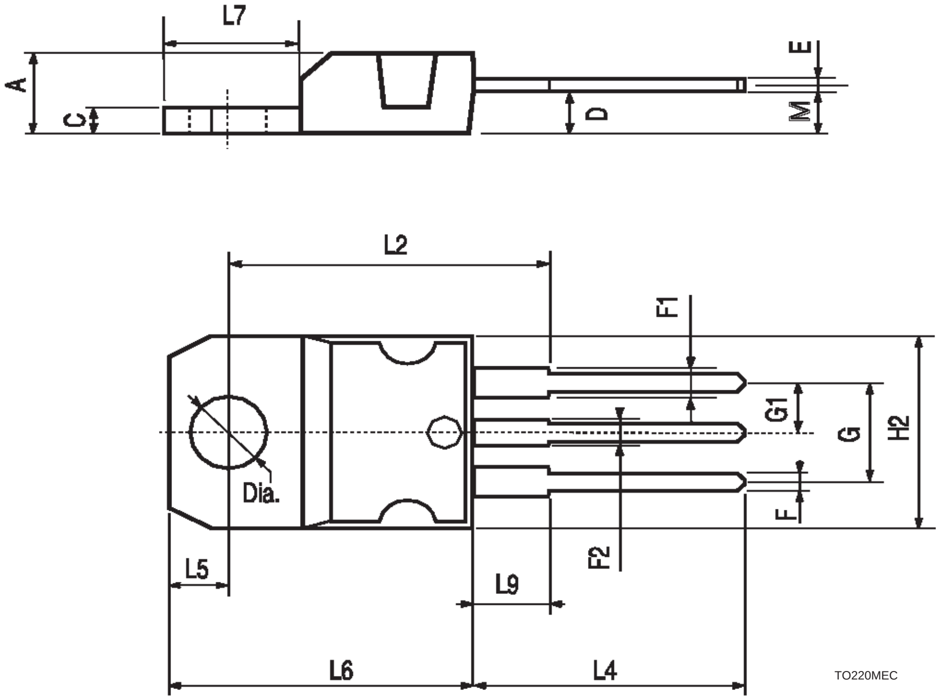
The paeassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

OUTLINE AND MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10.0		10.4	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
M		2.6			0.102	
Dia	3.75		3.85	0.147		0.151



Versawatt (TO220)



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