



## L6275

### 5V DISK DRIVE SPINDLE & VCM, POWER & CONTROL "COMBO"

#### PRODUCT PREVIEW

#### GENERAL

- 5V (+/- 10%) OPERATION.
- REGISTER BASED ARCHITECTURE
- MINIMUM EXTERNAL COMPONENTS
- BICMOS + VERTICAL DMOS (1.5mm)

#### VCM DRIVER

- 1.5A DRIVE CAPABILITY
- 0.9Ω TOTAL BRIDGE IMPEDANCE AT 25°C
- LINEAR MODE
- PHASE SHIFT MODULATION (PWM MODE)
- INSTANTANEOUS, (GLITCH FREE) SWITCH BETWEEN THE 2 MODES
- CLASS AB OUTPUT DRIVERS
- ZERO CROSSOVER DISTORTION
- 14 BIT DAC DEFINE OUTPUT CURRENT
- SELECTABLE TRANSCONDUCTANCE
- 4 PROGRAMMABLE PARKING VOLTAGE
- DYNAMIC BRAKE

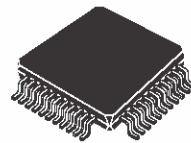
#### SPINDLE DRIVER

- 2.0A DRIVE CAPABILITY
- 0.8Ω TOTAL BRIDGE IMPEDANCE AT 25°C
- BEMF, INTERNAL OR EXTERNAL, PROCESSING
- SENSOR-LESS MOTOR COMMUTATION
- PROGRAMMABLE COMMUTATION PHASE DELAY
- LINEAR MODE AND CONSTANT TOFF PWM OPERATION MODE
- INTERNAL FREQUENCY LOCKED LOOP SPEED CONTROL (FLL)
- BEMF RECTIFICATION DURING RETRACT
- BUILT-IN ALIGNMENT&GO START-UP
- INDUCTIVE SENSING START UP OPTION
- RESYNCHRONIZATION
- DYNAMIC & REVERSE BRAKE
- CONTROLLABLE OUTPUT SLEW RATE

#### OTHER FUNCTIONS

- 5V MONITORING WITH EXTERNAL SET TRIP POINTS AND HYSTERESIS
- POWER UP/DOWN SEQUENCING
- LOW VOLTAGE SENSE

#### BICMOS TECHNOLOGY



TQFP44 (10x10mm)

ORDERING NUMBER: L6275

- 3.3V INPUT LOGIC COMPATIBILITY
- THERMAL SHUTDOWN AND PRETHERMAL WARNING
- SYSTEM CLOCK WATCHDOG

#### DESCRIPTION

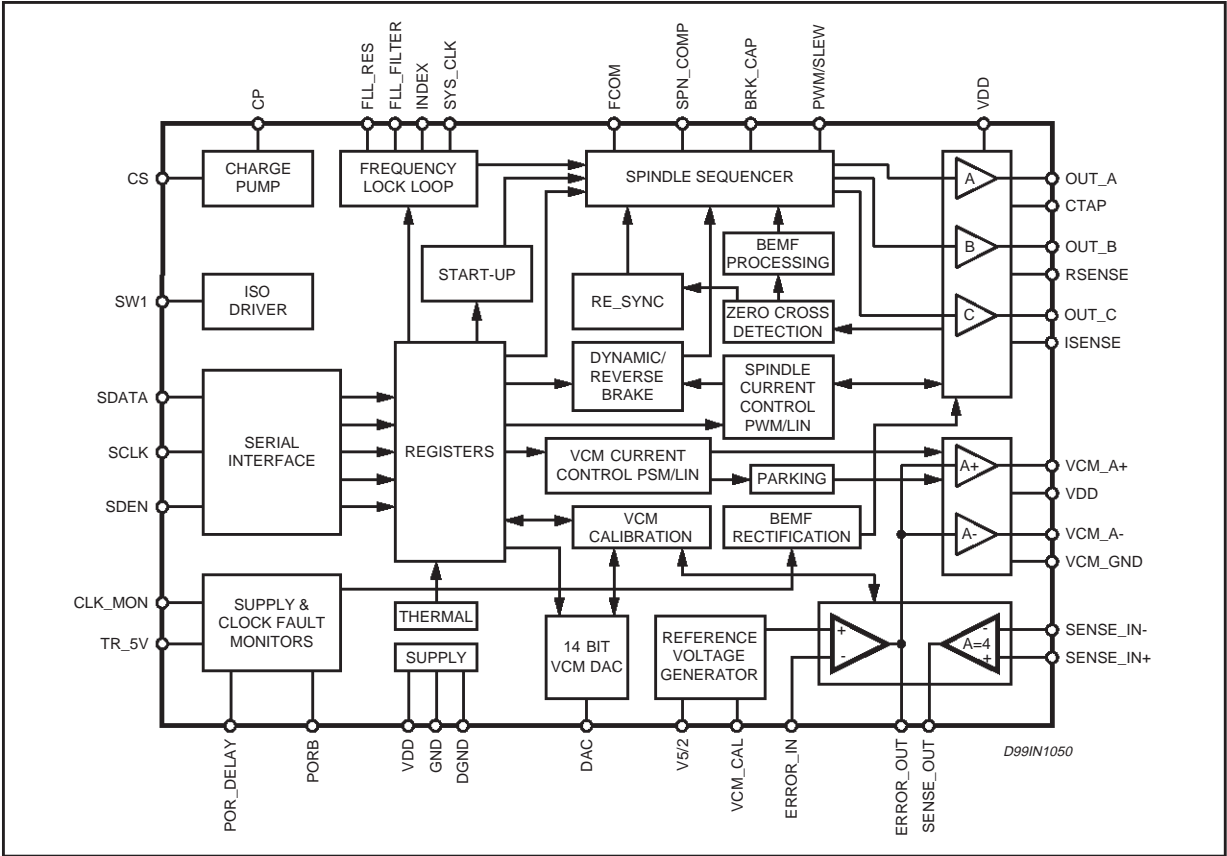
The L6275 integrates into a single chip both spindle and VCM controllers as well as power stages. The device is designed for 12V disk drive application requiring up to 2.0A of spindle and 1.5A of VCM peak currents.

A serial port with up to 25 MHz capability provides easy interface to the microprocessor. A register controlled Frequency Locked Loop (FLL) allows flexibility in setting the spindle speed. Integrated BEMF processing, digital masking, digital delay, and sequencing minimize the number of external components required.

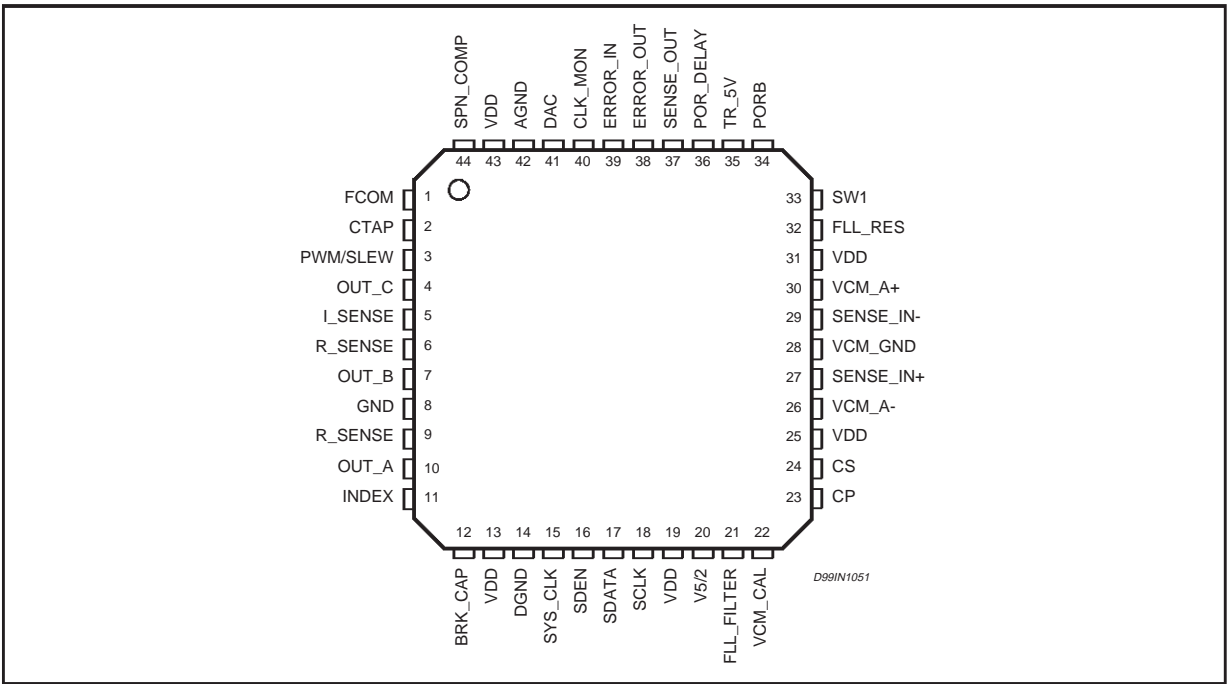
Power On Reset (POR) circuitry is included. Upon detection of a low voltage condition, POR is asserted, the internal registers are reset, and spindle power circuitry is tri-stated. The BEMF is rectified providing power for actuator retraction followed by dynamic spindle braking.

The device is built in BICMOS technology allowing dense digital/analog circuitry to be combined with a high power DMOS output stage.

BLOCK DIAGRAM



PIN CONNECTION



**PIN DESCRIPTION** (Pin Types: D = Digital, P = Power, A = Analog)

N.	Name	Function
1	FCOM	Output of the Spindle zero cross or Current Sense circuit.
2	CTAP	Spindle Central Tap used for differential BEMF sensing.
3	PWM/SLEW	RC network sets the Spindle Linear Slew Rate and PWM OFF-Time.
4	OUT_C	Spindle DMOS Half Bridge Output and Input C for BEMF sensing.
5	I_SENSE	Input to sense the voltage the SPINDLE Sense Resistor.
6	R_SENSE	Output connection for the Motor Current Sense Resistor to ground.
7	OUT_B	Spindle DMOS Half Bridge Output and Input B for BEMF sensing.
8	GND	Spindle Ground (Substrate).
9	R_SENSE	Output connection for the Motor Current Sense Resistor to ground.
10	OUT_A	Spindle DMOS Half Bridge Output and Input A for BEMF sensing.
11	INDEX	Input to allow Spindle to be locked to Index (servo) pulse.
12	BRK_CAP	Storage Capacitor for brake circuit. typically 5.9V.
13	VDD	+5V Power Supply for Spindle Power section.
14	DGND	Digital Ground.
15	SYS_CLK	Clock Frequency for system timers and counters.
16	SDEN	Serial Data Enable. Active high input pin for the serial port enable.
17	SDATA	Serial Port Data. Input/Output pin for serial data, 8bits of instruction/address followed by 8 bits of data. Open pin is at logic low as an input.
18	SCLK	Serial Port Data Clock. Positive edge triggered clock input for the serial data.
19	VDD	Digital/Analog power supply. +5V nominally.
20	V12/2	Reference Output for VCM control loop. Typically, half of the VCC except when parking.
21	FLL_FILTER	Speed loop R/C compensation connection used for FLL mode operation.
22	VCM_CAL	VCM loop offset voltage used for calibration.
23	CP	External Main Charge Pump Capacitor, Typically, Vz+Vcc is about 17.8V
24	CS	External Charge Pump Capacitor.
25	VDD	+5V Power Supply for VCM Power section.
26	VCM_A-	VCM Power Amplifier negative output terminal.
27	SENSE_IN+	Non inverting Input of the Sense Amplifier for VCM block.
28	VCM_GND	Ground for VCM Power section.
29	SENSE_IN-	Inverting Input of the Sense Amplifier for VCM block.
30	VCM_A+	VCM Power Amplifier positive output terminal.
31	VDD	+5V Power Supply for VCM Power section.
32	FLL_RES	Resistor for setting accurate bias current sources for the chip (62K required).
33	SW1	External ISOFET driver.
34	PORB	Power on Reset Output. Low signal indicates the failure of the supplies.
35	TR_5V	Set Point Input for 5V Supply Monitor ( 2V threshold, 100mV Hysteresis)
36	POR_DELAY	Capacitor connection to set the Power on Reset Delay (3V threshold, 2μA charging)
37	SENSE_OUT	Output of the Sense Amplifier.
38	ERROR_OUT	Output of the Error Amplifier.
39	ERROR_IN	Inverting Input of the Error Amplifier.
40	CLK_MON	Watchdog clock monitoring pin
41	DAC	Output of the VCM DAC.
42	AGND	Analog Ground. For bang gap voltage reference.
43	VCC	+12V Power Supply for Spindle Power section.
44	SPN_COMP	External RC network that defines the compensation of the Spindle Transconductance Loop in Linear Mode.

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Maximum Supply voltage	-0.5 to 14	V
$V_{dd}$	Maximum Logic supply	-0.5 to 6	V
$V_{in\ max}$	Maximum digital input voltage	$V_{dd} + 0.3V$	V
$V_{in\ min}$	Minimum digital input voltage	GND - 0.3V	V
SPINDLE $I_{peak}$	Spindle peak sink/source output current	2.1	A
VCM $I_{peak}$	VCM peak sink/source output current	1.6	A
$P_{tot}$ (*)	Maximum Total Power Dissipation	$\approx 1.7$	W
$T_{stg}, T_j$	Maximum Storage/Junction Temperature	-40 to 150	°C

**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal Resistance Junction to Case	$\approx 20$	°C/W
$R_{th\ j-amb}$ (*)	Thermal Resistance to Junction to ambient	$\approx 40$	°C/W

(\*) In typical application with multilayer 120X120mm Printed Circuit Board

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{dd}$	Supply Voltage	4.5 to 5.5	V
$T_{amb}$	Operating Ambient Temperature	0 to 70	°C
$T_j$	Junction Temperature	0 to 125	°C

**ELECTRICAL CHARACTERISTICS** (All specifications are for  $0 < T_{amb} < 70^{\circ}C$ ,  $V_{CC} = 12V$ ;  $V_{DD} = 5V$ ,  $FLL\_RES = 62k\Omega$ , unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
V <sub>rectified</sub>	V <sub>CC</sub> Supply Rectified		3.5		13.2	V
V <sub>dd</sub>	5V supply		4.5		5.5	V
I <sub>Vdd</sub>	5V supply	SPINDLE + VCM		6		mA
		SPINDLE ONLY		7		mA
		VCM ONLY		12		mA
THERMAL SENSING						
T <sub>SD</sub>	Shutdown Temperature		150		180	°C
T <sub>HYS</sub>	Hysteresis			60		°C
T <sub>EW</sub>	Early Warning			T <sub>SD</sub> -25		°C

## ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>SUPPLY MONITOR</b>						
$V_{TR}$	Trip Point	Input Rising	1.92	2	2.08	V
$V_{HYS}$	Hysteresis Voltage	Input falling		100		mV
$I_{DLY}$	Porb Delay Current	$TR_{5V}, TR_{12V} > V_{TR}$ $V_{pordly} = 2V$	1.5	2	2.5	$\mu A$
$R_{on\_por}$	Porb Pull Down Ron	$V_{dd} > 2V$ and sink 1mA $V_{pordly} = 2V$			500	$\Omega$
$V_{DLY}$	Porb Dly Threshold	$TR_{5V} > V_{TR}$		2.0		V
$I_{IN}$	Input Current	$V_{IN} < 4V$	-1		1	$\mu A$
<b>VOLTAGE BOOST</b>						
$V_{BOOST}$	Output Voltage		$V_{dd}+5$		$V_{dd}+6.3$	V
$F_{OSC}$	Internal Oscillator		130	200	250	kHz
<b>SYSTEM CLOCK WATCHDOG</b>						
Min_Clk	Min. System Clock Time		7	10	13	$\mu s$
<b>SW1 OUTPUT</b>						
$R_{GATE}$	Gate Driver for External Mosfet	Internal Resistor to CP		200		k $\Omega$
$V_{GATE}$	Off Gate State Voltage for External Mosfet	$I_O = 1mA$ $V_{dd} = 3.5V$			0.7	V
<b>DIGITAL LOGIC LEVELS</b>						
$V_{IH}$	Input Logic "1"		2.5			V
$V_{IL}$	Input Logic "0"				0.5	V
$V_{OH}$	Output Logic "1"	$I_{SOURCE} = 20\mu A$	$V_{dd}-0.2$			V
$V_{OL}$	Output Logic "0"	$I_{SOURCE} = -400\mu A$			0.4	V
$F_{SYSCLK}$	System Clock			20	25	MHz
<b>VCM, DAC</b>						
	Resolution			14		Bits
	Differential Linearity	1 LSB Change - Tested - By design	-1 -0.5		1 0.5	LSB
	Integral Linearity		9			Bits
	Midscale Offset	Referenced to $V_{CC}/2$	-5		5	mV
$T_C$	Conversion Time				5	$\mu s$
	Full Scale Voltage	Referenced to $V_{CC}/2$		$\pm 1$		V
	Full Scale Error		-4		4	%
<b>VCM, ERROR AMPLIFIER</b>						
$A_{VOL}$	Open Loop Gain	DC	50			db
$V_{OS}$	Input Offset Voltage		-5		5	mV
$I_{IB}$	Input Bias Current		--250		250	nA
$V_{ICM}$	Input Common Mode Range		$V_{CC}/2-0.5$		$V_{CC}/2+0.5$	V

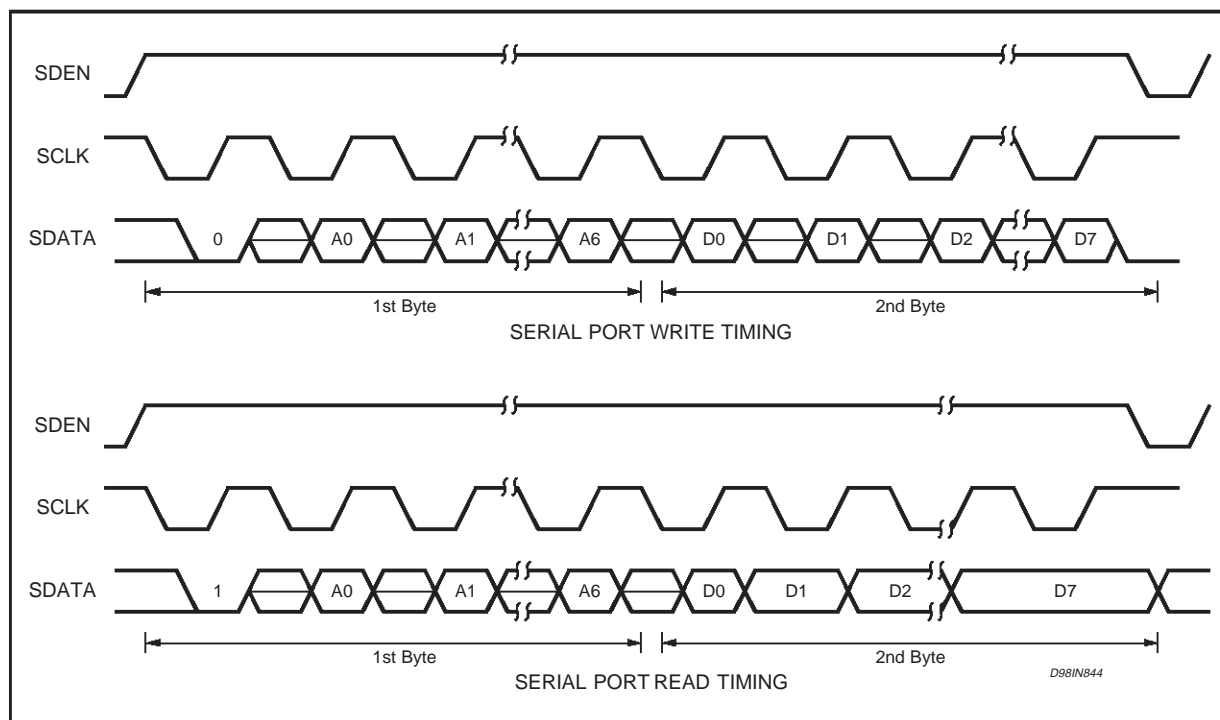
## ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>clamp</sub>	Output Clamp Voltage	-1mA < I <sub>O</sub> < 1mA Lowside/Highside clamp		V <sub>dd</sub> /2± 1.4V		V
F <sub>ODB</sub>	Unity Gain Bandwidth			10		MHz
<b>VCM, POWER STAGE</b>						
R <sub>DS(ON)</sub>	Output ON Resistance (Each device)	T <sub>j</sub> = 25°C T <sub>j</sub> = 125°C			0.5 0.8	Ω Ω
I <sub>O</sub>	Operating Current				1.3	A
I <sub>O(LEAK)</sub>	Output Leakage Current	V <sub>CC</sub> = 5.5V			1.0	mA
<b>VCM, CURRENT SENSE AMPLIFIER</b>						
A <sub>V</sub>	Voltage Gain		3.88	4	4.12	V/V
V <sub>ICM</sub>	Input Common Mode Range		-0.3		V <sub>dd</sub> +0.3	V
V <sub>OCM</sub>	Output Common Mode Range	-3mA < I <sub>O</sub> < 3mA	2		V <sub>dd</sub> -2	V
V <sub>OS</sub>	Output Offset Voltage	SENSE_IN (±) = V <sub>dd</sub> /2	-15		15	mV
F <sub>3dB</sub>	3dB Bandwidth			1		MHz
CMRR	Input Common Mode Rejection		50			dB
PSRR	Power Supply Rejection Ratio		60			dB
<b>VCM, RETRACT</b>						
V <sub>park</sub>	RETRACT VOLTAGE	PKV_1 = 0 & PKV_2 = 0 PKV_1 = 0 & PKV_2 = 1 PKV_1 = 1 & PKV_2 = 0 PKV_1 = 1 & PKV_2 = 1		0.850 0.650 1.600 1.150		mV mV mV mV
T <sub>retract</sub>	Retract Time limited by the internal oscillator 200kHz	RT0 = 0 & RT1 = 0 RT0 = 0 & RT1 = 1 RT0 = 1 & RT1 = 0 RT0 = 1 & RT1 = 1		160 320 80 160		ms ms ms ms
<b>SPINDLE, PWM CURRENT SENSE COMPARATOR</b>						
T <sub>DLY</sub>	Delay to FCOM Out			200	500	ns
<b>SPINDLE, POWER STAGE</b>						
R <sub>DS(ON)</sub>	Output On Resistance (Each device)	T <sub>j</sub> = 25°C T <sub>j</sub> = 125°C			0.45 0.74	Ω Ω
I <sub>O</sub>	Start-Up Current				2	A
I <sub>O(LEAK)</sub>	Output Leakage Current	V <sub>CC</sub> = 14V			1.0	mA
dV <sub>O</sub> /d <sub>t</sub>	Output Slew Rate (Linear)	R <sub>slew</sub> = 100kΩ	0.2	0.3	0.5	V/μs
	Output Slew Rate (PWM)	Reg#8Eh, Bit 0 = 0 Reg#8Eh, Bit 0 = 1		10 20		V/μs V/μs
BEMF <sub>MIN</sub>	Minimum BENF Voltage for Detection		20	28	40	mVp-p
V <sub>HYS</sub>	Hysteresis			15		mV
<b>FLL CHARGE PUMP OUTPUT</b>						
I <sub>LEAK</sub>	Off State Leakage	0 < V <sub>fil_res</sub> , 3V	-50		+50	nA
I <sub>O</sub>	On State Current	FLL_RES = 62kΩ ICP = "1"	22	25	32	μA
		ICP = "0"	80	100	120	μA
V <sub>RCP</sub>	Current Set Voltage	FLL_RES = 62kΩ	1.18	1.225	1.25	V

## ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIER						
I <sub>BIAS</sub>	Input Bias Current				2	μA
A <sub>v</sub>	Voltage Gain		3.8	4.0	4.2	V/V
dV <sub>o</sub> /d <sub>t</sub>	Output Slew Rate			20		V/μs
SERIAL PORT						
Symbol	Parameter	Min.	Typ.	Max.	Unit	
T <sub>SCK</sub>	SCLK Period	40			ns	
T <sub>CKL</sub>	SCLK low time	15			ns	
T <sub>CKH</sub>	SCLK high time	15			ns	
T <sub>SDENS</sub>	Enable to SCLK	35			ns	
T <sub>SDENH</sub>	SCLK to disable	20			ns	
T <sub>DS</sub>	Data set-up time before rising edge SCLK	10			ns	
T <sub>DH</sub>	Data Hold Time	10			ns	
T <sub>SDENL</sub>	Minimum SDEN Low Time	50			ns	
T <sub>SDV</sub>	SCLK falling edge (A6) to SDATA valid on READ op.	3		10	ns	
T <sub>SDV</sub>	SCLK rising edge (D0-D7) to SDATA Transition on READ op.	5		35	ns	

Figure 1. Serial Port Timing Information.

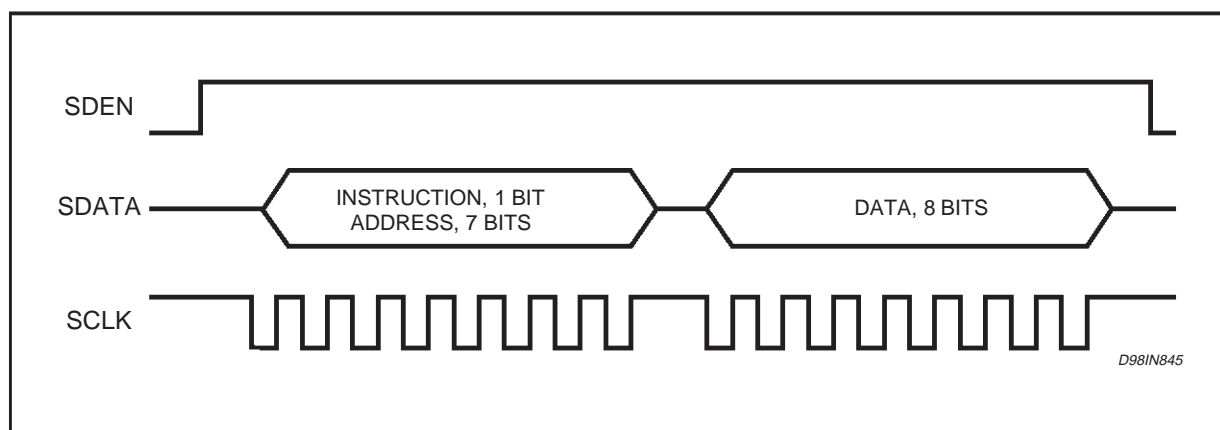


## SERIAL PORT OPERATION

The serial port interface is a bi-directional port for reading and writing programming data from/to the internal registers of this device. For data transfers SDEN\* is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN\* goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched after the 16th SCLK pulse. If less than 16 clock pulses are provided before SDEN\* goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is for R/W and address and instruction information. The first bit is R/W instruction bit, 0 is for WRITE and 1 is for READ. Following 7 bits are Address.

**Figure 2. Serial Port Data Transfer Format.**



## INTERNAL REGISTER DEFINITION

Reg: 0  
 Name: VCM DAC (High) Register  
 Type: Write only  
 Address: 0Eh

BIT	LABEL	DESCRIPTION
0	VDAC BIT8	VCM DAC bit 8
1	VDAC BIT9	VCM DAC bit 9
2	VDAC BIT10	VCM DAC bit 10
3	VDAC BIT11	VCM DAC bit 11
4	VDAC BIT12	VCM DAC bit 12
5	VDAC BIT13	MSB resistor ladder of the 14 bit VCM DAC
6	PSM/LINEAR	Selects Voice Coil PSM or Linear Output Current Control. 1=PSM 0=Linear.
7	VCM_CAL	VCM calibration. 1 = Enables VCM control circuits and tristates VCM power transistors.



**INTERNAL REGISTER DEFINITION****VCM DAC (High and Low) Registers**

Bit 0 through 5 of the VCM DAC (High) Registers and bit 0 through 7 of the VCM DAC (Low) Registers control the absolute value of the voice coil current. Bit is the sign bit, controlling the current direction. All the 13 bits are part of a resistor divider network.

Note. It is required to write on register 1 to make effective changes on register 0.

<b>Reg:</b>	<b>1</b>
<b>Name:</b>	<b>VCM DAC (Low) Registers</b>
<b>Type:</b>	<b>Write only</b>
<b>Address:</b>	<b>1Eh</b>

BIT	LABEL	DESCRIPTION
0	VDAC BIT0	LSB resistor ladder of the 14 bit VCM DAC
1	VDAC BIT1	VCM DAC bit 1
2	VDAC BIT2	VCM DAC bit2
3	VDAC BIT3	VCM DAC bit3
4	VDAC BIT4	VCM DAC bit4
5	VDAC BIT5	VCM DAC bit5
6	VDAC BIT6	VCM DAC bit6
7	VDAC BIT7	VCM DAC bit7

<b>Reg:</b>	<b>2</b>
<b>Name:</b>	<b>Spindle Control Register</b>
<b>Type:</b>	<b>Write only</b>
<b>Address:</b>	<b>2Eh</b>

BIT	LABEL	DESCRIPTION
0	INCRE_SEQ	A 0 to 1 transition of this bit increments the spindle Sequencer.
1	START_UP	1 = Spindle Internal start up, 0 = Spindle External start up
2	R_SEQ	Reset Spindle sequencer. 1 = Reset sequencer to phase 1.
3	RUN	1 = Start Spindle ALIGN & GO, 0 = Reset Spindle control logic.
4	SPIN_EN	Enable Spindle section. 1 = Enable, 0 = Disable.
5	MEC/ELEC	Specifies electrical or mechanical cycle for Spindle FLL control. 1=Electrical, 0 = Mechanical.
6	PWM/LINEAR	Selects Spindle PWM or Linear Output Current Control. 1 = PWM, 0=Linear.
7	EXT/INT	External or internal Spindle loop feedback. 1 = external feedback via index pin.

## INTERNAL REGISTER DEFINITION

**Reg:** 3  
**Name:** Spindle Delay Register  
**Type:** Write only  
**Address:** 3Eh

BIT	LABEL	DESCRIPTION			
0	MASK_TIME	Spindle BEMF Mask Time. 0 = 15 degree, 1 = 7.5 degree			
1	MIN2	Control Spindle PWM on time	Min 1	Min2	Min. on Time
			0	0	5.9μs
2	MIN1		0	1	1.4μs
			1	0	12μs
			1	1	5.21μs
3	8_12_POLE	Selects 8 or 12 pole motors. 1 = 8 pole, 0 = 12 pole.			
4	SD3	Spindle commutation delay MSB			
5	SD2	Spindle commutation delay bit			
6	SD1	Spindle commutation delay bit			
7	SD0	Spindle commutation delay LSB			

## SPINDLE PHASE DELAY

SD3-0 set the phase delay from BEMF zero crossing to the next commutation. The 30 theoretical degree value can be changed to compensate for switching and other delays that are always present. The delay adjustment range is from 1.875 through to 30 electrical degrees in 1.875 degree increments.

**Reg:** 4  
**Name:** FLL Coarse Counter Register  
**Type:** Write only  
**Address:** 4Eh

BIT	LABEL	DESCRIPTION
0	C4	Bit 4 of Spindle FLL Coarse Counter
1	C5	Bit 5 of Spindle FLL Coarse Counter
2	C6	Bit 6 of Spindle FLL Coarse Counter
3	C7	Bit 7 of Spindle FLL Coarse Counter
4	C8	Bit 8 of Spindle FLL Coarse Counter
5	C9	Bit 9 of Spindle FLL Coarse Counter
6	C10	Bit 10 of Spindle FLL Coarse Counter
7	C11	MSB of Spindle FLL Coarse Counter

## INTERNAL REGISTER DEFINITION

**Reg:** 5  
**Name:** FLL Coarse/Fine Counter Register  
**Type:** Write only  
**Address:** 5Eh

BIT	LABEL	DESCRIPTION
0	F8	Bit 8 of Spindle FLL Fine Counter
1	F9	Bit 9 of Spindle FLL Fine Counter
2	F10	MSB of Spindle FLL Fine Counter
3		Unused. Set = 0
4	C0	LSB of Spindle FLL Coarse Counter
5	C1	Bit 1 of Spindle FLL Coarse Counter
6	C2	Bit 2 of Spindle FLL Coarse Counter
7	C3	Bit 3 of Spindle FLL Coarse Counter

**Reg:** 6  
**Name:** FLL Fine Counter Register  
**Type:** Write only  
**Address:** 6Eh

BIT	LABEL	DESCRIPTION
0	F0	LSB of Spindle FLL Fine Counter
1	F1	Bit 1 of Spindle FLL Fine Counter
2	F2	Bit 2 of Spindle FLL Fine Counter
3	F3	Bit 3 of Spindle FLL Fine Counter
4	F4	Bit 4 of Spindle FLL Fine Counter
5	F5	Bit 5 of Spindle FLL Fine Counter
6	F6	Bit 6 of Spindle FLL Fine Counter
7	F7	Bit 7 of Spindle FLL Fine Counter

## INTERNAL REGISTER DEFINITION

**Reg:** 7  
**Name:** Spindle Status Register  
**Type:** Read only  
**Address:** 7Eh

BIT	LABEL	DESCRIPTION
0	THERMAL	Thermal Shutdown = 0 indicates that the chip temperature has exceeded 160°C. The bit will reset (=1) when the temperature falls below 130°C. When Thermal Shutdown =0, the spindle logic will tristate both high and low side drivers, protecting the output circuitry.
1	THERM_WARN	Thermal Shutdown Warning =0 indicates that the chip temperature is approximately 25°C before the device goes in thermal shut down.
2	ROTOR_STUCK	0 = A sequential Spindle BEMF has not been detected
3	FAULT	1 = Rapid deceleration of the Spindle motor or High frequency on FCOM signal.
4	MASK_TIME	Mask Time toggled to "0" indicates that the Spindle BEMF is masked.
5	ERROR_LOCK	0 = Indicates error Spindle speed > 16msec/sample, either electrical or mechanical.
6	ALIGN	0 indicate that the Spindle is in the Internal Start-Up Align Phase.
7	GO	0 indicate that the Spindle is in the Internal Start-Up Go Phase.

**Reg:** 8  
**Name:** Spindle FLL Register  
**Type:** Write only  
**Address:** 8Eh

BIT	LABEL	DESCRIPTION
0	SSLEW	Spindle PWM (chopping) Slew Rate. 0 = 10V $\mu$ S, 1 = 20V $\mu$ S
1	ICP	Spindle FLL Charge pump current. 1= 25 $\mu$ A, 0 = 100 $\mu$ A.
2		Unused. Set = 0.
3	ISNS	1 = Puts output of the Spindle sense amplifier on FCOM pin and changes limit to roughly 1/3 of normal.
4	IL1	Adjust maximum voltage on Spindle Rsense
5	IL0	Adjust maximum voltage on Spindle Rsense
6	CPL	1 = Spindle FLL Charge pump low
7	CPH	1 = Spindle FLL Charge pump high

"IL0"	"IL1"	"ISNS"	V(I_SENSE) LIMIT ( $\pm 10\%$ )
0	0	0	0.45V
1	0	0	0.50V
0	1	0	0.55V
1	1	0	0.75V
0	0	1	0.15V
1	0	1	0.20V
0	1	1	0.25V
1	1	1	0.30V

## INTERNAL REGISTER DEFINITION

<b>Reg:</b>	<b>9</b>
<b>Name:</b>	<b>System Control Register</b>
<b>Type:</b>	<b>Write only</b>
<b>Address:</b>	<b>9Eh</b>

BIT	LABEL	DESCRIPTION
0	PKV_1	VCM Parking Voltage
1	PKV_2	VCM Parking Voltage
2	VR	1 = connects internal VR reference (2V) to level shift Opamp (for Vcm calibration).
3	RT0 (*)	VCM Retract Time
4	DOUBLE	1 = Spindle Internal Start-Up Align and Energization time doubled.
5	VCM_EN	Enable VCM section. 1 = Enable, 0 = Disable.
6	RT1 (*)	VCM Retract Time
7	RETRACT	1= VCM retract

"PKV_1"	"PKV_2"	"PARKING VOLTAGE"
0	0	0.850V
0	1	0.650V
1	0	1.600V
1	1	1.150V
"RT0"	"RT1"	"RETRACT TIME"
0	0	160ms
0	1	320ms
1	0	80ms
1	1	160ms

(\*) When program Retract Time (RT0 and RT1), Bit 2 REG#8Eh must be always written to 0.

## INTERNAL REGISTER DEFINITION

**Reg:** 10  
**Name:** Test Control Register  
**Type:** Write only  
**Address:** AEh

BIT	LABEL	DESCRIPTION
0		Unused. Set = 0
1		Unused. Set = 0
2		Unused. Set = 0
3		Unused. Set = 0
4	FLL_OUT	1 = Spindle Mech/Elec (see bit 5 register 2) output, 0 = Spindle zero crossing output.
5	REV_BRAKE	Spindle Reverse Brake command. 1 = Brake. "0" has to be reinserted to enable the spindle start up.
6		Unused. Set = 0
7	VB/DIS	1 = Disable Vboost

**Reg:** 11  
**Name:** VCM Control Register  
**Type:** Write only  
**Address:** BEh

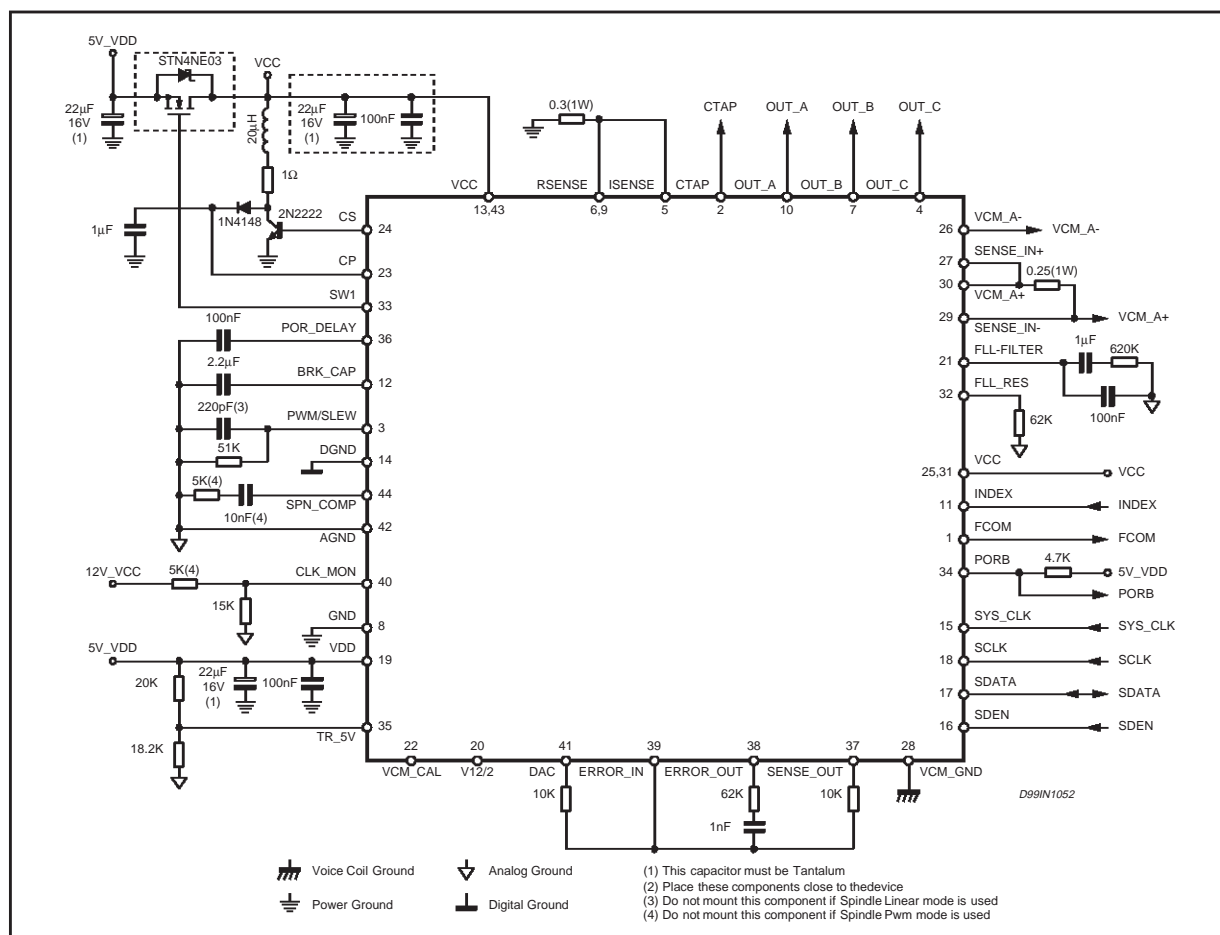
BIT	LABEL	DESCRIPTION
0	VCMS	VCM PSM (chopping) Slew Rate. 0 = 10V/μs, 1 = 20V/μs
1	VCMH	1 = Forces VCM outputs to be High in PSM mode.
2	SLEEP	Unused (for future power saving mode).
3	COMSLEW	Spindle PWM (phase commutation) Slew Rate. 0 = 30Vμs, 1 = 2Vμs.
4		Unused. Set = 0
5		1 = Tristate the VCM outputs for half of the Retract Time during retract.
6		1 = Brakes the VCM outputs for half of the Retract Time during retract.
7		Unused. Set = 0

## INTERNAL REGISTER DEFINITION

**Reg:** 12  
**Name:** Chip ID Register  
**Type:** Read only  
**Address:** FFh

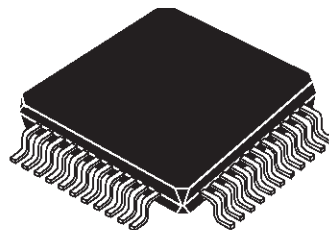
BIT	LABEL	DESCRIPTION
0	ID_REV_0	Minor Revision Bit 0.
1	ID_REV_1	Minor Revision Bit 1.
2	ID_REV_2	Minor Revision Bit 2.
3	ID_REV_3	Minor Revision Bit 3.
4	ID_REV_4	Minor Revision Bit 0.
5	ID_REV_5	Minor Revision Bit 1.
6	ID_REV_6	Minor Revision Bit 2.
7	ID_REV_7	Minor Revision Bit 3.

Figure 3. Application Circuit.

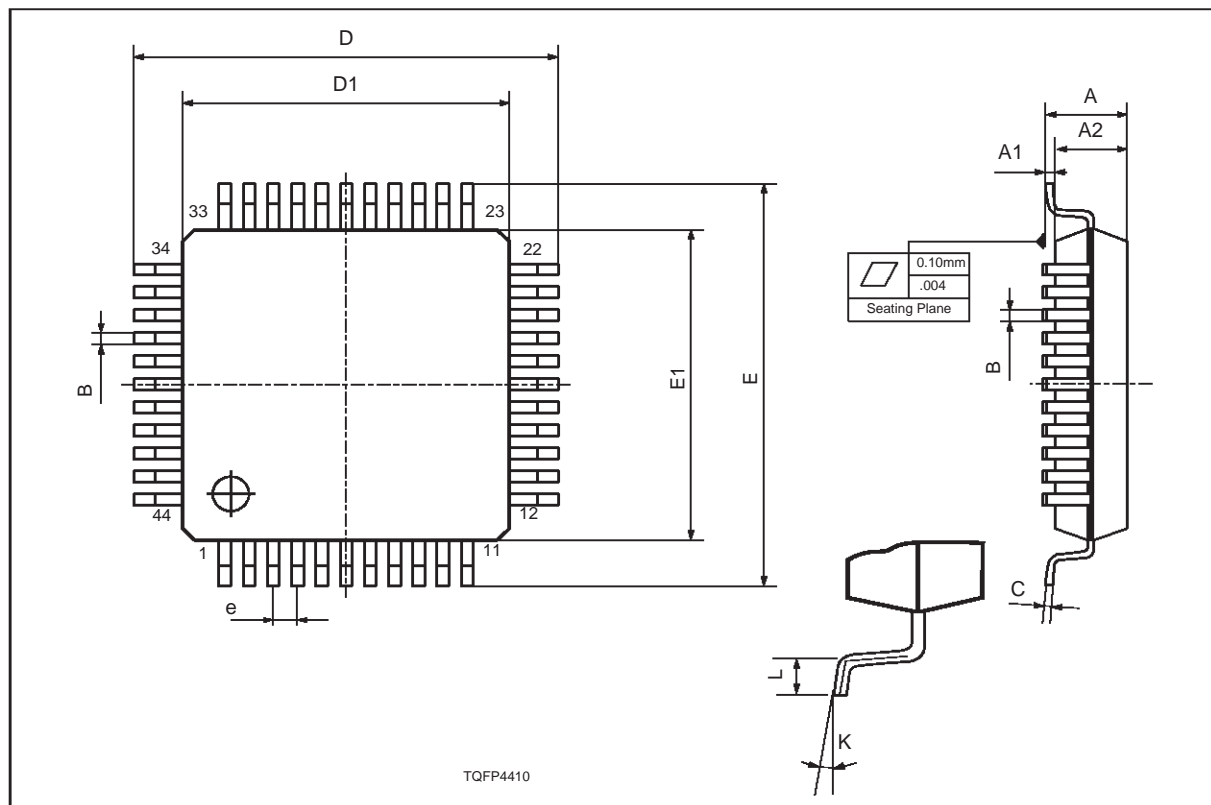


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

## OUTLINE AND MECHANICAL DATA



## TQFP44 (10 x 10)





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