



L6452

DUAL 13X16 MATRIX HEAD INK JET DRIVER

- DRIVES TWO 13X16 MATRIX HEADS
- HEAD TEMPERATURE SENSING
- POWER UP SYSTEM
- ELECTRICAL NOZZLE CHECK
- 8 BIT A/D
- 5 BIT D/A
- ± 4KV ESD PROTECTED OUTPUTS

DESCRIPTION

L6452 is a device designed to drive two 13x16 matrix ink jet printheads in printer applications.

The output stage is able to source simultaneously 400 mA on each of the 16 power lines (columns) with a duty cycle of 33% in normal printing and 66% in head pre-heating. On the address lines (rows), the load is only capacitive (MOS FET driving capability). The driver can control two printheads, but only one is active at a time. The address scanning counter is included and can be disabled to allow a different scanning scheme.

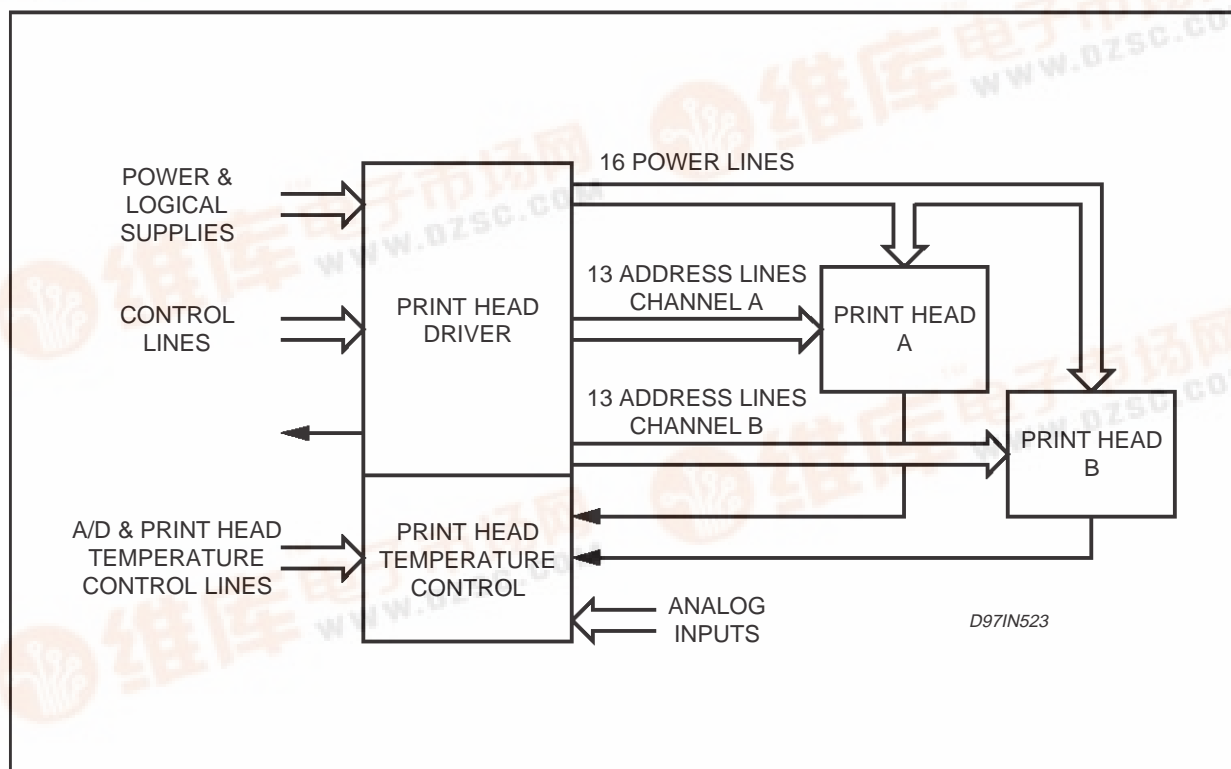


In order to avoid output activation during the supply transient, an internal power-up system is implemented.

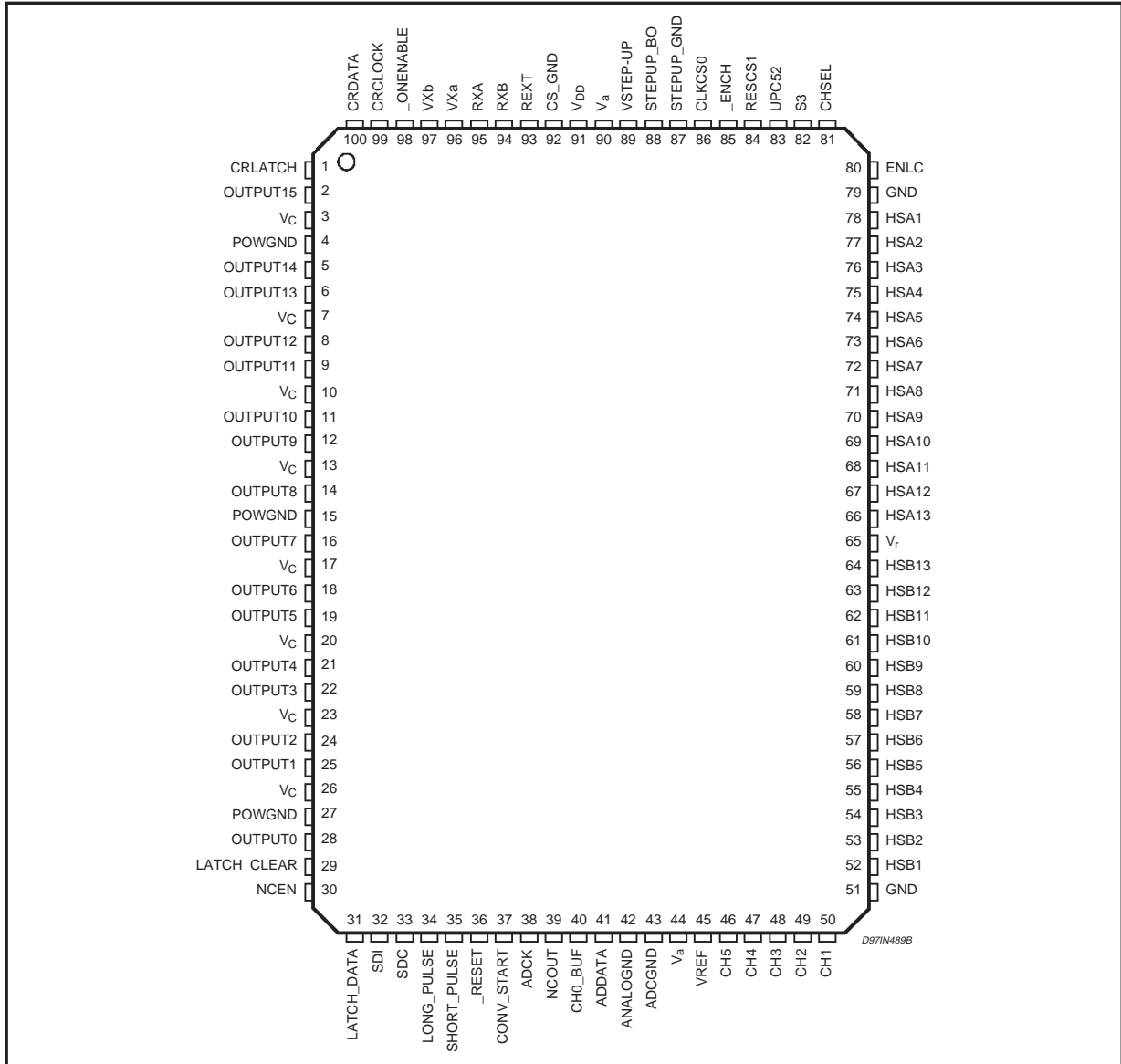
As supporting function, L6452 is capable of sensing the head silicon temperature and to electrically check each nozzle.

The device is also integrating a thermal protection.

Figure 1. Block Diagram



PIN CONNECTION (Top view)



PIN FUNCTIONS

Pin #	Name	Function
1	CRLatch	A rising edge latches the information present into the control register
2, 5, 6, 8, 9, 11, 12, 14, 16, 18, 19, 21, 22, 24, 25, 28	Output 15...0	High side DMOS outputs. To be active, Short Pulse and/or Long Pulse and Nozzle Check Enable must have a low level
3, 7, 10, 13, 17, 20, 23, 26	Vc	Outputs Power Supply
4, 15, 27, 51, 79, 92	GND	logic and power ground
29	Latch Clear	A high level resets all bit in the latch

## PIN FUNCTIONS (continued)

Pin #	Name	Function
30	NCEn	A high level enables the internal current sources and disables all DMOS outputs. To be active, the internal current sources must have their corresponding bit set in the 16 bit latch and Long Pulse must be set to low level. A low level enables the internal HSA/B short circuit detection
31	Latch Data	A rising edge latches the 16 bit stored in the shift register in the 16 bit latch
32	SDI	Serial data input of the shift register
33	SDC	The data bit presented to the Serial Data Input pin is stored into the register on the rising edge of this pin
34	Long Pulse	A low level activates all outputs having their corresponding bit in the 16 bit latch set (this pin has an internal pull-up resistor)
35	Short Pulse	A low level activates all outputs having their corresponding bit in the 16 bit latch reset (this pin has an internal pull-up resistor)
36	_Reset	A low level disables all functions and clears all registers
37	ConvStart	A high level enables the A/D to start the new conversion
38	ADCK	A/D clock signal; the ADDATA signal are valid on the falling edge of this pin
39	NCOut	If Nozzle Check Enable is high this output provides a high level when the open load is detected on the output. If Nozzle Check Enable is low this output provides a high level when a short circuit is detected on HSA/B output
40	CH0_buf	Analog output signal (CH0 buffered)
41	ADDATA	A/D serial data output
42	AnalogGND	Analog ground connection
43	ADCGND	Ground of internal ADC
44, 90	Va	Power supply
45	Vref	Reference voltage generator
46 to 50	CH5..CH1	A/D input signals
52 to 64	HSB1..HSB13	Head selector address output channel B
65	Vr	Head Select Power Supply
66 to 78	HSA13..HSA1	Head selector address output channel A
80	EnIC	A high level enables the counter and the internal decoder will activate of the HSx outputs according to the counter's outputs. Signal S0 becomes Clock Counter and S1 becomes Reset Counter
81	ChSel	A low level enables channel A and a high level enables channel B
82	S3	Decoder input signals when Enable Counter is low
83	UpC/ S2	A high level enables the internal counter to up counting. A low level enables down counting
84	ResC/S1	A low level resets the internal counter
85	_EnCh	A low level enables the selected channel (this input has an internal pull up resistor)
86	ClkC/S0	A high level clocks the internal counter
87	Step up GND	Ground of step up block
88	Step up boost	Boost voltage
89	Vstep up	Driving voltage of power DMOS stage
91	VDD	5V logic supply
93	Rext	An external resistor connected versus ground fixes the internal current source value
94, 95	RxB, RxA	Current source outputs
96, 97	VxA, VxB	RxA, RxB voltage after an optional external filter
98	_ONenable	A low level enables the current source generator according the _A/B and ON/_OFF control register bit
99	CRclock	Data on pin CRdata are stored into the register on the rising edge of this pin
100	CRdata	Control register serial data input

Figure 2. Block Diagram: Nozzle activation part.

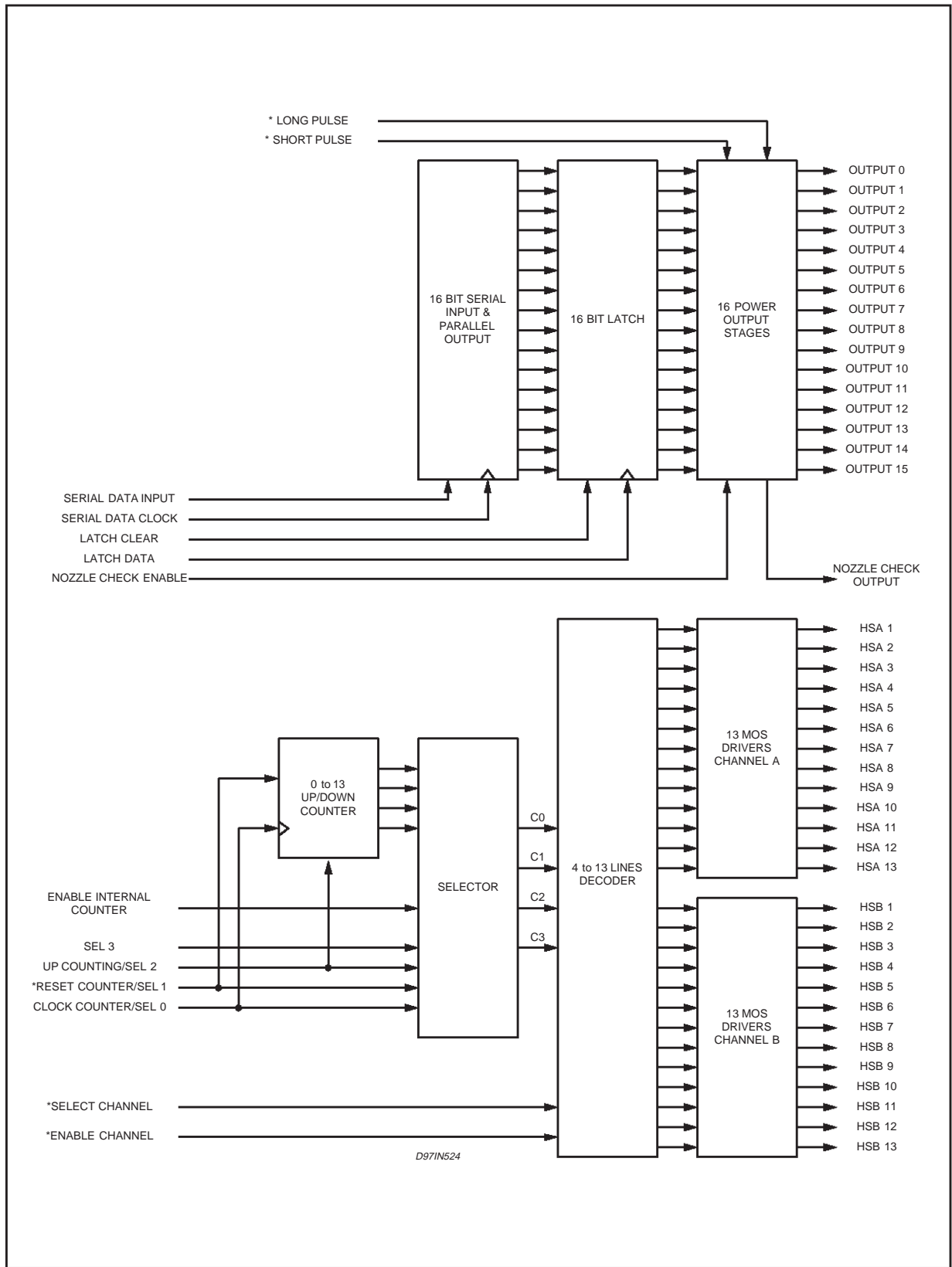
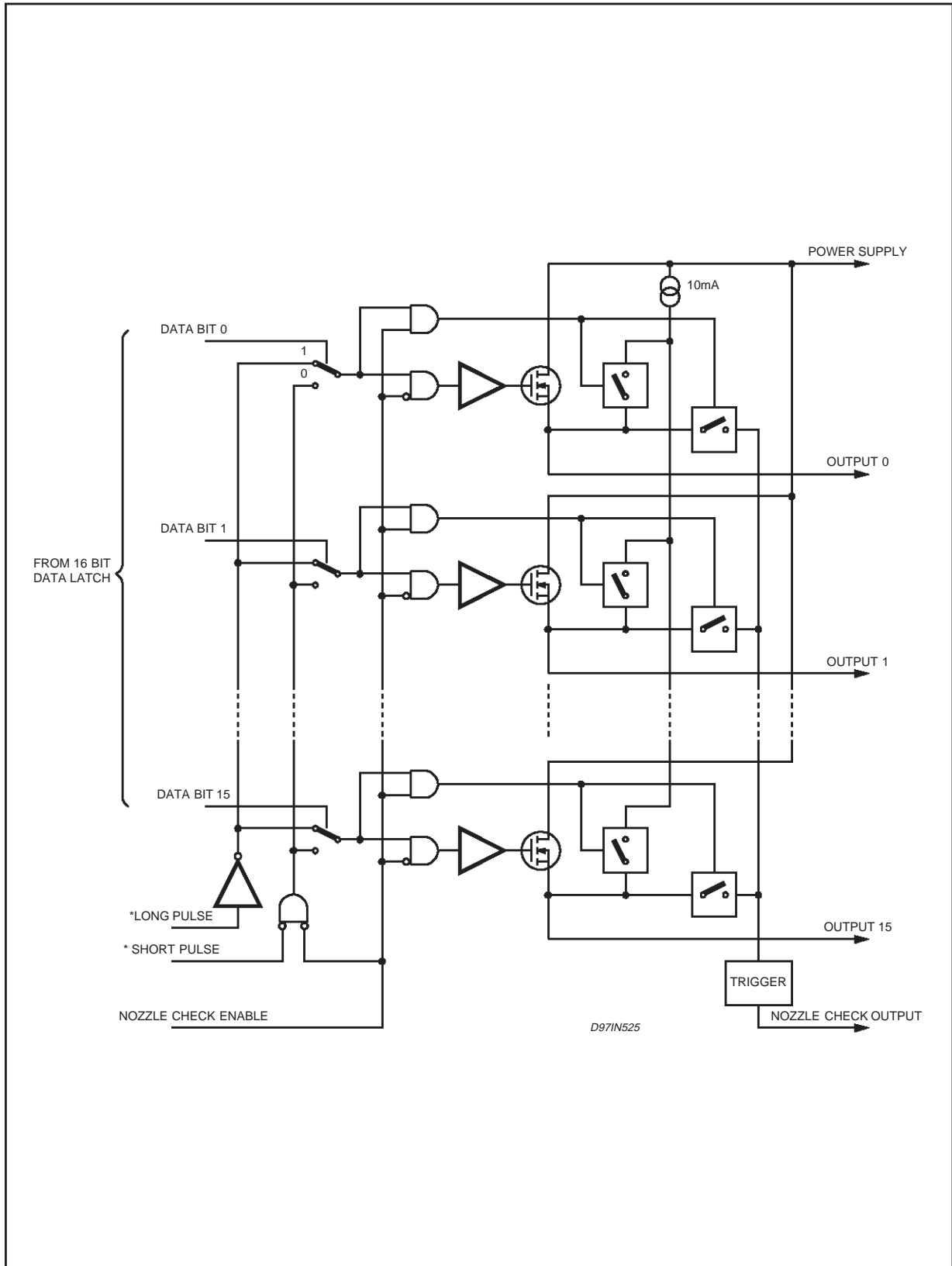


Figure 3. Block Diagram: Power Line Output Stage.



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>c</sub>	Power line supply voltage	14	V
V <sub>r</sub>	Address line supply voltage	14	V
V <sub>a</sub>	Analog supply voltage	14	V
V <sub>dd</sub>	Logic supply voltage	6	V
V <sub>step up</sub>	Driving voltage of power DMOS stage	28	V
V <sub>in</sub>	Logic input voltage range	-0.3 to V <sub>dd</sub> +0.3	V
I <sub>out</sub>	Output continuous current	0.5	A
T <sub>j</sub>	Junction temperature	150	°C
T <sub>amb</sub>	Operating temperature range	0 to 70	°C
T <sub>stg</sub>	Storage temperature range	-55 to 150	°C

DC ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>c</sub>	Power Line Supply voltage	*	10.5 **	11.5	12.5	V
V <sub>r</sub>	Address line supply voltage	*	10.5	11.5	12.5	V
V <sub>a</sub>	Analog supply voltage	*	10.5	11.5	12.5	V
V <sub>dd</sub>	Logic supply voltage		4.5	5	5.5	V
I <sub>cs</sub>	V <sub>c</sub> sleep supply current	ONenable = 1 Reset = 0			1	mA
I <sub>rs</sub>	V <sub>r</sub> sleep supply current				0.3	mA
I <sub>as</sub>	V <sub>a</sub> sleep supply current				3	mA
I <sub>c</sub>	V <sub>c</sub> supply current				1.5	mA
I <sub>r</sub>	V <sub>r</sub> supply current				0.6	mA
I <sub>a</sub>	V <sub>a</sub> supply current	I <sub>REXT</sub> = 3mA			13	mA
I <sub>dd</sub>	V <sub>dd</sub> supply current	sleep or normal condition			5	mA
V <sub>ref</sub>	Reference Voltage	T <sub>amb</sub> = 5 to 55°C	4.85	5	5.15	V
I <sub>refext</sub>	Reference current (external)				7	mA
I <sub>css</sub>	Programmed constant current	$I_{css} = \frac{V_{ref}}{2R_{ext}} \cdot 4$		12	13.5	mA
$\Delta I_{css}/I_{css}$	Constant current regulation	V <sub>a</sub> = 11V T <sub>amb</sub> = 5 to 55°C		0.33		%
V <sub>ampout</sub>	Output voltage of integrated amplifier		e ***		V <sub>a</sub> -1	V
V <sub>cm</sub>	Operating input voltage at pins V <sub>xa</sub> and V <sub>xb</sub>	V <sub>ref</sub> = 5V g <sub>1</sub> =1.2 g <sub>2</sub> =3			7	V
g <sub>1</sub>	Amp. A1 Voltage gain		1.188	1.2	1.212	
g <sub>2</sub>	Amp. A2 Voltage gain		2.95	3.02	3.10	
V <sub>step-up</sub>	Driving Voltage of power DMOS			V <sub>c</sub> +11		V

\* the three supply voltage are independent inside the specified value;

\*\* the Min value for V<sub>c</sub> Power line could be decreased up to 9V (under evaluation);

\*\*\* e = 2 · V<sub>step</sub>

## A/D CONVERTER

V <sub>A/D in</sub>	A/D input voltage	Selected Channel: CH1 to CH5 Selected Ch=CH0	0 e ***		V <sub>ref</sub> V <sub>ref</sub>	V V
I <sub>exch</sub>	A/D input current	Input CH1 to CH5 Channel selected or not			±1	µA

## OFFSET VOLTAGE GENERATION / DAC

V <sub>offset</sub>	Offset Voltage	V <sub>ref</sub> = 5V	25+e***		7.34	V
V <sub>step</sub>	Voltage increment (1LSB)	V <sub>ref</sub> = 5V		156		mV
K <sub>dac</sub>	V <sub>offset</sub> /V <sub>ref</sub>	Any step N>=4			±3	%

DC ELECTRICAL CHARACTERISTICS ( $T_j = 25^\circ\text{C}$ )

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>A/D CONVERTER TIMINGS</b>						
$T_{cscks}$	Conv. start set up time		200			ns
$T_{cckh}$	Conv. Start hold time		200			ns
$T_{ckout}$	Falling edge of clock to data out valid delay	$C_{load} \leq 20\text{pF}$			200	ns
$T_{csz}$	ConvStart falling edge to output in Hi-Z delay				200	ns
$F_{adck}$	Clock frequency				250	KHz
$T_{cslow}$	Conv. Start low level time		5.6			$\mu\text{s}$
$T_{acqth}$	Theoretical acquisition time	$f_{adck} = 250\text{ kHz}$	32.4			$\mu\text{s}$
$T_{acqpr}$	Real acquisition time	$f_{adck} = 250\text{ kHz}$	36			$\mu\text{s}$
<b>DIGITAL INTERFACE INPUT</b>						
$V_{inp}$	Schmitt Trigger positive-going Threshold				$2/3V_{dd}$	V
$V_{inm}$	Schmitt Trigger negative-going Threshold		$1/3V_{dd}$			V
$V_{hys}$	Scmitt Trigger Hysteresis		0.1	0.3	1	V
$I_{in}$	Input Current ( $V_{in}=0$ ; $V_{dd}=5$ )*		50	150	300	$\mu\text{A}$
* This applies to input pins having an internal pull-up (ENABLE_CHANNEL, LONG_PULSE, SHORT_PULSE)						
<b>CR LATCH TIMINGS</b>						
$T_{ls}$	Latch set up time		100			ns
$T_{lhigh}$	Latch high time		100			ns
$T_{lconv}$	Latch data valid to A/D input valid delay	Selected channel: CH1..CH5 CH0	4 7			$\mu\text{s}$ $\mu\text{s}$
NB: The control register (driving signals CRdata, CRclock) is accessed with the same timing specifications as the data 16 bit shift register (signals Serial data, Serial clock)						
<b>SHIFT REGISTER AND LATCH TIMING</b>						
$T_a$	Set up time		50			ns
$T_b$	Hold time		50			ns
$T_c$	Serial clock low time		50			ns
$T_d$	Serial clock high time		50			ns
$T_e$	Serial clock period		150			ns
$T_f$	Latch set up time		100			ns
$T_g$	Latch data high time		100			ns
$T_{set}$	Long Pulse set_up time with respect to NCEn		160			ns
$T_{hold}$	Long Pulse hold time with respect to NCEn		0			ns
<b>OUTPUTS ELECTRICAL CHARACTERISTICS</b>						
$I_{out}$	Output Current (outputs 0..15)	DC=33%; preheating DC=66%		400		mA
$R_{ds(ON)}$	On Resistance	$T_j = 25^\circ\text{C}$			1.3	$\Omega$
$T_{on}$	Turn on Time ( $T_{delay} + T_{rise}$ )	From 50% Long Pulse to 90% power output rising edge Load = 30 Ohm in parallel with 1.5nF			160	ns
$T_{off}$	Toff delay time	From 50% Long Pulse to 90% power output falling edge Load = 30 Ohm in parallel with 1.5nF			100	ns

DC ELECTRICAL CHARACTERISTICS ( $T_j = 25^\circ\text{C}$ )















Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>HEAD ADDRESS SELECTOR OUTPUT</b>						
$T_h$	Up Counting, Reset Counter, Select Channel, Clock Counter and Enable Internal Counter set-up time with respect to Enable channel		150			ns
$T_k$	Up Counting, Reset Counter, Select Channel, Clock Counter and Enable Internal Counter hold time with respect to Enable channel		50			ns
$T_j$	Up Counting with respect to Clock Counter hold time		200			ns
$T_i$	Up counting with respect to Clock Counter set_up time		100			ns
$T_m$	Enable input to active output delay time				100	ns
$T_n$	Clock to active output delay time				150	ns
$T_o$	Disable input to inactive output delay time				100	ns
$f_{\text{clk-counter}}$	Counter Clock Frequency				1	MHz
$\text{CIK}_{\text{dc}}$	Clock duty cycle		10		90	%
$T_{\text{on/off}}$	Turn on/off time	From 50% Clock counter or selector signal to 90% of the address output variation Load: see fig. 10			325	ns

## COUNTER TRUTH TABLE

Enable internal counter = 1

Up Counting = 1

Reset Counter = 1

Clock Counter	C3	C2	C1	C0
0	0	0	0	0
	0	0	0	1
	0	0	1	1
	0	0	1	0
	0	1	1	0
	0	1	1	1
	0	1	0	1
	0	1	0	0
	1	1	0	0
	1	1	0	1
	1	1	1	1
	1	1	1	0
	1	0	1	0
	1	0	0	0
	0	0	0	0



**COUNTER TRUTH TABLE** (continued)

Enable internal counter = 1

Up Counting = 0

Reset Counter = 1

Clock Counter	C3	C2	C1	C0
0	0	0	0	0
	1	0	0	0
	1	0	1	0
	1	1	1	0
	1	1	1	1
	1	1	0	1
	1	1	0	0
	0	1	0	0
	0	1	0	1
	0	1	1	1
	0	1	1	0
	0	0	1	0
	0	0	1	1
	0	0	0	1
	0	0	0	0

**DECODER TRUTH TABLE**

OUTPUTS (HS) ACTIVE	C3	C2	C1	C0
All inactive	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	0	1	0
4	0	1	1	0
5	0	1	1	1
6	0	1	0	1
7	0	1	0	0
8	1	1	0	0
9	1	1	0	1
10	1	1	1	1
11	1	1	1	0
12	1	0	1	0
13	1	0	0	0
All inactive	1	0	0	1
All inactive	1	0	1	1

This table is valid for both Channel A and Channel B and when Enable Channel is set to low level.

**PRINT HEAD TEMPERATURE CONTROL PART**  
**Introduction**

For quality printing, it is necessary to know and control the temperature of the printhead. Thus, the latter has a built-in aluminium resistor, whose value changes slightly with the temperature. The temperature determination is done by injecting a constant current in the resistor, and measuring the voltage drop across it. Since high-end printers have two heads, it must also be possible to switch quickly the measurement process from one to the other. The function is foreseen to be integrated into the head driver, and is described hereafter.

**Print Head Block Diagram (fig. 4)**

At first we have a constant current source, which can be disabled by an external pin (ONenable) or by a control register, described later. The value of the current can be programmed by an external resistor, and is given by:

$$I_{CCS} = \frac{V_{ref} \cdot 4}{2 \cdot R_{ext}}$$

This current is injected either into the aluminium resistor of the head A (Ralu. A) or B (Ralu. B), depending of the switch SW3. The alu. resistors are grounded, and the voltage at their << hot >> side

(Vx) is re-entered via the pins Vxa and Vxb. Using separate pins from Rxa and Rxb permits to be more flexible, and a filter can eventually be added as shown in the drawing.

The voltage Vx is amplified by A1 and A2, and then converted in a digital value. To be compatible with the input range of the A/D converter, it is necessary to subtract an offset voltage Voffset from Vx. Moreover, as the initial value of the alu. resistor is very unprecise. Voffset must be adjustable; this is done by means of a 5 bit - D/A converter, giving 32 different values. Finally, the voltage at the input of the A/D converter is:

$$V_{CH0} = g1 \cdot g2 \cdot Vx - g2 \cdot V_{OFFSET}$$

or

$$V_{CH0} = g1 \cdot g2 \cdot Ralu \cdot I_{CCS} - g2 \cdot V_{OFFSET};$$

$$V_{OFFSET} = V_{REF}/2 + N \cdot V_{REF}/32 \quad N = 0, 1, \dots, 31$$

The reference voltage generator (VREF) is integrated, and used for the current source and both the A/D and D/A converters. In this way, the system performance is independent from the precision of VREF; this one should, however, be stable. Vref is also available on pin #45, and can be used for low consumption purposes. (The external sinked current has to be a DC current)

The system is under control of a 10 bit register, CR. CR is accessed serially and has a transparent latch, which can be used or not (by trying the latch signal CR latch to Vcc).

**Figure 4. Print Head Block Diagram**

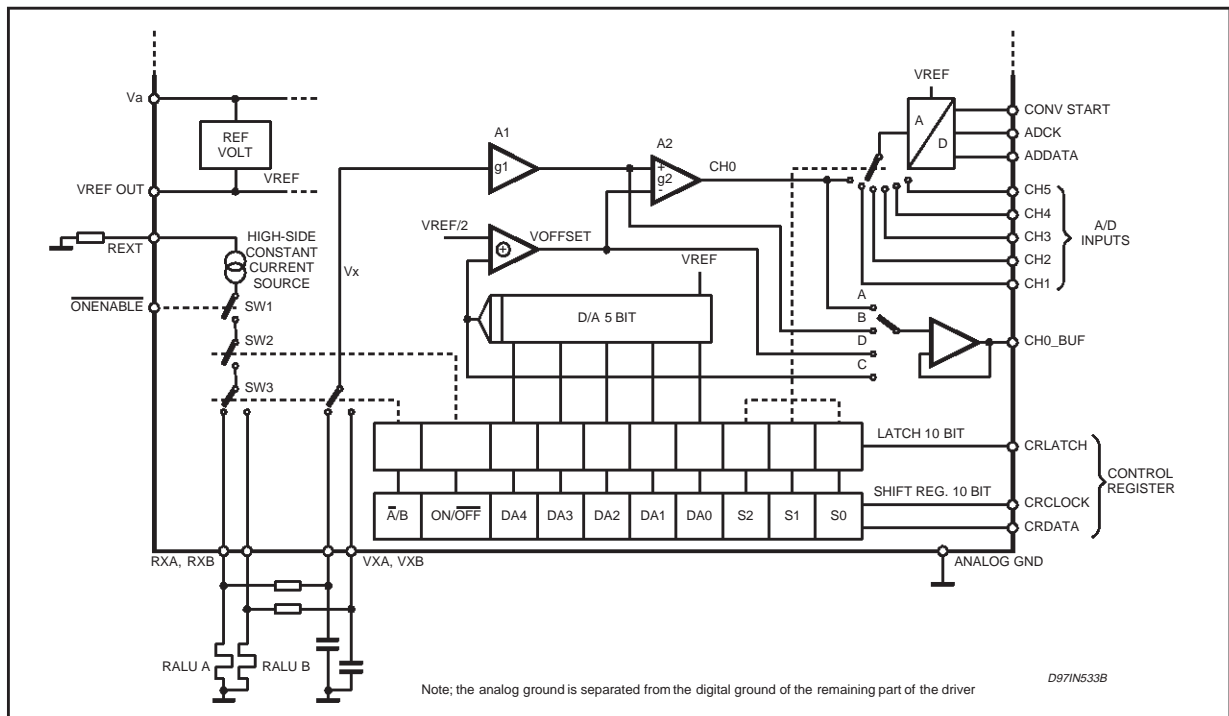


Figure 5. Control Register details.

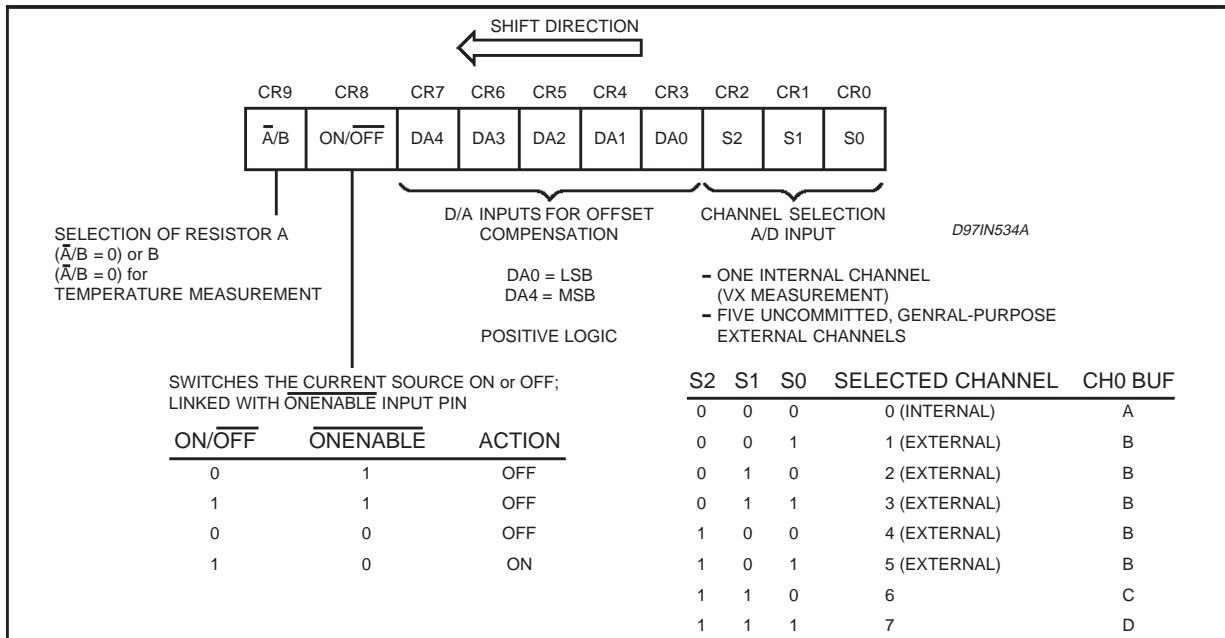


Figure 6. CR Latch Timings

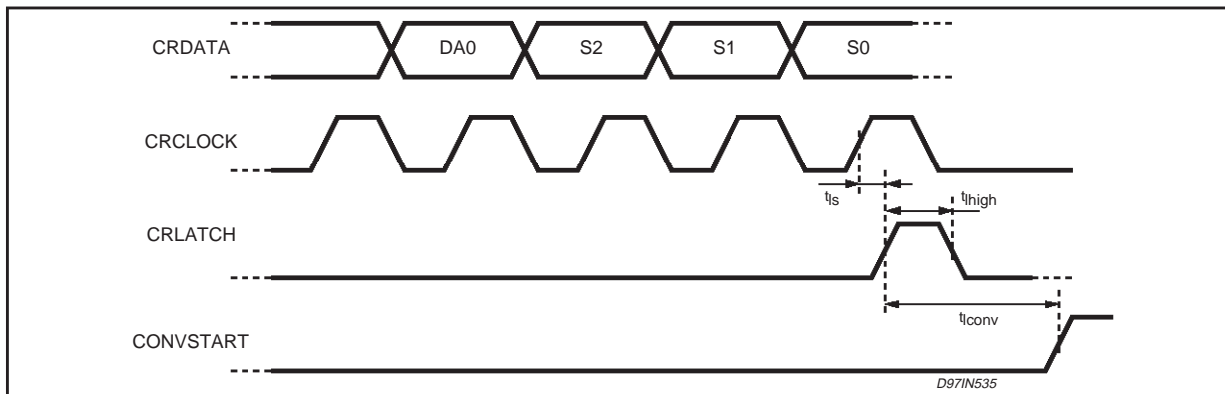


Figure 7. A/D Converter Timings

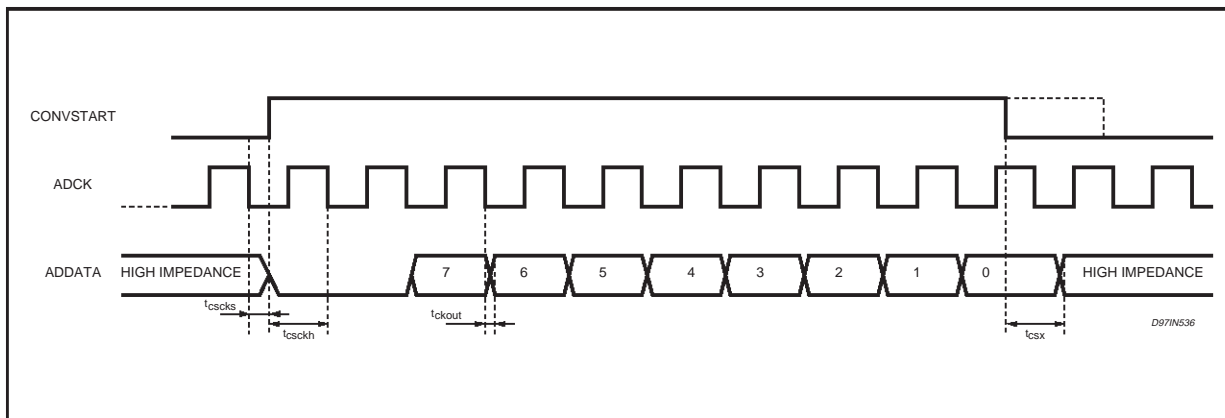


Figure 8. Power Output Timing

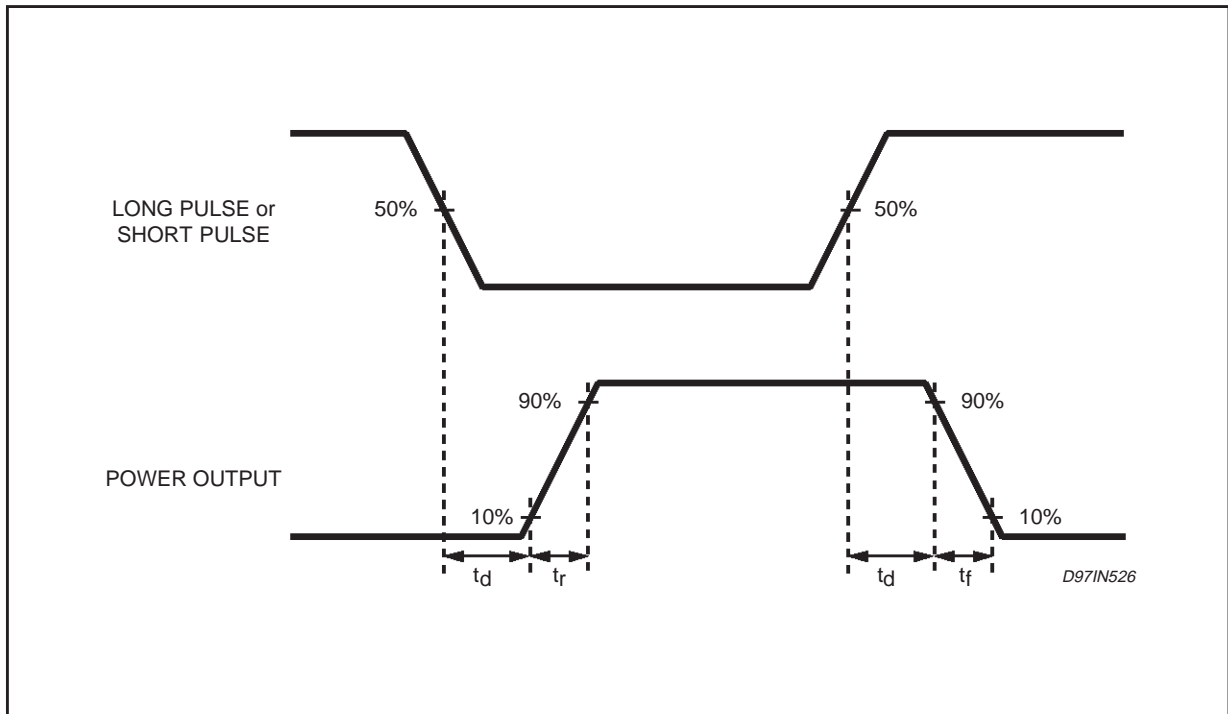


Figure 9. Trigger of Nozzle Check Signal

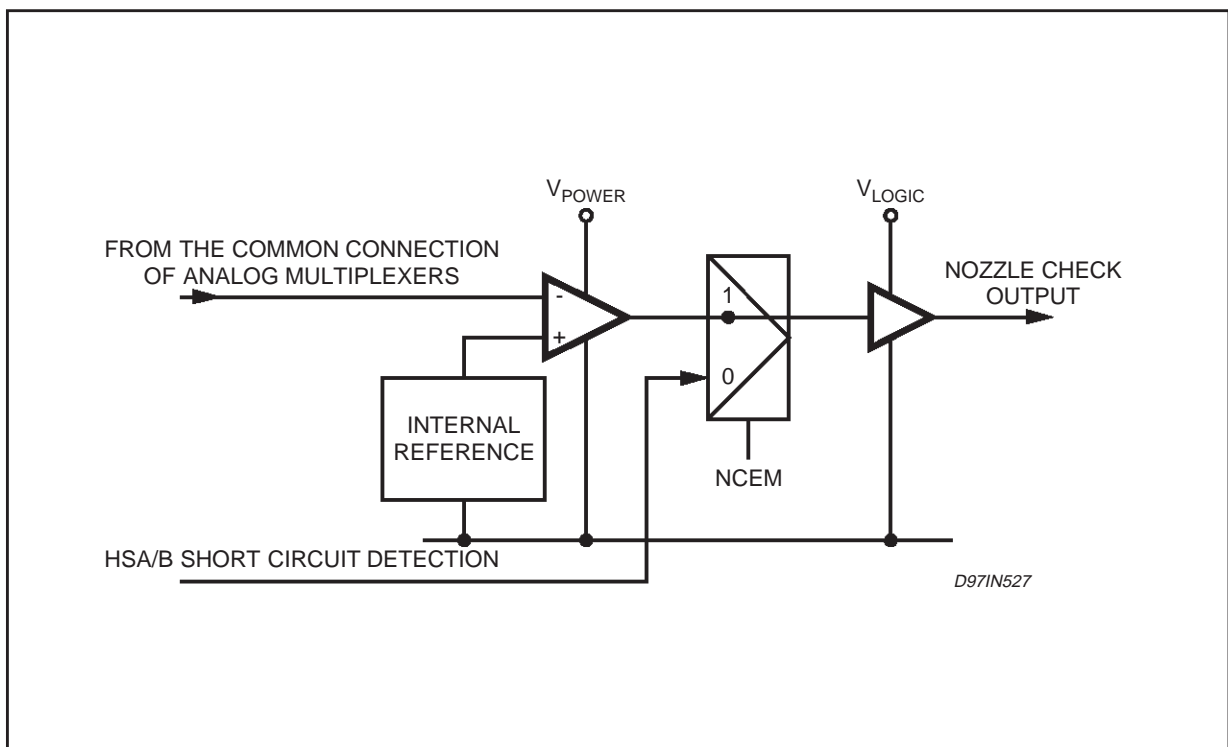


Figure 10. Address Output Timing

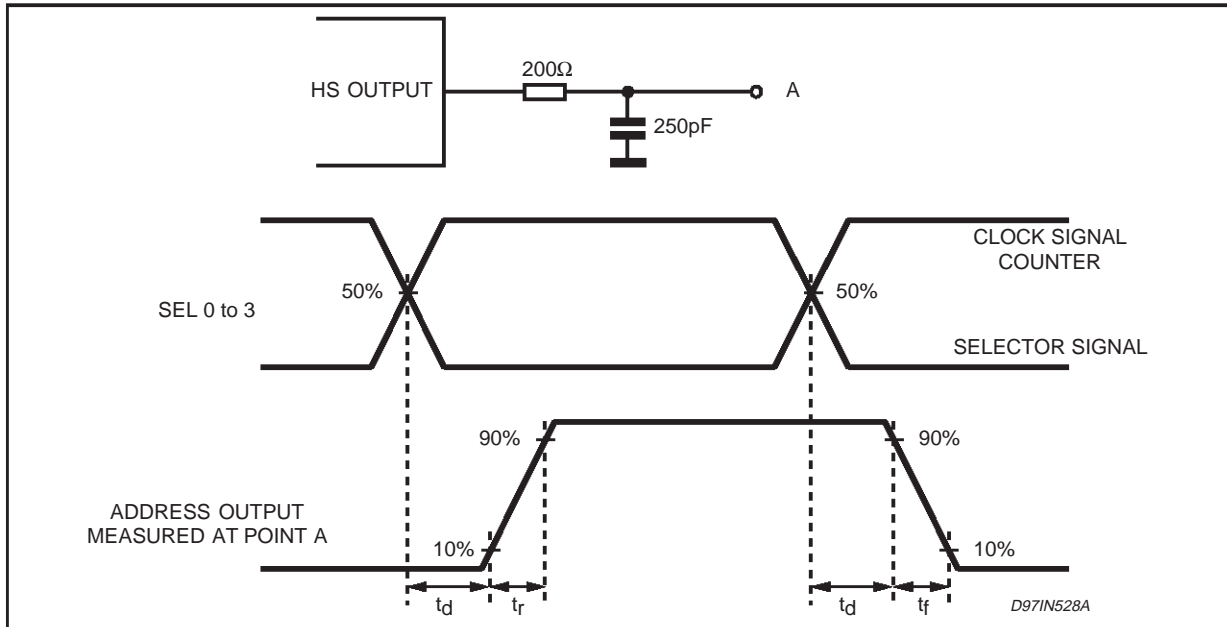


Figure 11. Mode Counter

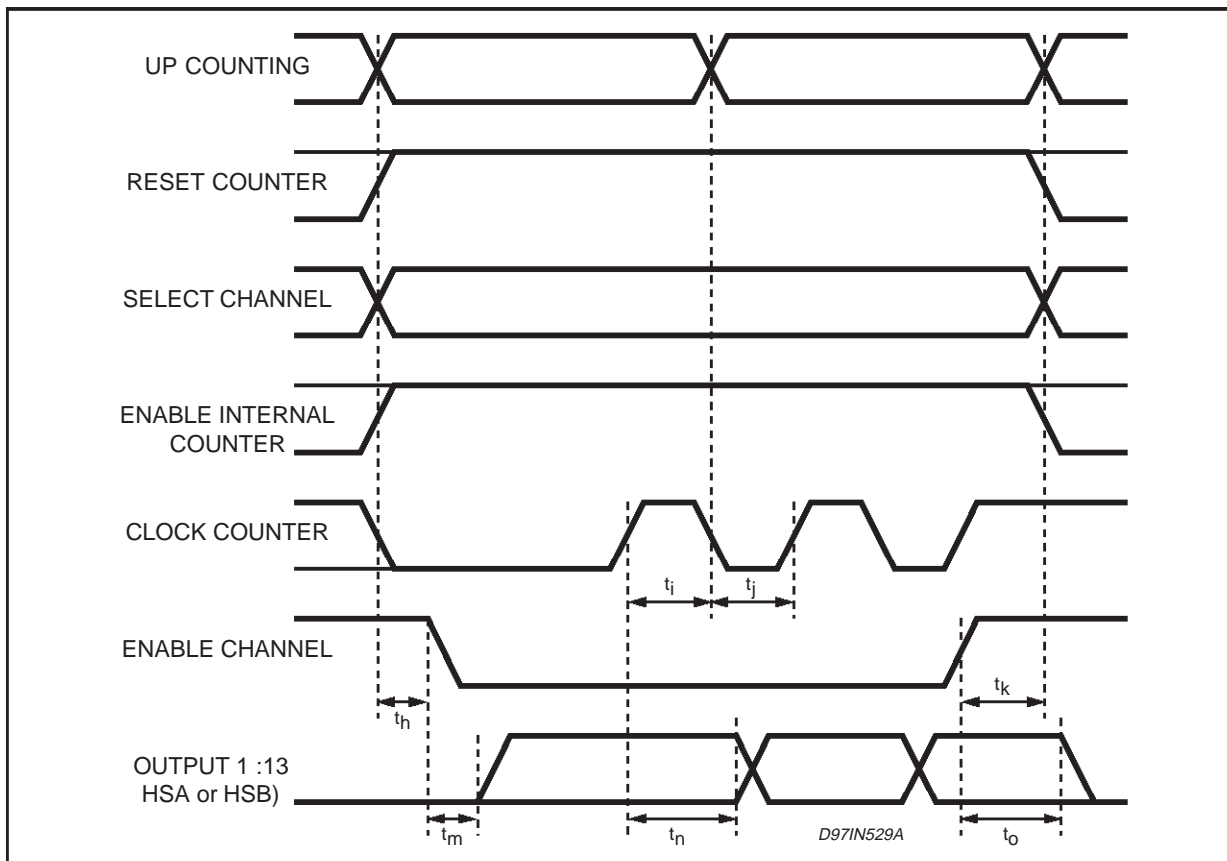


Figure 12. Mode Sel 0:3

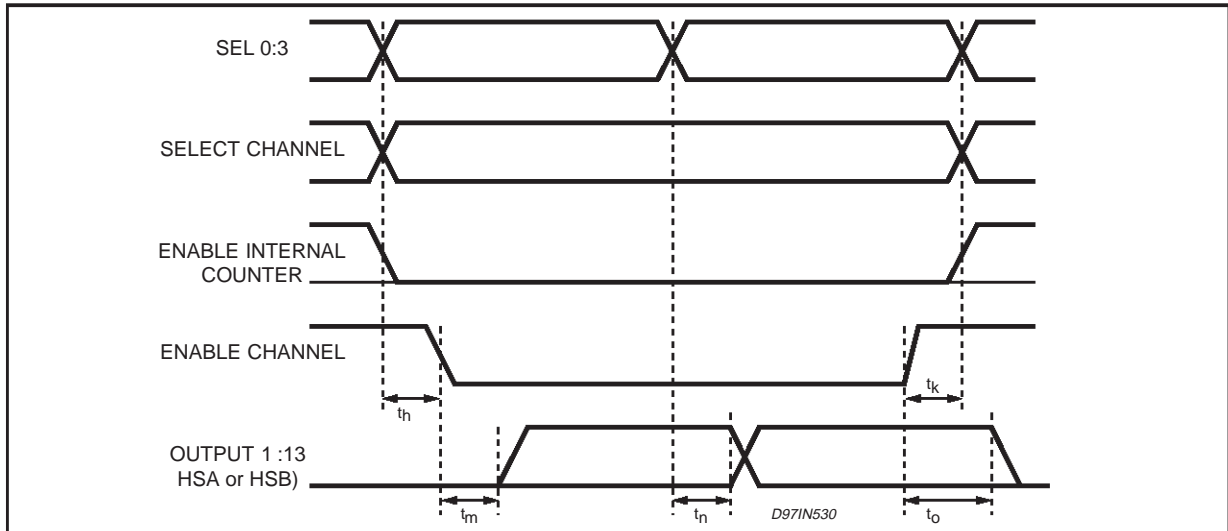


Figure 13. Sequence of Shift Register Data Loading

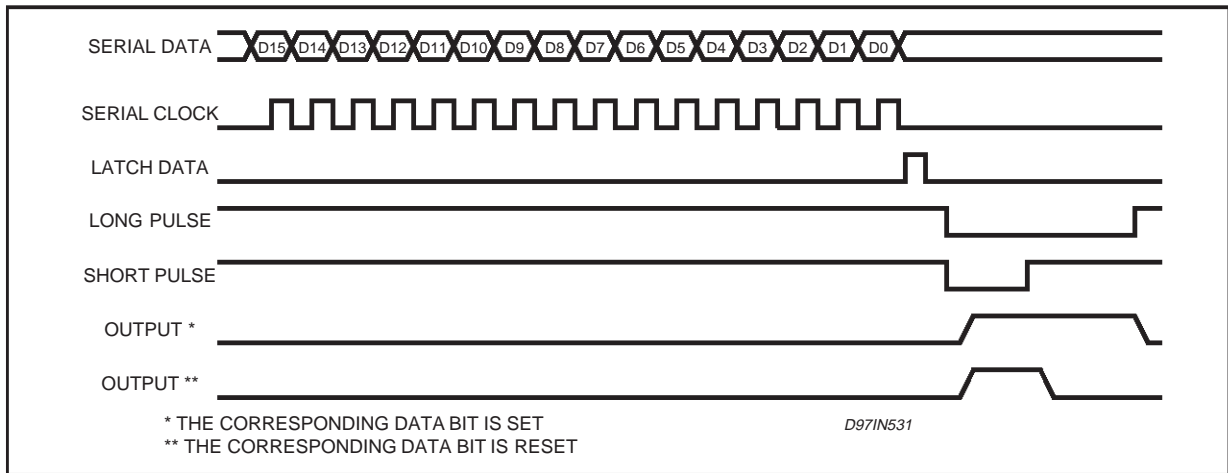
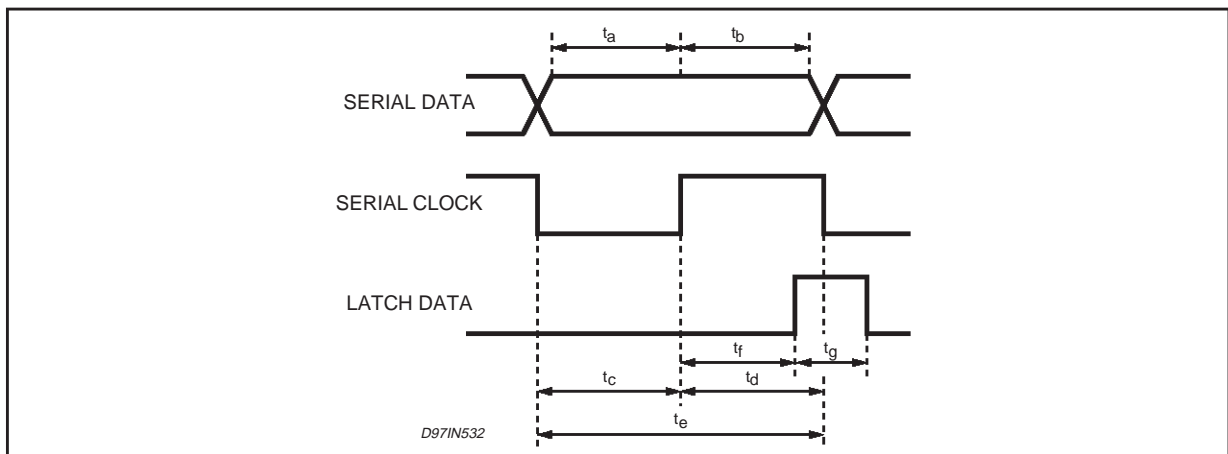
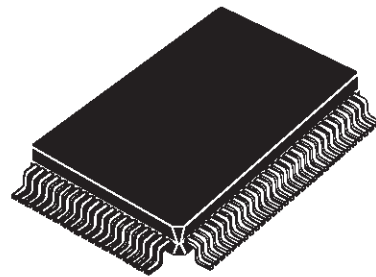


Figure 14. Latch Timing

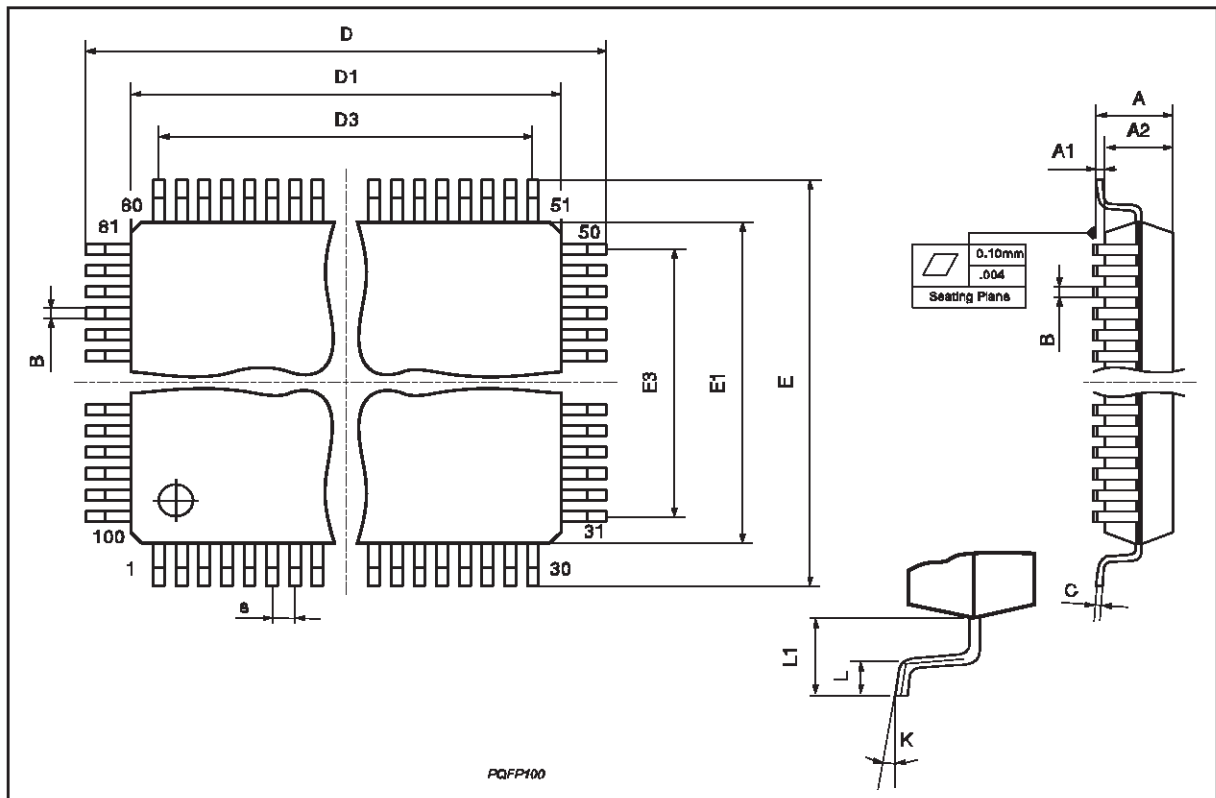


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.22		0.38	0.0087		0.015
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
e		0.65			0.026	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

## OUTLINE AND MECHANICAL DATA



**PQFP100**



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