SGS-THOMSON MICROELECTRONICS

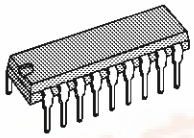
L6605

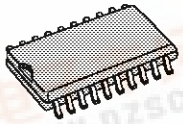
SMART CARD INTERFACE

ADVANCE DATA

- 8 DIFFERENT VPP OUTPUT VOLTAGE LEVELS
- V_{PP}, V_{CS} RISE AND FALL TIME FULL SPEC WITH ISO/IEC 7816-3
- POWER SUPPLY OUTPUT FOR MEMORY CARD (5V/80mA)
- POWER ON/OFF RESET
- AUTOMATIC SWITCH-OFF OF ALL FUNCTIONS IF THE REGULAR OPERATION IS ABORTED BY EXTRACTING THE SMART CARD
- INTERNAL STATUS FAILURE CODING
  - INSERTION FAILURE CODE
  - OVERTEMPERATURE FAILURE
- ANTI-BOUNCING SYSTEM
- INPUT/OUTPUT LOGIC TTL COMPATIBLE
- THERMAL PROTECTION

MULTIPOWER BCD TECHNOLOGY





Powerdip 12+3+3 **SO 12+4+4**

ORDERING NUMBERS:

L6605 L6605D

DESCRIPTION

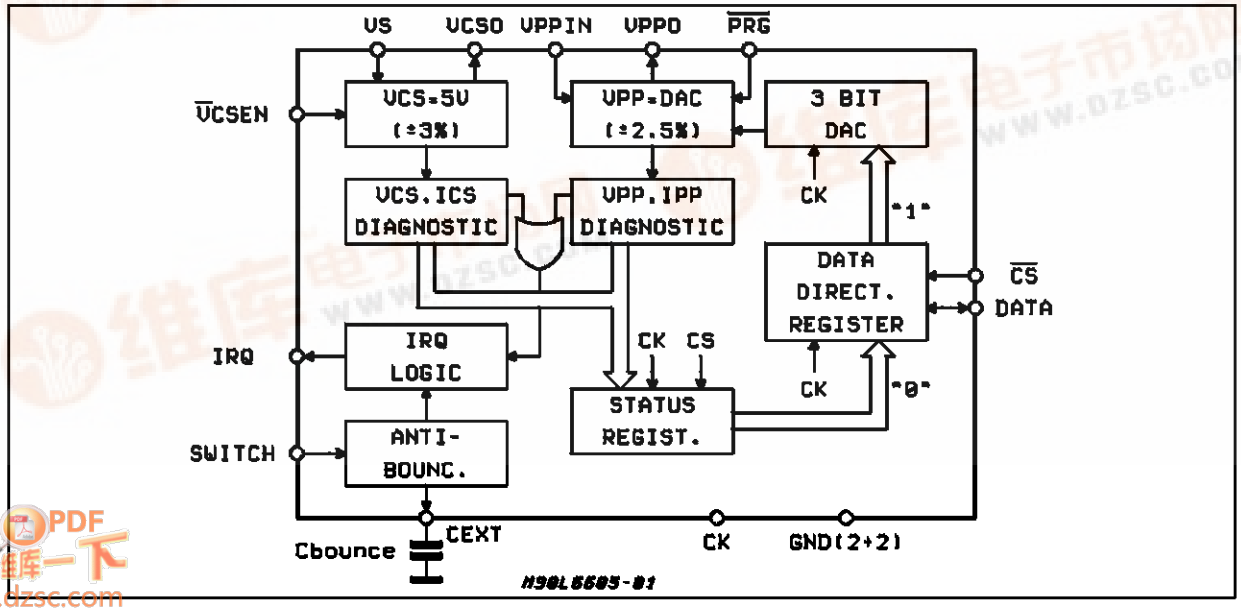
The L6605 is an IC dedicated as intelligent interface between different types of smart cards and microprocessors. The internal architecture can be shared in a power supply section and in a diagnostic parts.

The power supply section can deliver 5V/80mA to supply the card and V_{PP}/50mA to write the memory inside the card; the V_{PP} voltage can be programmed by means of the 3 serial input bit (see TAB, 1).

Table 1: 3 bit DAC CODE

CODE	V_{PP}
0 0 0	5V
0 0 1	10V
0 1 0	12.5V
0 1 1	13.5V
1 0 0	15V
1 0 1	18V
1 1 0	21V
1 1 1	25V

BLOCK DIAGRAM

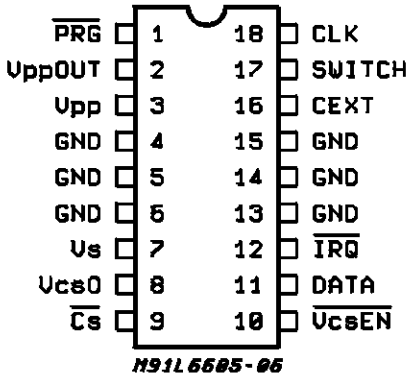


DESCRIPTION (continued)
The diagnostic part allows to monitor failures due to overtemperature or wrong card positioning. The failures are internally coded and readable inside the STATUS REGISTER through the bidirectional pin DATA configurated in output.
The antibouncing circuitry, active during card insertion only, rejects ripetitive switching-on of the power supply sections.

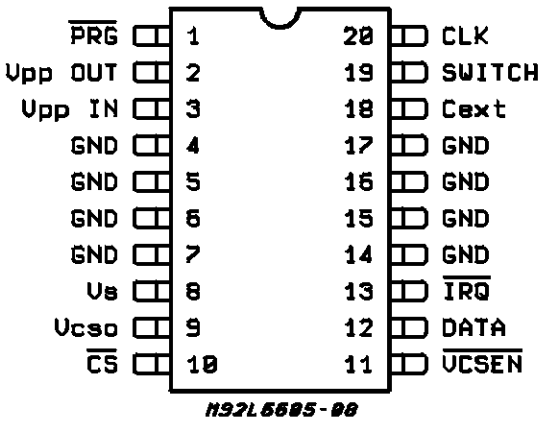
PIN FUNCTION

Pin	Description
V_S	Input Power Supply voltage for V_{CS} regulated output and for device supply.
V_{CSO}	Output regulated voltage for card supply; I_{CSmax} = 80mA; overload protected (81 to 200mA)
V_{PPIN}	Input power supply for V_{PP} regulated voltage
V_{PPOUT}	Programmable output regulated voltage for memory card writing; 8 voltage levels are allowed by means of 3 bit DAC. I_{PPmax} = 50mA.
$V_{\overline{CSEN}}$	(Active Low) V_{CS} supply input enable; Its value is fixed from the µP allowing or not the normal R/W operations on the card.
SWITCH	Input signal produced by the reader system indicating that a card has been inserted. Internally, an antibouncing system is provided to avoid multiple switching.
$\overline{CS}$	Chip select (active low). $\overline{CS}$ low level indicates an I/O operation request from µP.
IRQ	Interrupt Request (Active low). An IRQ low level indicates that a card insertion/extraction or Failure has occured.
$\overline{PRG}$	Program (Active low). PRG low level enables L6605 to deliver in output the V_{PPO} level set by 3 bit DAC.
DATA	I/O pin for data exchange between µP and the device. Through this pin flow 3 bit input DAC or 2 bit STATUS REGISTER code.
CK	External clock.
C_{EXT}	Pin to connect an external capacitor for antibouncing delay time.
GND	4 pins to ground.

PIN CONNECTIONS (Top view)



Powerdip 12+3+3



SO 12+4+4

THERMAL DATA

Symbol	Parameter	L6605	L6605D	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	60	50 (*)	°C/W

(*) Soldered an a 35µ thick 6cm^2 P.C. board copper area.

ELECTRICAL CHARACTERISTICS (V_S = 12V; T_j = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10	12	15	V
V_{CS}	Card Supply Voltage (Logic Inputs onset)	I_{CS} = 80mA, V_S = 12V	4.85	5	5.15	V
		I_{CS} = 1mA to 80mA V_S = 10V to 15V $C_{LOAD\,min}$ = 5nF; $C_{LOAD\,max}$ = 20µF	4.75	5	5.25	V
I_{CS}	Current Supply Card				80	mA
I_{CSS}	I_{CS} Short Circuit	V_S = 12V	81		200	mA
V_{PPI}	V_{PP} Supply Voltage		V_{PPO} + 2.5V		33	V
V_{PPO}	Programming Voltage	I_{PP} = 50mA; V_{PPI} = 30V; $T_{on} \leq$ 5ms	-2.5%	V_{DAC}	+2.5%	V
		I_{PP} = 1mA to 50mA V_{PPI} = max. 33V (see note 1) $C_{LOAD\,min}$ = 5nF $C_{LOAD\,max}$ = 500nF (see note 2)	-5%	V_{DAC}	+5%	V
I_{PP}	Output Program. Current	V_{PPI} = 30V			50	mA
I_{PPs}	I_{PP} Short Circuit		51		150	mA
t_{on}	V_{PP}, Rise Time	$C_{LOAD\,min}$ = 5nF $C_{LOAD\,max}$ = 500nF (see note 2) I_L = 50mA (see note 1)			200	µs
t_{off}	V_{PP}, Fall Time				200	µs
t_{shadow}	Shadow Timing	Cbounce = 0.1µF		1		ms
V_{SWLOW}	Low Level Switch Input				0.8	V
V_{SWHIGH}	High Level Switch Input		2		Vs-2V	V
t_{CKON}	Clock ON Time	C_{LOAD} = 50pF, I_{SINK} = 4mA, V_L = 0.4V	1			µs
t_{CKOFF}	Clock OFF Time		1			µs
t_D	Delay Time		250			ns
$t_{SET-UP1}$	1st bit Set-up Time		500			ns
t_{HOLD1}	1st bit Hold Time		500		t_{CKON}	ns
$t_{SET-UP2}$	Data Set-up Time		500			ns
t_{HOLD2}	Data Hold Time		500			ns
t_{SCK}	Clock Set-up Time		250			ns
t_{HCK}	Clock Hold Time		250			ns
f	Clock Frequency				500	KHz
SR	V_{PP} Slew Rate	From rest state to programming state and viceversa			2	V/µs
V_{STH}	Power ON/OFF Threshold	Logic inputs onset		8.5	9.5	V
V_{SHY}	V_{STH} Hysteresis			0.6		V
T_S	Thermal Shutdown			180		°C
T_H	Thermal Hysteresis			20		°C

Note 1: True for values in Tab. 1 only. ; **Note 2:** Values higher than 500nF are permitted, but the ton, toff timing will be out ISO norm.

CIRCUIT OPERATION

CARD POWER SUPPLY

Regulated voltage to supply the card (5V/80mA). During nominal condition (V_S = 12V, I_{CS} = 80mA) the V_{CS} range variation is equal to ± 3%.
While during line/load variation (V_S = 10V to 15V; I_{CS} = 1mA to 80mA) the V_{CS} range is ± 5%.
An internal circuitry checks the I_{CS} level; the protection block activates an IRQ with the proper failure code when the output current is in 81mA to 200mA range.

PROGRAMMING POWER SUPPLY

L6605 works in step-down mode by means of the programmed output voltage V_{PP}. 8V_{PP} levels can be selected programming the 3 bit DAC as per Table 1. During nominal conditions (I_{PP} = 50mA; V_{PPI} = 30V) the V_{PP} range variation is equal to

±2.5%; while during line/load variation (I_{PP} = 1mA to 50mA; V_{PPI} = max. 33V) the V_{PP} range is ±5%. An internal circuitry checks the I_{PP} level; the protection block activates an IRQ with the proper failure code when the output current is in 51mA to 150mA range. Under the power ON/OFF threshold value the logic section and the power supply regulators are disabled.

LOGIC SECTION
L6605 includes a logic circuitry in order to protect, both card and itself. If a failure occours an asynchronous IRQ is sent to the µP; consequently the µP forces low CS signal as I/O request. After CS variation the µP sends also one "data direction bit" into DATA DIRECTION REGISTER.

- Direction bit = "0"
  Pin DATA is configurated in output and the µP reads the 2 bit STATUS REGISTER content

Code	1st bit	2nd bit
0	No insertion	No Failure
1	Card Inserted	Failure

Failure could be overtemperature over the 2 regulators (VPP, VCS).

- Direction bit = "1"
  Pin DATA is configurated in input to allow the 3 bit DAC loading and than the programming of V_{PP0} output level voltage. (see Table 1).

During card insertion only rising edge of switch signal is detected , while during card extraction switch level is detected.

In card extraction mode if occours a mechanical switch bouncing, which causes a pulse on SWITCH input pin with duration t ≥ 50µs the L6605 will have the 1st Status Register content equal to "0" and 1 ms t_{shadow} timing like during card insertion mode.
Bouncing on SWITCH pin with duration T<50µs will be transparent in the Status Register.

Figure 1: Card Insertion

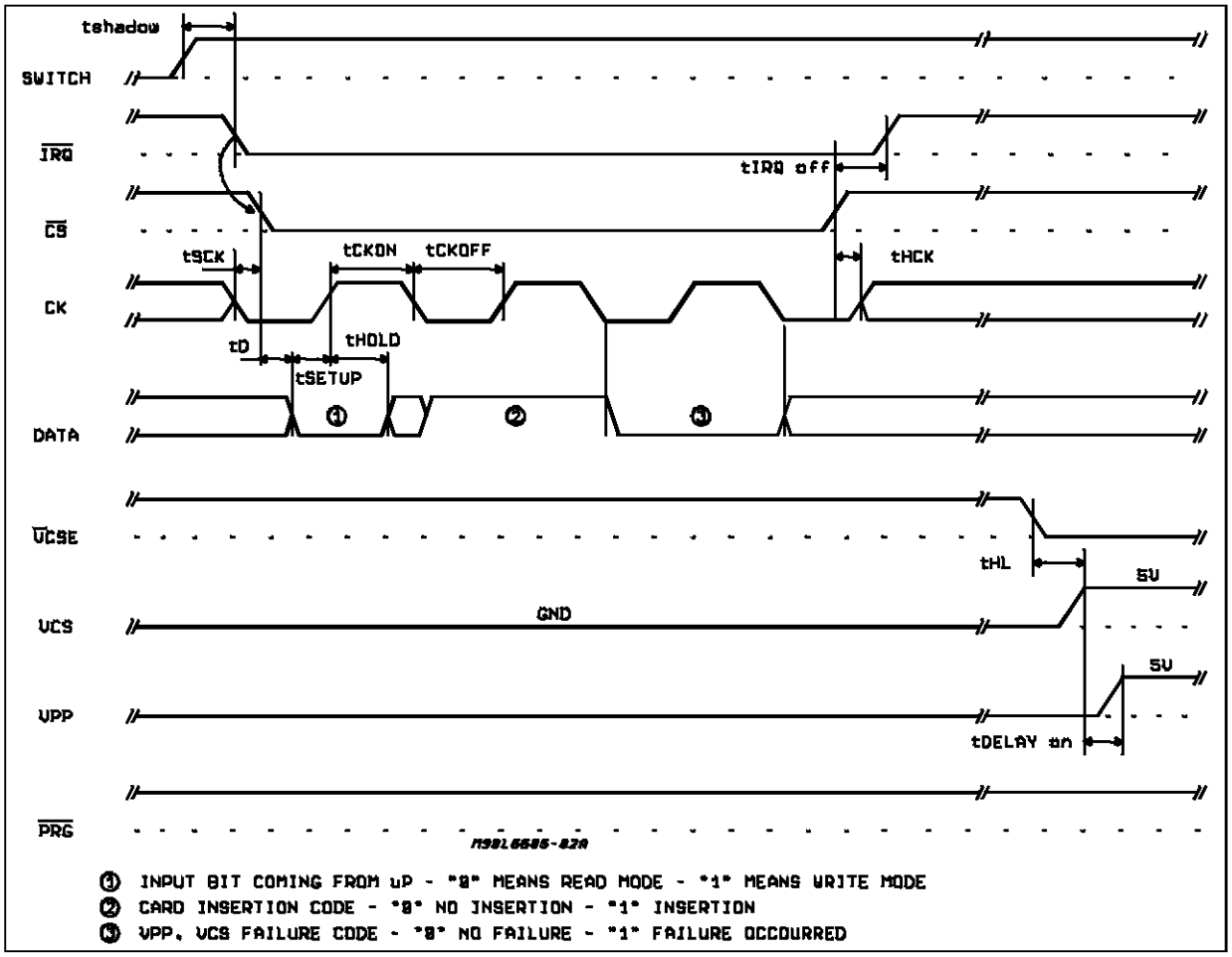


Figure 2: DAC Loading and Programmed Voltage on Set

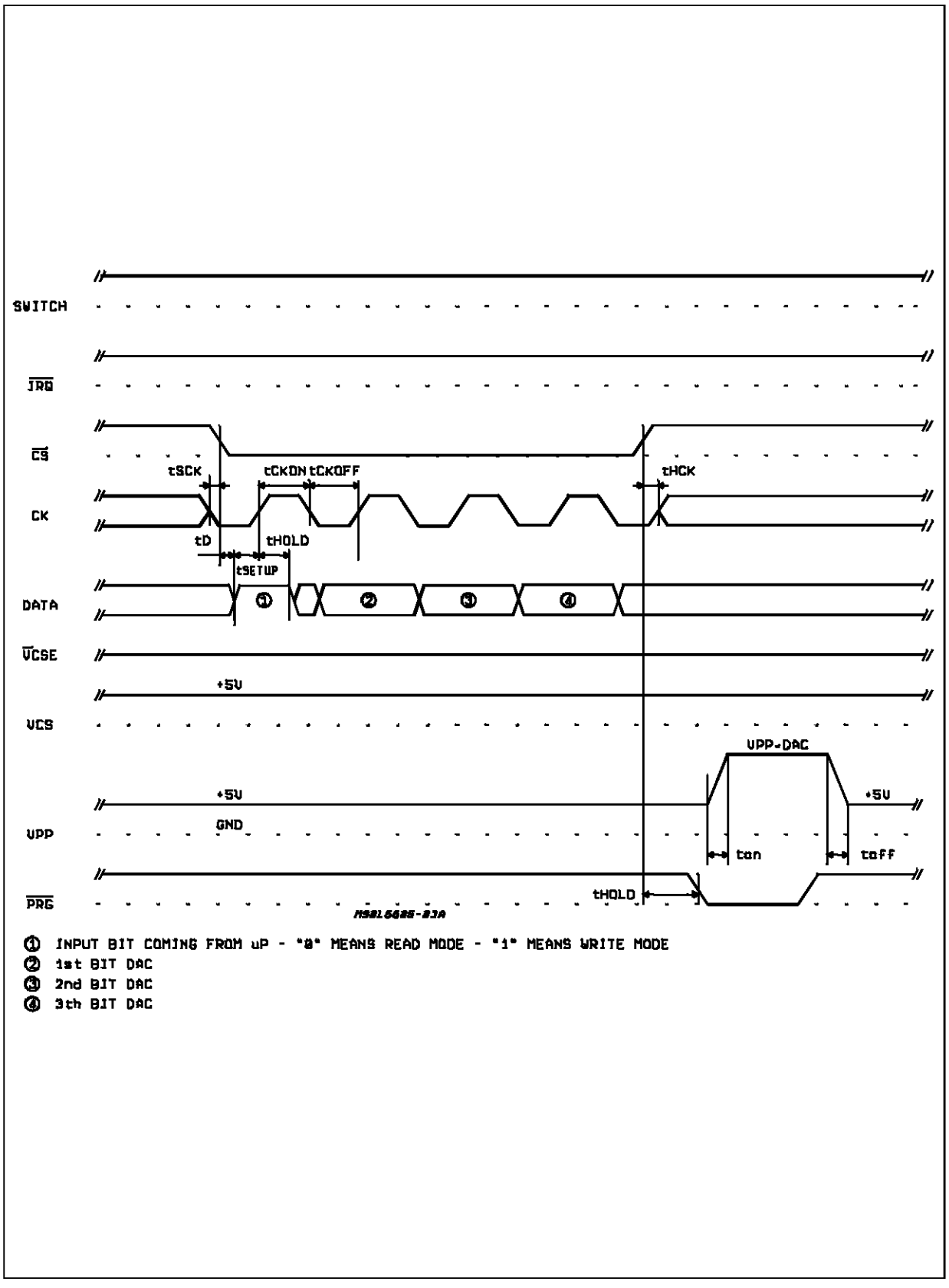


Figure 3: End Normal Operation

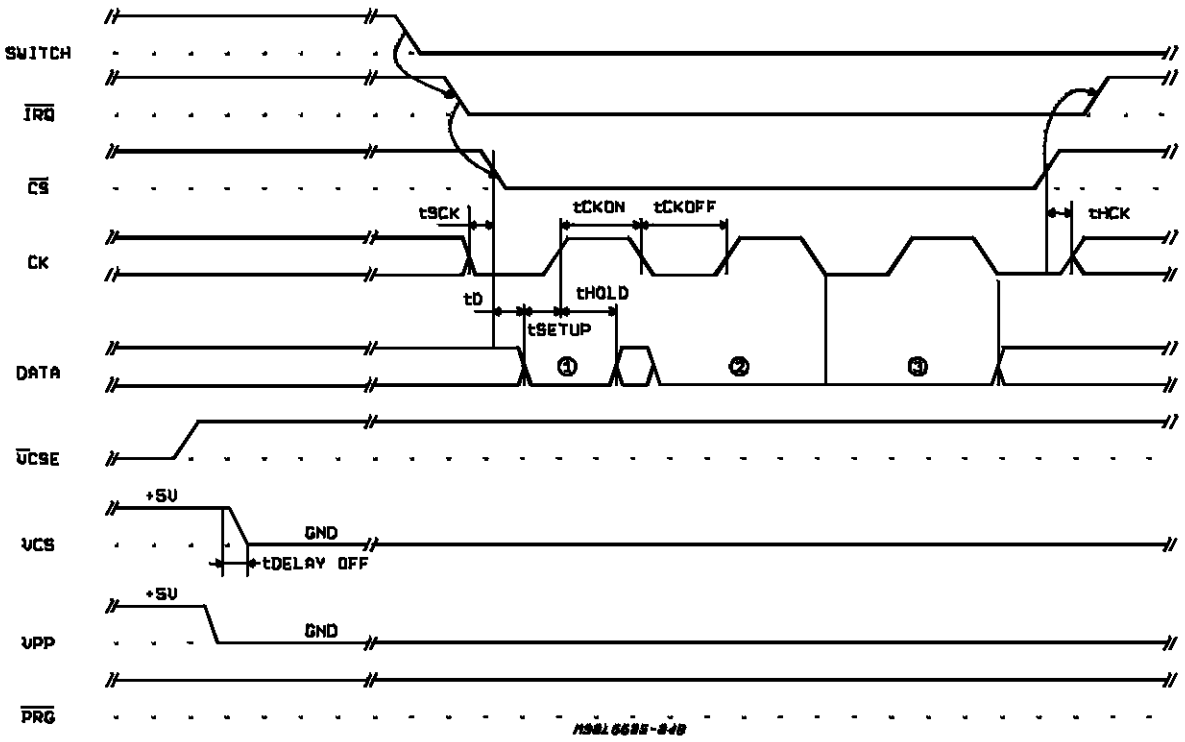


Figure 4.

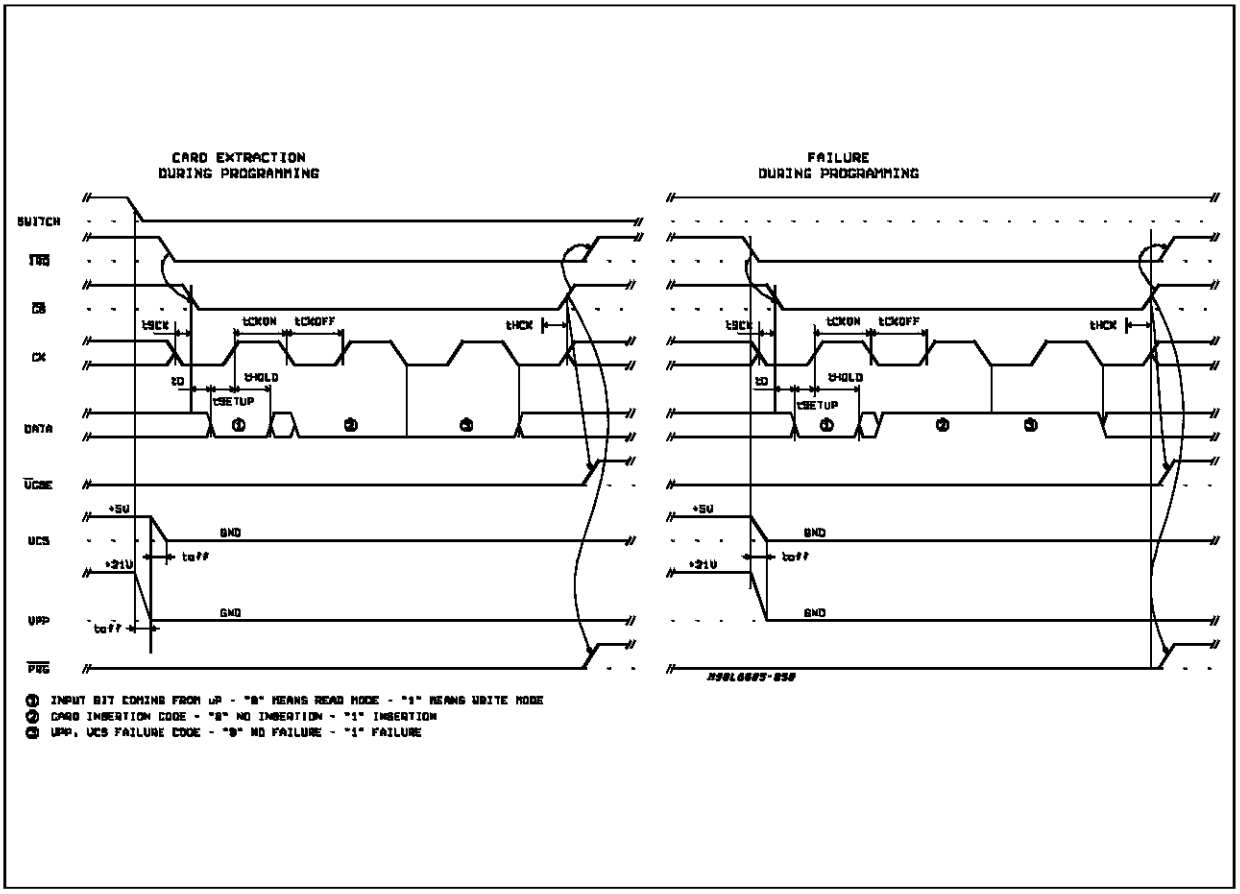
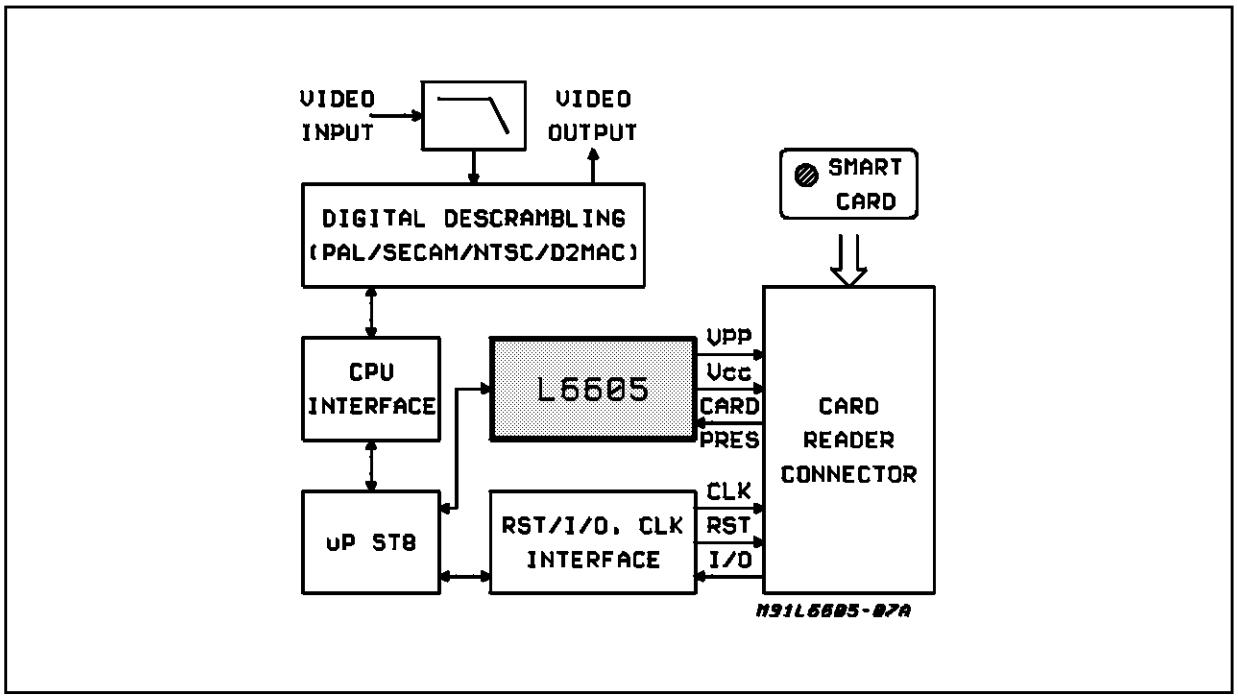
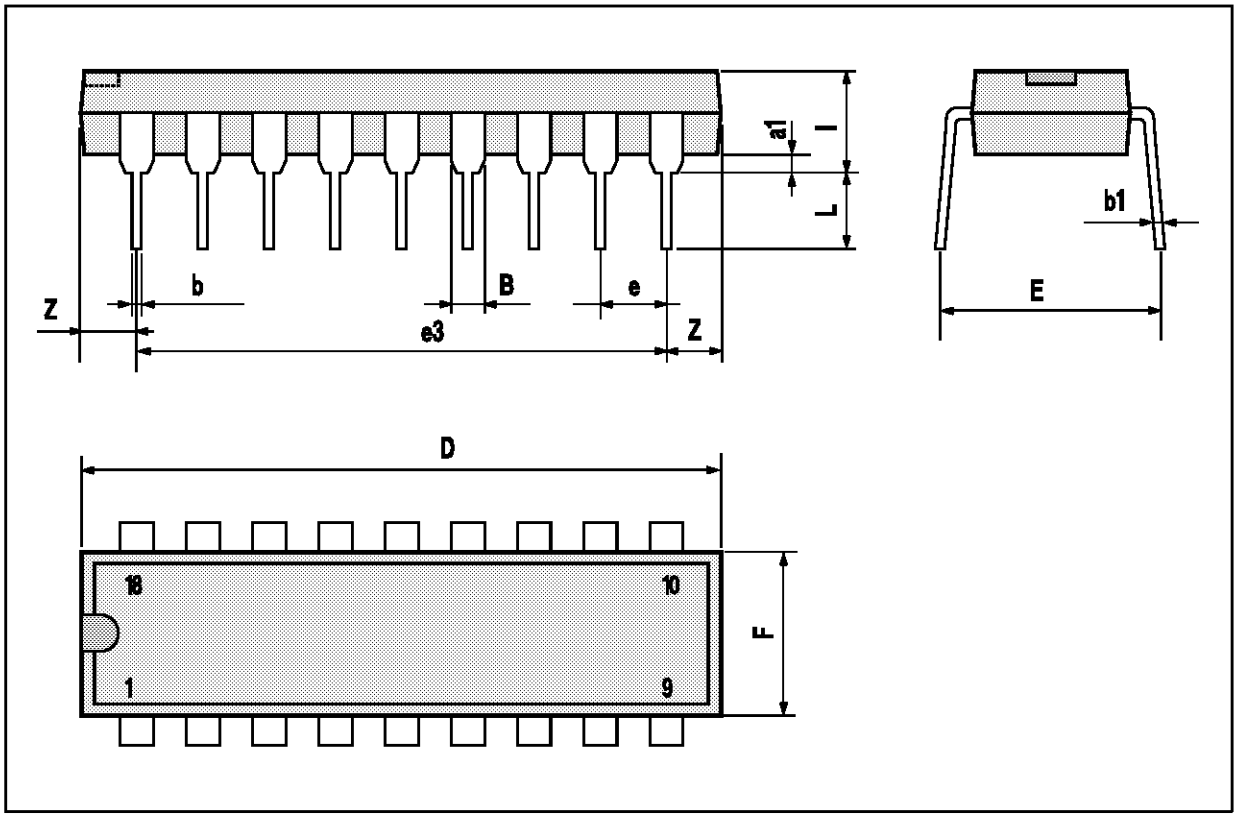


Figure 5: PAY-TV Application



POWERDIP18 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)