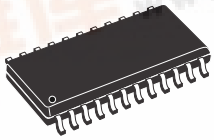
L6996

DINAMICALLY PROGRAMMABLE SYNCHRONOUS STEP DOWN CONTROLLER FOR MOBILE CPUs

- 5 BIT DAC WITH AVAILABLE EXTERNAL OUTPUT VOLTAGE.
- 0.6 TO 1.750V, DYNAMICALLY ADJUSTABLE OUTPUT VOLTAGE RANGE.
- ±1% OUTPUT ACCURACY OVER LINE AND LOAD.
- ACTIVE DROOP.
- CONSTANT ON TIME TOPOLOGY ALLOWS LOW DUTY CYCLE AND FAST LOAD TRANSIENT.
- 90% EFFICIENCY FROM 12V TO 1.35V/8A.
- 1.750V TO 28V BATTERY INPUT RANGE.
- OPERATING FREQUENCY UP TO 1MHZ.
- INTEGRATED HIGH CURRENT DRIVERS.
- LATCHED OVP AND UVP PROTECTIONS. OCP PROTECTION.
- 350µA TYP. QUIESCENT CURRENT.
- 7µA TYP. SHUTDOWN SUPPLY CURRENT.
- PGOOD AND OVP SIGNALS.
- ZERO-CURRENT DETECTION AND PULSE-FREQUENCY MODE.



TSSOP24

ORDERING NUMBERS: L6996D (TSSOP24)
L6996DTR (Tape & Reel)

APPLICATIONS

- ADVANCED MOBILE CPUs SUPPLY WITH DYNAMIC TRANSITIONS.
- NOTEBOOK/LAPTOP, CONCEPT PC CPUs SUPPLY.
- DC/DC FROM BATTERY SUPPLY EQUIPMENTS.

DESCRIPTION

The device is dc-dc controller specifically designed to provide extremely high efficiency conversion for mobile advanced microprocessors.

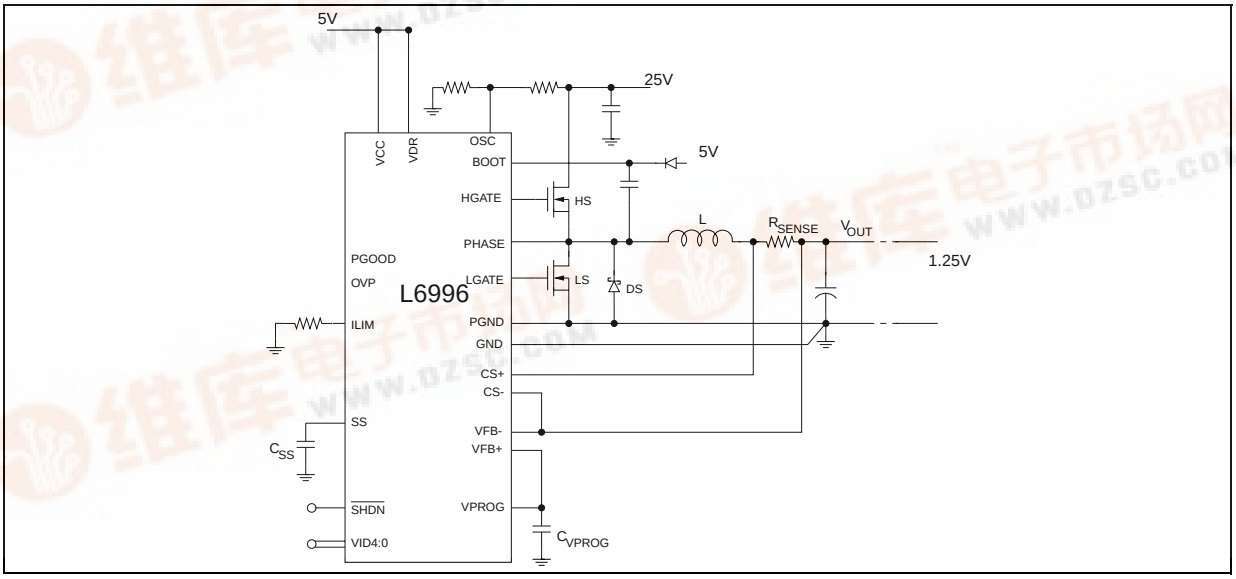
The "constant on-time" topology assures fast load transient response. The embedded "voltage feedforward" provides nearly constant switching frequency operation.

A precise 5-bit DAC allows select output voltage from 0.6V to 1V with 25mV steps and from 1V to 1.75V with 50mV steps.

L6996 is capable of supporting CPUs VID combination changing during normal operation.

The active droop allows adjust both the output load-line slope and the zero-load output voltage.

APPLICATION DIAGRAM



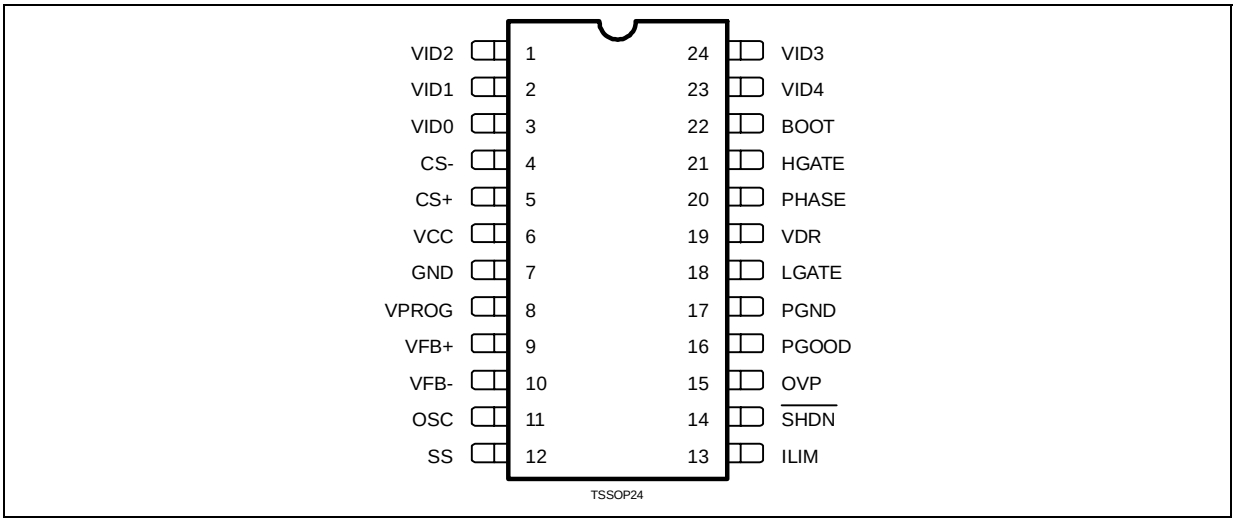
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	-0.3 to 6	V
V_{DR}	V_{DR} to GND	-0.3 to 6	V
	HGATE and BOOT, to PHASE	-0.3 to 6	V
	HGATE and BOOT, to PGND	-0.3 to 36	V
V_{PHASE}	PHASE	-0.3 to 30	V
	LGATE to PGND	-0.3 to V_{DR}+0.3	V
	ILIM, VFB+, VFB-, CS-, CS+, SHDN, VID0-4, PGOOD, OVP, VPROG to GND	-0.3 to V_{CC}+0.3	V
P_{tot}	Maximum Power dissipation at T_{amb} = 25°C	1	W
T_j	Junction operating temperature range	0 to 125	°C
T_{stg}	Storage temperature range	-55 to 125	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	125	°C/ W

PIN CONNECTION



PIN FUNCTIONS

N	Name	Description
1,2,3, 23,24	VID4-0	Voltage Identification inputs. VID0 is the LSB and VID4 is the MSB for the DAC (see VID table)
4	CS-	This pin is used for both current sensing and to detect overvoltage and undervoltage conditions.
5	CS+	Current sense pin. Overcurrent condition is detected by sensing CS+ to CS- voltage.
6	VCC	Supply voltage for analogy blocks. Connect it to 5V bus.
7	GND	Signal ground
8	VPROG	DAC output voltage. This pin provides the voltage programmed by the DAC. Connect a 10nF capacitor between this pin and GND.
9	VFB+	PWM comparator reference input. Connect this pin to VPROG. An additional external voltage divider between output and VPROG may be used to realize the active droop function.
10	VFB-	PWM comparator feedback input, to be connected to the regulated output. By inserting a resistor between this pin and the regulated output, a positive offset can be added to the output voltage.
11	OSC	Connect this pin to the battery through a voltage divider in order to provide the voltage feedforward feature.
12	SS	Soft start pin. 5µA constant current charges an external capacitor whose value sets the soft-start time.
13	ILIM	An external resistor connected between this pin and GND sets the current limit threshold.
14	$\overline{SHDN}$	ShutDown input. When connected to GND the device stops working. When high, it enables the IC operation.
15	OVP	Open drain output. The pull-down transistor is off either in OV condition or during a VID transition.
16	PGOOD	Open drain output. The pull-down transistor is on during soft-start, dynamic transitions and when an output voltage fault occurs.
17	PGND	Power Ground. This pin has to be connected close to the low side MOSFET source in order to minimize switching noise.
18	LGATE	Lower MOSFET gate driver output.
19	V_{DR}	Voltage supply for the low side internal driver.
20	PHASE	This pin provides the return path of the high side driver.
21	HGATE	High side MOSFET driver output.
22	BOOT	Bootstrap capacitor pin. The high side driver is supplied through this pin.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DR} = 5V; T_{amb} = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
Vin	Input voltage range	Vout=1V Fsw=110Khz Iout=1A	1		28	V
Vcc, V_{DR}			4.5		5.5	V
Vccoff	Turn-off voltage		4.1		4.3	V
V_{HYST}	UVLO Hysteresys		60	90	100	mV
Iqcc (V_{DR})	Quiescent current driver	VFB- > VFB+			20	µA
Iqcc (Vcc)	Quiescent current	VFB- > VFB+			600	µA
SHUTDOWN SECTION						
SHDN	SHDN Threshold		0.6		1.2	V
I_{SH} (V_{DR})	Driver quiescent current in shutdown.	SHDN to GND			5	µA
I_{SH} (Vcc)	Shut down current	SHDN to GND			15	µA
SOFT START SECTION						
I_{SS}	SS charge current		4		6	µA
	Soft-start active range			0.9		V
ON TIME						
Ton	On time duration	Vprog=CS- =1.15 Osc=250mV	720	800	880	ns
		Vprog=CS-=1.15 Osc=500mV	355	420	485	ns
		Vprog=CS-=1.15 Osc=1V	210	250	290	ns
		Vprog=CS-=1.15 Osc=2V	120	150	180	ns
OFF TIME						
	Minimum Off Time				580	ns
	K_{OSC}/T_{OFFMIN}	OSC=250mV V_{PROG}=CS-=1.15V		0.28		
DAC						
Vprog	Voltage Accuracy	VID0-4 see table 1	-1		+1	%
PWM COMPARATOR						
	Input voltage offset	V_{PROG}=1.6V=V_{FB-}	-2		+2	mV
I_{VFB-}	Input bias current (VP)	V_{VFB-} =1.6V	4	5	6	µA
CURRENT LIMIT AND ZERO CURRENT COMPARATOR						
I_{LIM}	ILIM input bias current	CS-=V_{PROG}=1.6V ILIM to GND = 120KΩ		4.95		µA
K_C	Positive and negative Current Limit factor.	R_{ILIM} = 120 KΩ	0.18	0.3	0.24	µA
PHASE-GND	Zero Crossing Comparator offset		-2		2	mV
GATE DRIVERS						
	High side rise time	V_{DR}=5V; C=7nF HGATE - PHASE from 2 to 4.5V		50	70	ns
	High side fall time			50	70	ns
	Low side rise time			50	70	ns
	Low side fall time			50	70	ns
PROTECTIONS						
OVP	Over voltage trip	CS- rising	117	120	123	%

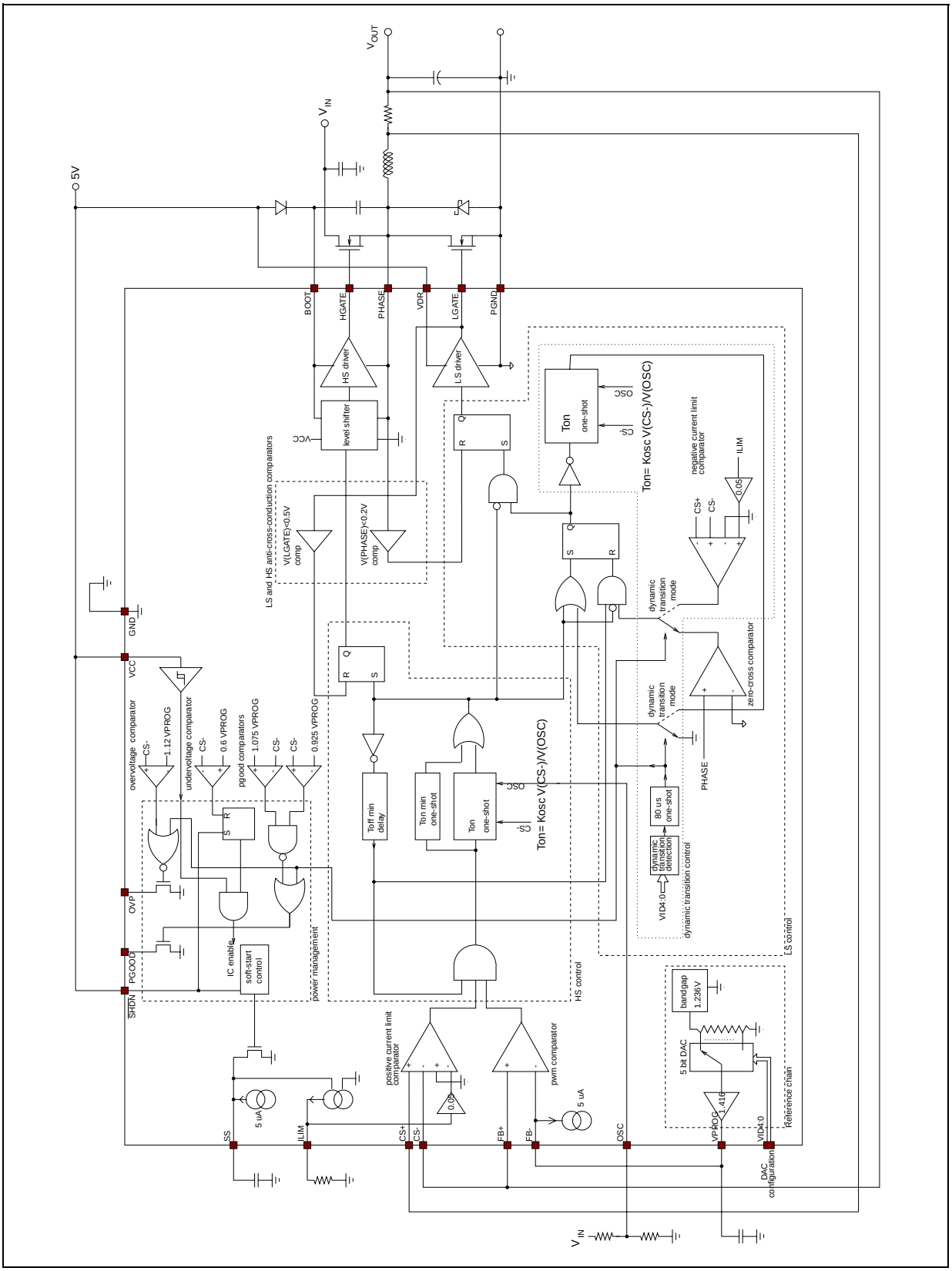
ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = V_{DR} = 5V; T_{amb} = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
UVP	Under voltage trip	CS- falling	66	69	72	%
PGOOD	Upper threshold (CS-/V_{PROG})	CS- rising; PGOOD active	109	112	115	%
PGOOD	Lower threshold (CS-/V_{PROG})	CS- falling; PGOOD active	84	87	90	%
Ron P_{GOOD}		I_{SOURCE}=2mA	40	60	100	Ω

Table 1. DAC Output Voltage

VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
1	1	1	1	1	0.600
1	1	1	1	0	0.625
1	1	1	0	1	0.650
1	1	1	0	0	0.675
1	1	0	1	1	0.700
1	1	0	1	0	0.725
1	1	0	0	1	0.750
1	1	0	0	0	0.775
1	0	1	1	1	0.800
1	0	1	1	0	0.825
1	0	1	0	1	0.850
1	0	1	0	0	0.875
1	0	0	1	1	0.900
1	0	0	1	0	0.925
1	0	0	0	1	0.950
1	0	0	0	0	0.975
0	1	1	1	1	1.000
0	1	1	1	0	1.050
0	1	1	0	1	1.100
0	1	1	0	0	1.150
0	1	0	1	1	1.200
0	1	0	1	0	1.250
0	1	0	0	1	1.300
0	1	0	0	0	1.350
0	0	1	1	1	1.400
0	0	1	1	0	1.450
0	0	1	0	1	1.500
0	0	1	0	0	1.550
0	0	0	1	1	1.600
0	0	0	1	0	1.650
0	0	0	0	1	1.700
0	0	0	0	0	1.750

Figure 1. Functional & Block Diagram



TYPICAL OPERATING CHARACTERISTICS

The test conditions refer to the component list the table 5. V_{IN} = 20V V_{OUT} = 1.8V F_{SW} = 270kHz T_{amb} = 25°C unless otherwise noted.

Figure 2. Dynamic Output Voltage Transition 1.55V -> 1.35V

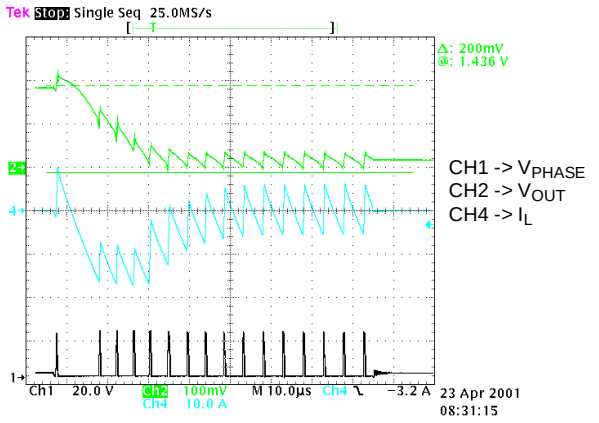


Figure 3. Dynamic Output Voltage Transition 1.35V -> 1.55V

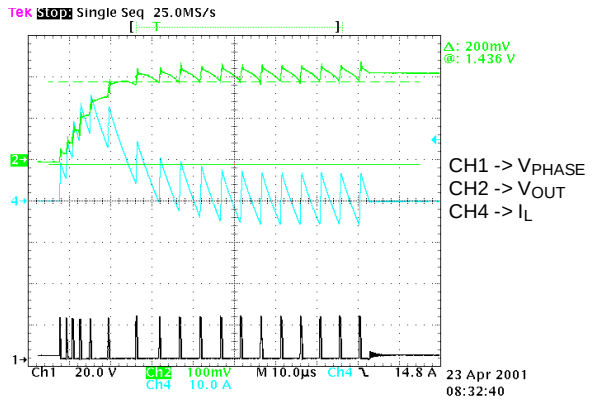


Figure 4. Load Transient 0-15A

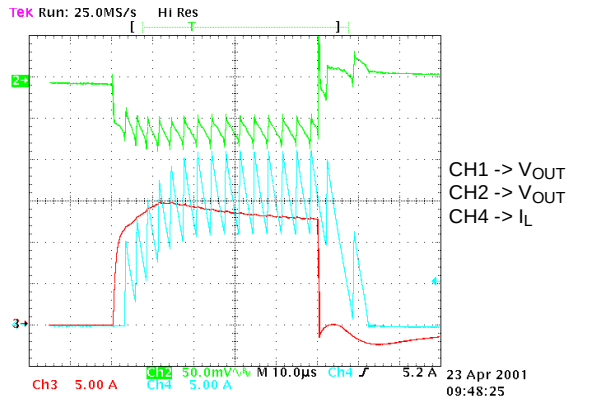


Figure 5. Startup with Zero Load

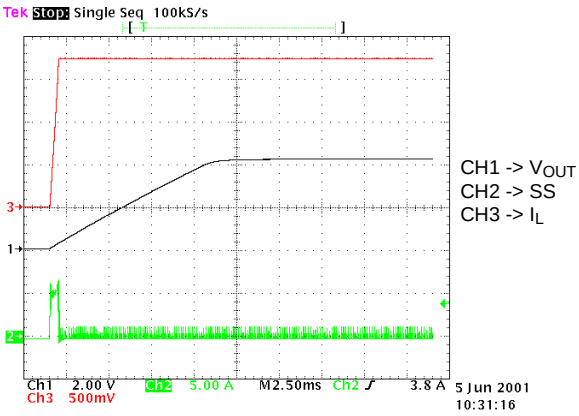


Figure 6. Startup with 10A

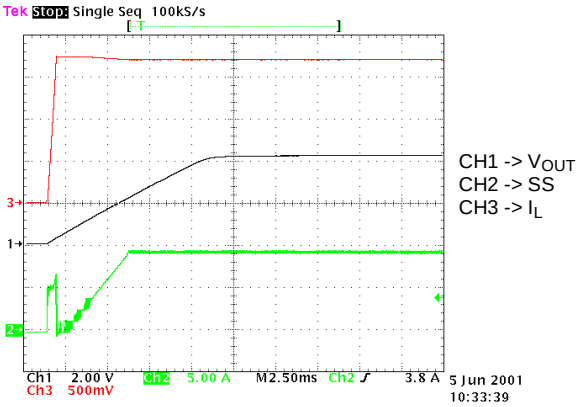


Figure 7. Test Condition: V_{in} = 20V, V5v=5V, F_{sw} = 300kHz, T_{amb} = +25°C

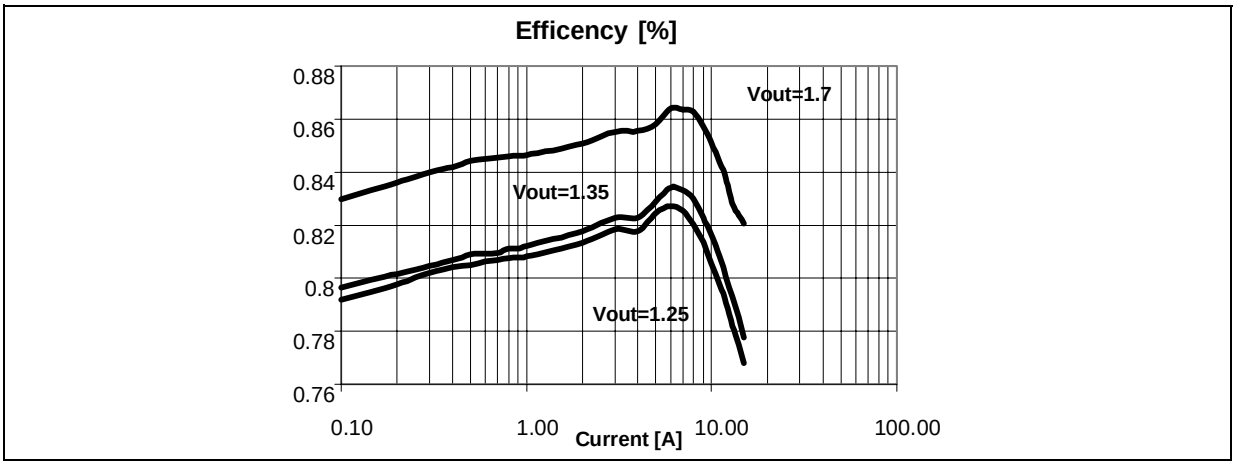


Figure 8. Test Condition: V_{out} = 1.75V, F_{sw} = 300kHz, V5v = 5V, T_{amb} = +25°C

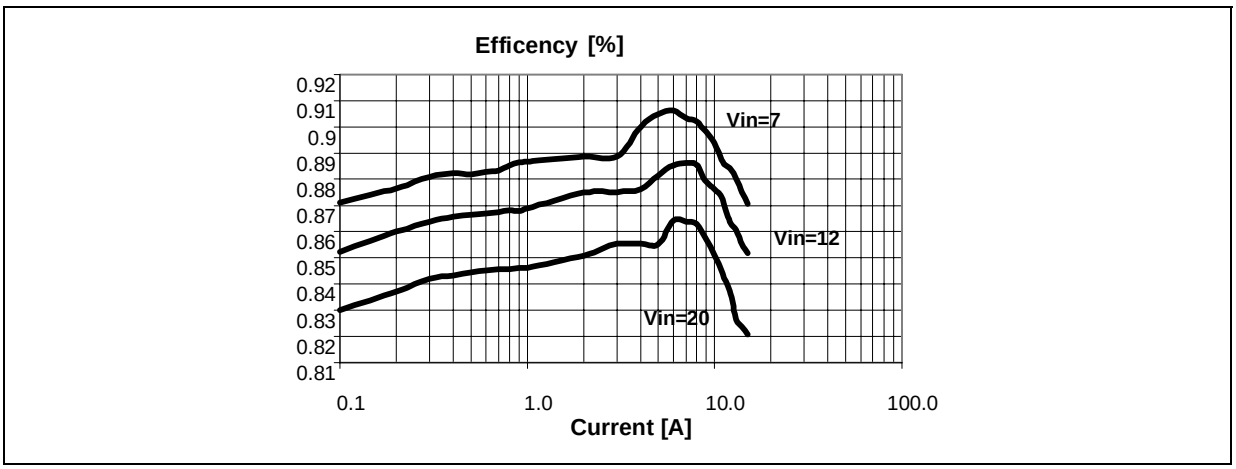


Figure 9. Test Condition: V_{out} = 1.75V, V5v = 5V, T_{amb} = +25°C

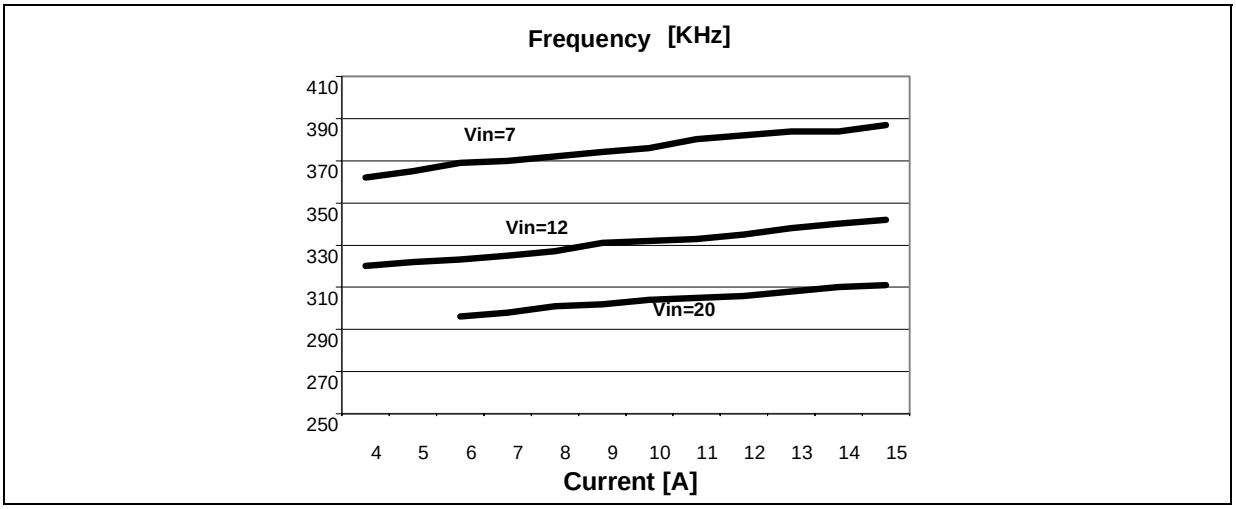


Figure 10. Typical Application with Active Voltage Droop

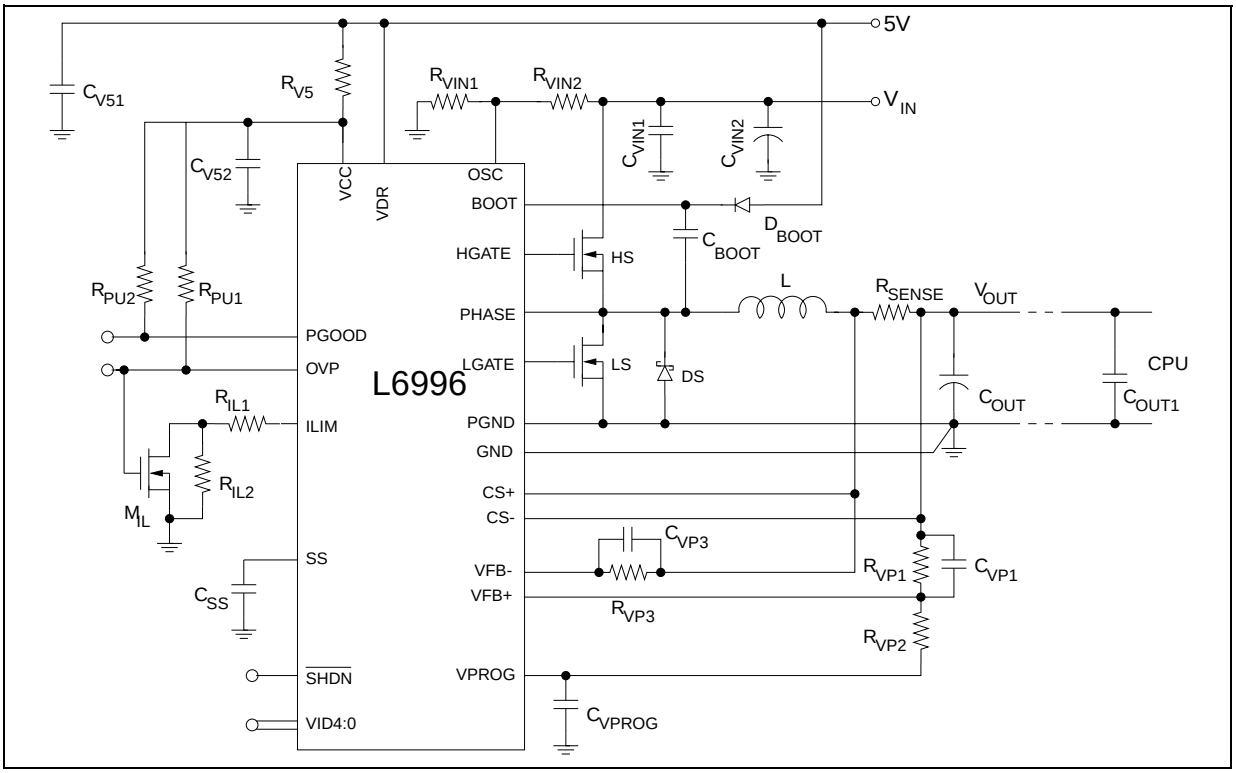
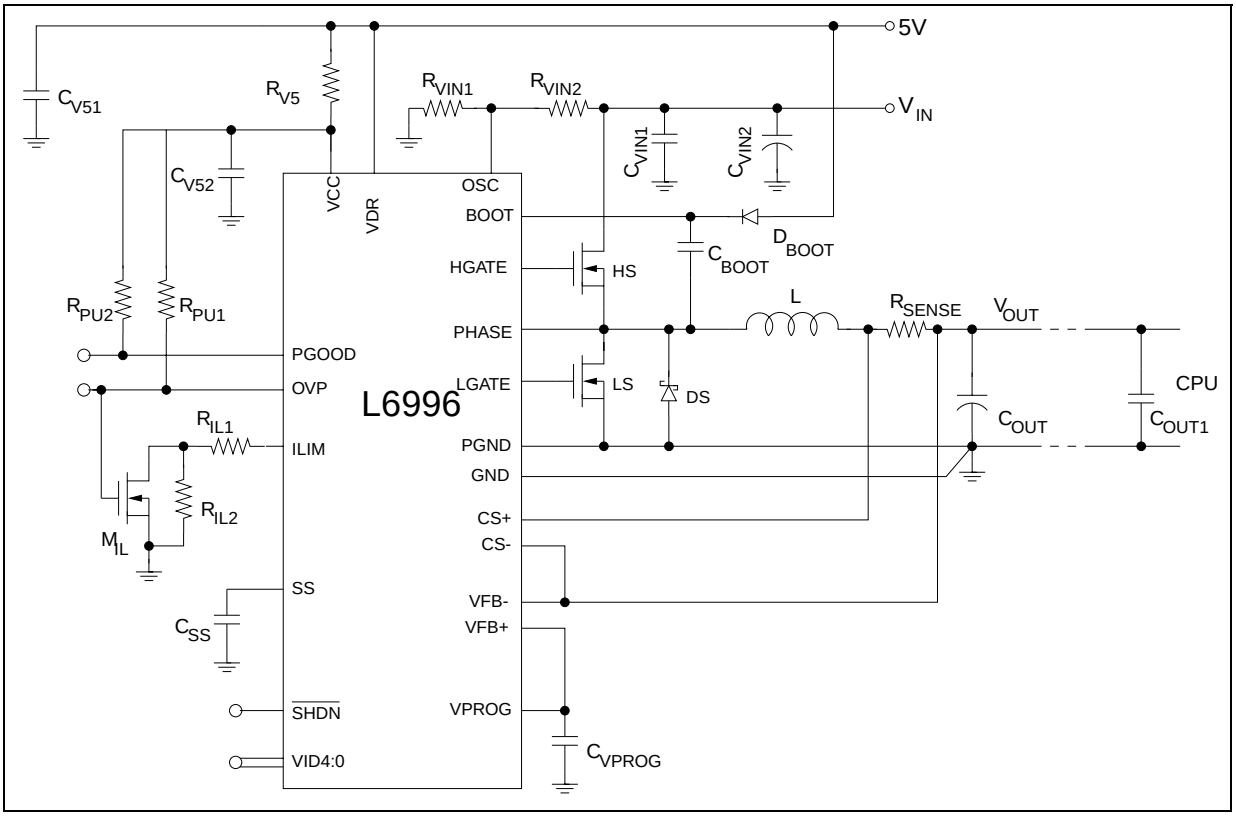


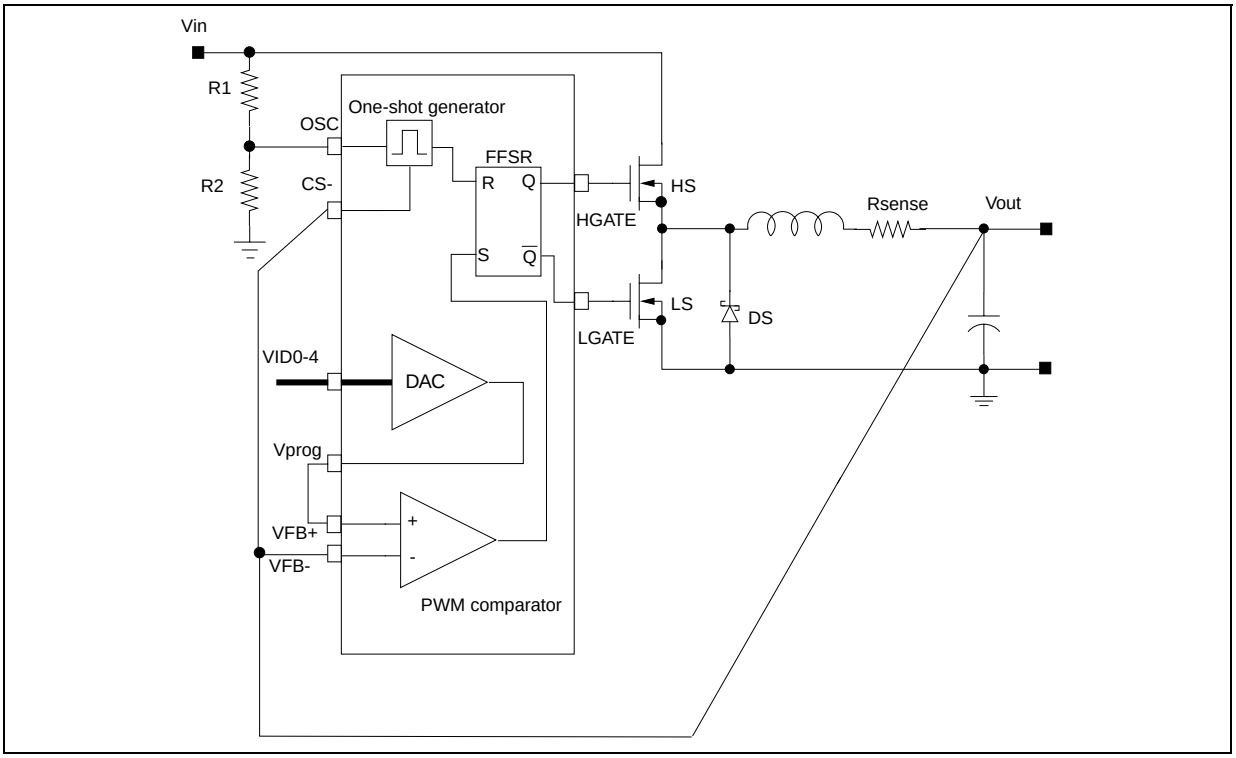
Figure 11. Typical Application without Active Voltage Droop



1 DEVICE DESCRIPTION

1.1 Constant On Time PWM Topology

Figure 12. Loop block schematic diagram



This device implements a Constant On Time control, where the Ton is the on time duration forced by a one-shot circuit. The controller calculates the one-shot time directly proportional to the V_{CS-} pin voltage and inversely to the OSC pin voltage as in Eq 1:

Eq 1
$$T_{ON} = K_{OSC}\frac{V_{CS-}}{V_{OSC}} + \tau$$

where K_{OSC}=180ns and τ is the internal propagation delay time (Typ. 40ns). The system imposes in steady state a minimum on time corresponding to V_{OSC} = 2V. In fact if the V_{OSC} voltage increases above 2V the corresponding Ton will not decrease. Connecting OSC pin to a voltage partition from V_{IN} to GND, it allows steady-state switching frequency F_{SW} independent of V_{IN}. It results:

Eq 2
$$F_{SW} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{T_{ON}} \rightarrow \alpha_{OSC} = F_{SW} \cdot K_{OSC}$$

where

Eq 3
$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}} = \frac{R_2}{R_2 + R_1}$$

The above equations allow setting the frequency divider ratio aOSC once output voltage has been set; note that such equations hold only if V_{OSC}<2.A minimum off-time constrain of about 500nS is introduced in order to assure the boot capacitor charge and to limit switching frequency after a load transient as well as to mask PWM comparator output against switching noise and spikes.

The system has not an internal clock, because this is a hysteretic controller, so the turn on pulse will start if three

conditions are met contemporarily: the PWM comparator output is low (i.e. the output voltage is below the reference voltage), the minimum off time is passed and the current limit comparator is not triggered (i.e. the inductor current is under the current limit programmed value). The voltage on the OSC pin must range between 50mV and 2V to ensure the system linearity.

1.2 Closing the loop

The loop is closed connecting the output voltage to the FB- pin. The FB- pin is linked internally to the comparator negative pin and the positive pin is connected to the programmed voltage as in Figure 12. When the FB- goes lower than FB+, the PWM comparator output goes high and sets the flip-flop output, turning on the high side MOSFET. This condition is latched to avoid noise spike. After the on-time (calculated as described in the previous section) the system resets the flip-flop and then turns off the high side MOSFET and turns on the low side MOSFET. Internally the device has more complex logic than a flip-flop to manage the transition in correct way. For more details refers to the schematic Fig. 1. Because the system implements a valley loop control, the average output voltage is different from the programmed one as shown in figure 13.

Figure 13. Valley Regulation

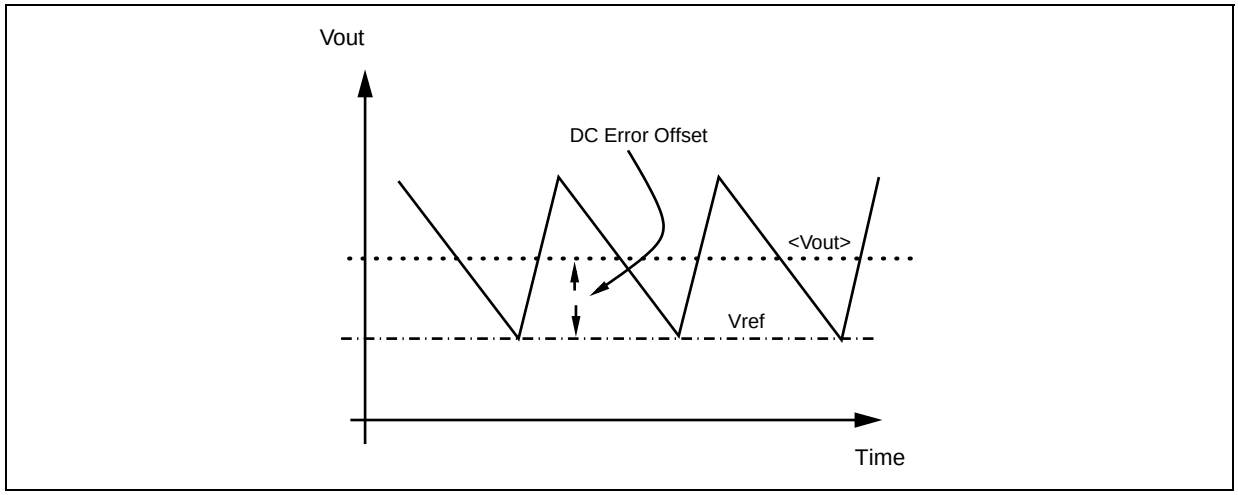
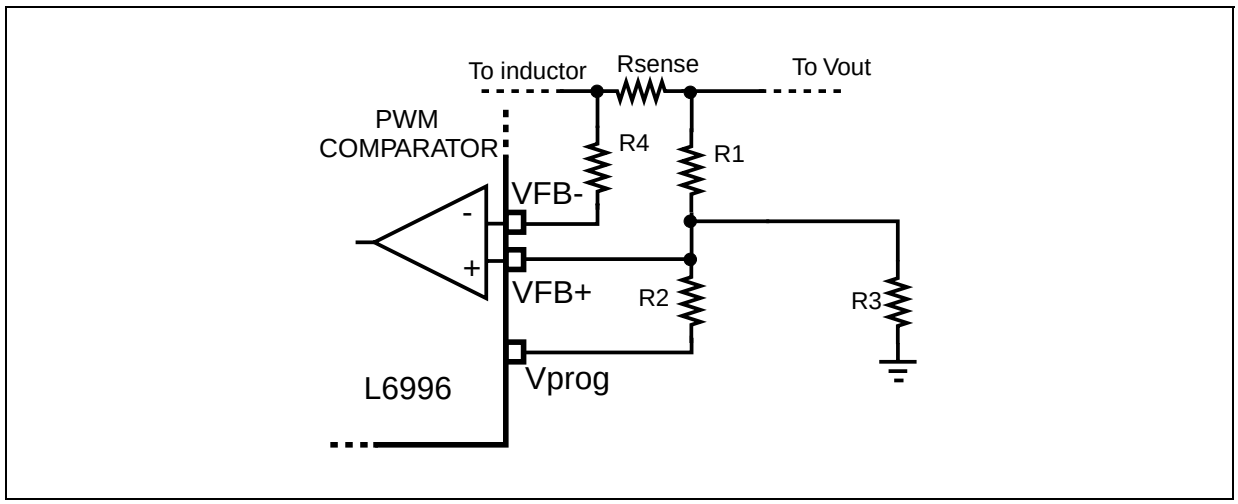


Figure 14. Voltage positioning network



The L6996 performs an externally adjustable active droop, achieving a 4m V/A load line slope using a 1.5mΩ sense resistor without use an external amplifier. Focusing the attention on the control part of the system (Figure 14), it can be considered that the inductor current can revert (the PFM function is deal towards) and the current

has an average value equal to Io. The intention is to find the output average value called $\overline{Vo}$. It is important to remember that the loop is closed a valley of the ripple, in this conditions the inputs of PWM comparator must be equal, so the VFB+ =VFB-. Suppose R4=0 and R3=open.

Considering this and watching the figure 14 it can be written two equations at the VFB+ and VFB- node:

Eq 4 $$Rsense \cdot Io = Vc$$

Eq 5 $$\frac{(V_{ovalley} - V_{prog}) \cdot R1}{R1 + R2} = Vc$$

Imposing Eq4=Eq5 it can be found the $V_{OVALLEY}$ value:

Eq 6 $$Vovalley = Vprog + Rs \cdot (1 + R1/R2) \cdot Io$$

Form Eq6 it can be noted the active drop effect due to R1, R2 resistors; it can be also noted the output average value is different from the V_{PROG} value, the error is due to the valley control, and it is equal to half of the ESR voltage ripple.

To reduce the error of the average output voltage we can change the V_{PROG} value using resistors. In fact considering the R3 resistor we can make a Thevenin equivalent:

Eq 7 $$Vprogeq = Vprog \cdot R3/(R3 + R2)$$

Eq 8 $$Req = R3//R2$$

How it can be seen the V_{PROGEQ} is less the V_{PROG} and so we can reduce the average output error. Remember that the R1, R2 and R_{SENSE} are selected in base at the Voltage Positioning needs.

The R4 resistor can be used to set also a positive offset at zero load. Considering the PWM comparator inputs:

Eq 9 $$Vo = V_{FB+} + R4 \cdot 5\mu A$$

Respect to a traditional PWM controller, that has an internal oscillator setting the switching frequency, in a hysteretic system the frequency can change with some parameters (input voltage, output current). In L6996 is implemented the voltage feed-forward circuit that allows constant switching frequency during steady-sate operation with the input voltage variation. There are many factors affecting switching frequency accuracy in steady-state operation. Some of these are internal as dead times, which depend on high side MOSFET driver. Others related to the external components as high side MOSFET gate charge and gate resistance, voltage drops on supply and ground rails, low side and high side RDS_{ON} and inductor parasitic resistance.

During a positive load transient, (the output current increases), the converter switches at its maximum frequency (the period is TON+TOFFmin) to recover the output voltage drop. During a negative load transient, (the output current decreases), the device stops to switch (high side MOSFET remains off).

1.3 Transition from PWM to PFM

To achieve high efficiency at light load conditions, PFM mode is provided. The PFM mode differs from the PWM mode essentially for the off section; the on section is the same. In PFM after a turn-on cycle the system turns-on the low side MOSFET, until the current reaches the zero A value, when the zero-crossing comparator turns off the low side MOSFET. In this way the energy stored in the output capacitor will not flow to ground, through the low side MOSFET, but it will flow to the load. In PWM mode, after a turn on cycle, the system keeps the low side MOSFET on until the next turn-on cycle, so the energy stored in the output capacitor will flow through the low side MOSFET to ground. The PFM mode is naturally implemented in hysteretic controller, in fact in PFM mode the system reads the output voltage with a comparator and then turns on the high side MOSFET when the output voltage goes down a reference value. The device works in discontinuous mode at light load and in

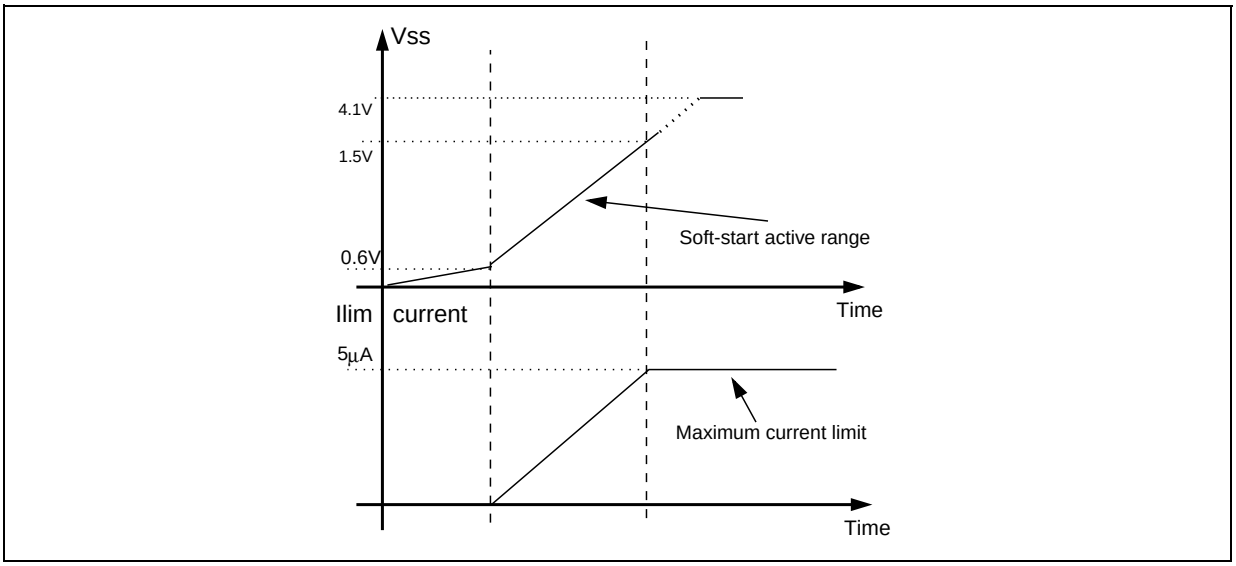
continuous mode at high load. The transition from PFM to PWM occurs when load current is around half the inductor current ripple. This threshold value depends on V_{IN}, L, and V_{OUT}. Note that the higher the inductor value is, the smaller the threshold is. On the other hand, the bigger the inductor value is, the slower the transient response is. In PFM mode the frequency changes, with the output current changing, more than in PWM mode; in fact if the output current increase, the output voltage decreases more quickly; so the successive turn-on arrives before, increasing the switching frequency. The PFM waveforms may appear more noisy and asynchronous than normal operation, but this is normal behaviour mainly due to the very low load. The NOSKIP feature cannot be disabled.

1.4 Softstart

If the supply voltages are already applied, the SHDN pin gives the start-up. The system starts with the high side MOSFET off and the low side MOSFET on. After the SHDN pin is turned on the SS pin voltage begins to increase and the system starts to switch. The softstart is realized by gradually increasing the current limit threshold to avoid output overvoltage. The active soft start range (where the output current limit increase linearly) starts from 0.6V to 1.5V. In this range an internal current source (5µA typ) charges the capacitor on the SS pin. The reference current (for the current limit comparator) forced through ILIM pin is proportional to SS pin voltage and it saturates at 5µA (typ.) when SS voltage is close to 1.5V; so the maximum current limit is active. Output protections like undervoltage is disabled until SS pin voltage reaches 1.5V, instead the overvoltage is always present.

Once the SS pin voltage reaches the 1.5V value, the voltage on SS pin doesn't impact the system operation anymore. If the SHDN pin is turned on before the supplies, the correct start-up sequence is the following: first turn-on the power section and after the logic section (V_{CC} pin).

Figure 15. Soft-start diagram



1.5 Current limit

The current limit comparator senses inductor current through the sense resistor when the low side MOSFET is on and compares this value with the ILIM pin voltage. While the current is above the prefixed value, the control inhibits the one-shot start.

To properly set the current limit threshold, it should be noted that this is a valley current limit. Average current depends on the inductor value, V_{IN} e V_{OUT}.

Eq 10 $$I_{OUTCL} = I_{MAX\_VALLEY} + \Delta I_L / 2$$

To set the current threshold, choose R_{ILIM} according to the following equation:

Eq 11 $$I_{MAX\_VALLEY} = \frac{R_{ILIM}}{R_{SENSE}} \cdot K_C$$

Where K_C is the current limit factor (0.25µA typ.). A negative current limit is also introduced during dynamic transitions, when zero-cross comparator is disabled and at the inductor current is allowed to reverse. The negative current limit is useful when performing a negative transition (that is, output voltage is reduced) to avoid too high discharging current.

Both positive and negative current limit have the same threshold; but the negative current limit can be set using the OVP signal plus a transistor, that changes during the dynamic transition, as in Fig. 16 (Q5, R11).

The system accuracy is function of the exactness of the resistance connected to I_{LIM} pin and RSENSE resistor. Moreover the voltage on ILIM pin must range between 10mV and 2V to ensure the system linearity.

1.6 Protection and fault

Sensing CS- pin voltage performs the output protection. The nature of the fault (that is, latched OV or latched UV) is given by the PGOOD and OVP pins. If the output voltage is within the 90% 110% range, PGOOD is high. If an overvoltage or an undervoltage occurs, the device is latched. low side MOSFET is turned ON and high side MOSFET off. PGOOD goes low. OVP goes high in case of overvoltage, allowing the fault nature to be detected.

To recuperate the functionality either the device must be shut down, thought the SHDN pin, or the supply has to be removed. These features are useful to protect against short-circuit (UV fault) as well as high side MOSFET short (OV fault).

1.7 Drivers

The integrated high-current drivers allow using different size of power MOSFET, maintaining fast switching transition. The driver for the high side MOSFET uses the BOOT pin for supply and PHASE pin for return (floating driver). The driver for the low side MOSFET uses the VDR pin for the supply and PGND pin for the return. The main feature is the adaptive anti-cross-conduction protection, which prevents from both high side and low side MOSFET to be on at the same time, avoiding a high current to flow from VIN to GND. When high side MOSFET is turned off the voltage on the pin PHASE begins to fall; the low side MOSFET is turned on only when the voltage on PHASE pin reaches 250mV. When low side is turned off, high side remains off until LGATE pin voltage reaches 500mV. This is important since the driver can work properly with a large range of external power MOSFETS.

The current necessary to switch the external MOSFETS flows through the device, and it is proportional to the root square of the MOSFET gate charge and the switching frequency. So the power dissipation of the device is function of the external power MOSFET gate charge and switching frequency.

Eq 12 $$P_{driver} = V_{CC} \cdot Q_{gTOT} \cdot F_{SW}$$

The maximum gate charge values for the low side and high side are given from:

Eq 13 $$Q_{MAXHS} = \frac{f_{SW0}}{f_{SW}} \cdot 75nC$$

Eq 14 $$Q_{MAXLS} = \frac{f_{SW0}}{f_{SW}} \cdot 125nC$$

Where f_{SW0} = 500kHz. The equations above are valid for T_J = 150°C. If the system temperature is lower the Q_G can be higher.

For the Low Side driver the max output gate charge meets another limit due to the internal traces degradation;

in this case the maximum value is Q_{MAXLS} = 125nC.

The low side driver has been designed to have a low resistance pull-down transistor, around 0.5 ohms. This prevents the voltage on LGATE pin raises during the fast rise-time of the pin PHASE, due to the Miller effect.

1.8 Digital to analog converter

The built-in digital to analog converter (DAC) allows the adjustment of the output voltage in correspondence to the Table1 in pag 4: from 0.6V to 1V with 25mV steps, and from 1V to 1.75V with 50mV steps. The DAC can receive the digital input from the CPU. The programmed voltage is available on VPROG pin, which is capable of sourcing or sinking up to 250µA. The internal reference accuracy is ±1%.

1.9 Dynamically changing DAC code

L6996 detects as a transition any change in VID code which duration is larger than 200ns. Then, a timer forces the chip in a 'transition state' for about 100µs. In such a state, output protections are disabled and OVP pin goes high.

Current limit threshold can be reduced during the transition state duration by using an external mos shorting part of the R_{ILIM} resistor. The MOSFET gate is driven by OVP. Reducing current limit threshold prevents from output voltage overshoot/undershoot once the new-programmed voltage has been reached (see waveforms reported below), especially when the droop is not implemented. Note that the reduced threshold must be however high enough to allow the output capacitor to charge/discharge within the transition time. During the transition state duration, zero-cross comparator is disabled and inductor current is allowed to reverse. A negative current limit is introduced. During OFF time, if inductor current is negative and reaches the threshold, low side MOSFET is forced OFF, and remain OFF, allowing negative current to flow across high side body diode, for at least T_{ON}. After then, the low side or high side turns ON again, depending on PWM comparator output. This allows switching frequency to be close to steady state frequency also when the device works in negative current limit protection.

Dynamically changing the VID code is useful for portable computers, where the CPU is supply at a higher voltage when the AC-DC adapter is plugged-in, to increase speed. A lower voltage is instead provided when only the battery powers the CPU, to save energy.

The dynamic transition is usually made at light load condition, to allow the full current to be available for charging/discharging the output capacitor:

Iout ~ 300mA

$\Delta Vout_{max}$ ~250mV

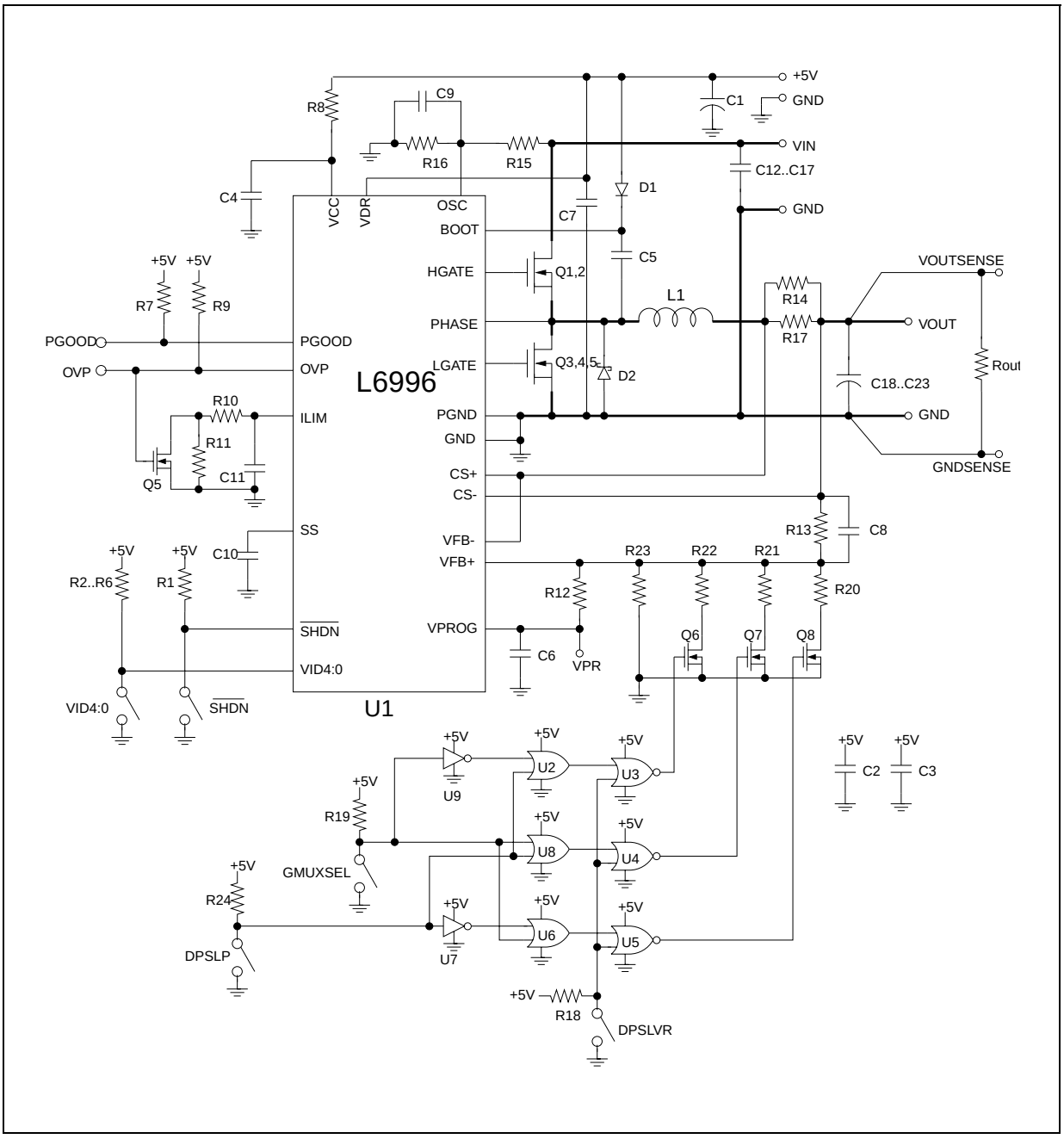
The current limit threshold should be set high enough to charge/discharge the output capacitor within the transition state duration (see below). If the output voltage changing is higher than 250mV the system can detect an overvoltage or undervoltage that can shut down the device.

2 APPLICATION INFORMATION

2.1 Demo board description

The demoboard shows the device operation in general purpose applications. The evaluation board needs two different supplies; one for the IC section (5V), and another for the conversion section (up to 28V). Output current in excess of 20A can be reached dependently on the MOSFET type. The SW1 is used to start the device (when the supplies are already present) and to select the VID code (i.e. the output voltage).

Figure 16. Schematic Diagram



2.2 Demoboard Layout

Figure 17. PCB Board Layout - Layer one (Top component side)

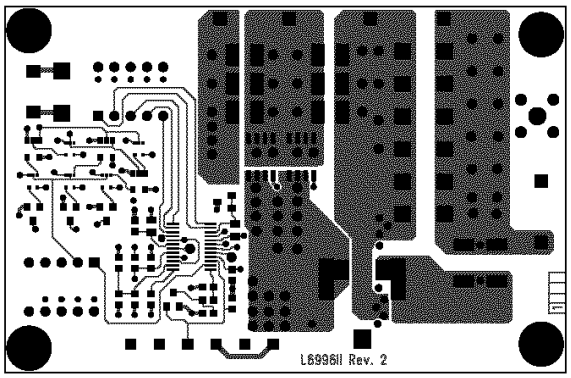


Figure 18. PCB Board Layout - Layer two (Internal Ground plane)

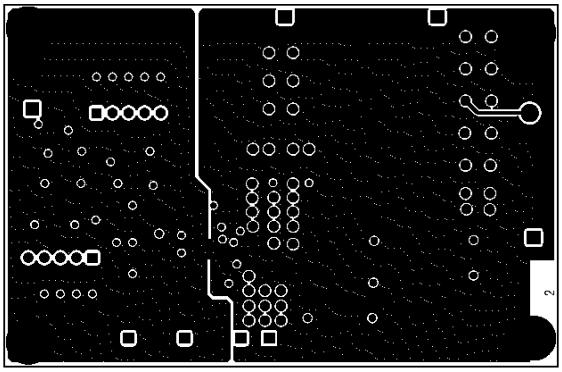


Figure 19. PCB Board Layout - Layer three (Internal signal plane)

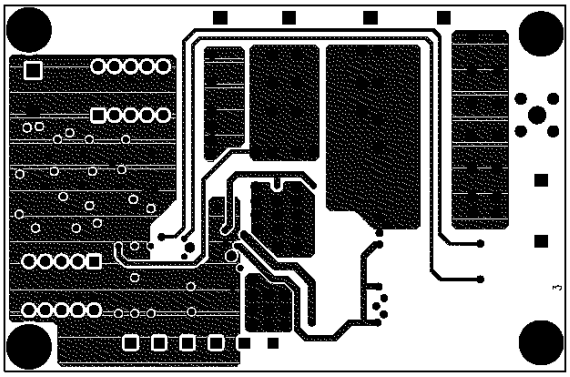


Figure 20. PCB Board Layout - Layer four (Bottom component side)

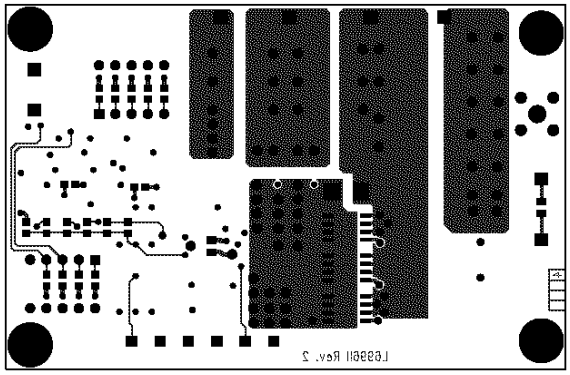


Figure 21. PCB Board Layout (Component position top view)

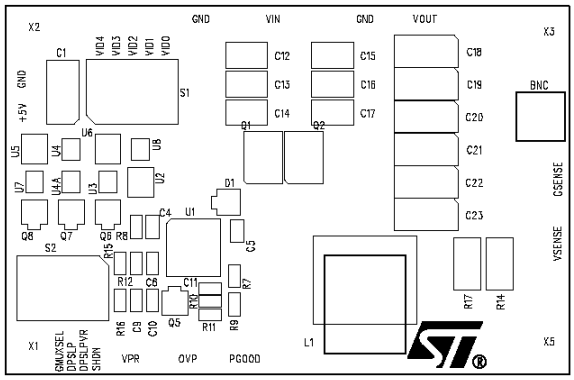


Figure 22. PCB Board Layout (Component position bottom view)

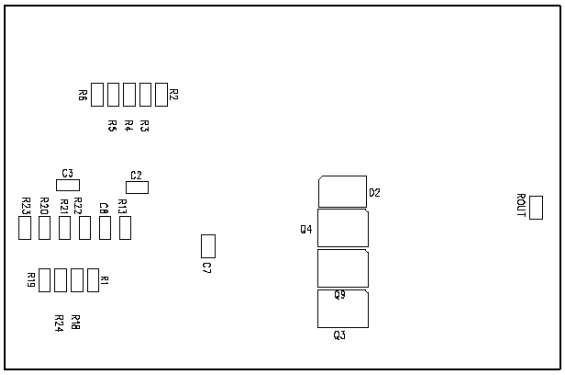


Table 2. PCB Layout guidelines

Goal	Suggestion
Low radiation and low magnetic coupling with the adjacent circuitry	1) Small switching current loop areas. (For example Placing C_{IN}, high side and Low Side MOSFET, Schottky diode, as close as possible each to others). 2) Controller placed as close as possible to the Power MOSFET. 3) Group the gate drive component (Boot cap and diode together near the IC.
Don't penalty the efficiency	Keep the power traces and load connections short and wide.
Ensure high accuracy in the current sense system	Cs+, CS- traces must be made by Kelvin connection. Also the traces should be separated from the power plane by a ground plane, run parallel.
Reduce the noise effects on IC	1) Put the feedback component (like the VP network as close as possible to the IC) 2) The feedback connection (like the FB trace, or CS+/CS- traces….) should be route as far as possible from the switching current loops. 3) Make the controller ground connection like in the figure 16.

3 DESIGN EXAMPLES

3.1 V_{IN} = 20V I_{OUT} = 23A

In this design it is considered a low profile demoboard, so a great attention is given to the components height.

3.2 Input capacitor

A pulsed current (with zero average value) flows through the input capacitor of a buck converter. The AC component of this current is quite high and dissipates a considerable amount of power on the ESR of the capacitor:

Eq 15 $$P_{CIN} = ESR_{CIN} \cdot Iout^2 \cdot \frac{Vin \cdot (Vin - Vout)}{Vin^2}$$

The I_{RMS} current is given by:

Eq 16 $$Icin_{rms} = \sqrt{Iout^2 \delta(1-\delta) + \frac{\delta}{12}(\Delta I_L)^2}$$

Neglecting the last term, the equation reduces to:

Eq 17 $$Icin_{rms} = Iout\sqrt{\delta(1-\delta)}$$

P_{CIN}, and also I_{CINRMS}, has a maximum equal to $I_{OUT}/2$ (@ $V_{IN} = 2 \times V_{OUT}$, that is, 50% duty cycle). The input, therefore, should be selected for a RMS ripple current rating as high as half the respective maximum output current. Electrolytic capacitors are the most used because are the cheapest ones and are available with a wide range of RMS current ratings. The only drawback is that, considering a requested ripple current rating, they are physically larger than other capacitors. Very good tantalum capacitors are coming available, with very low ESR and small size. The only problem is that they occasionally can burn out if subjected to very high current during the charge. So, it is better avoid this type of capacitors for the input filter of the device. In fact, they can be subjected to high surge current when connected to the power supply. If available for the requested value and voltage rating, the ceramic capacitors have usually a higher RMS current rating for a given physical size (due to the very low ESR). From the equation 17 it is found:

$$Icin_{rms} = 6.4A$$

Considering 10uF capacitors ceramic, that have ICINRMS =1.5A, 6 pzs. are needed.

3.3 Inductor selection

In order to determine the inductor value is necessary considering the maximum output current to decide the inductor current saturation. Once the inductor current saturation is found automatically it is found the inductor value also. The inductor value is important also to determine the duration of the dynamic output voltage transition. In our design it is considered a very low profile inductor.

$$L = 0.6\mu A$$

The saturation current for this choke is 25A

3.4 Output capacitors

The output capacitor is chosen by the output voltage static and dynamic accuracy. The static accuracy is related to the output voltage ripple value, while the dynamic accuracy is related to the output current load step.

If the static precision is around +/- 4% for the 1.25V output voltage, the output accuracy is ±50mV.

To determine the ESR value from the output precision is necessary before calculate the ripple current:

Eq 18 $$\Delta I = \frac{Vin - Vo}{L} \cdot \frac{Vo}{Vin} \cdot T_{sw}$$

Considering a switching frequency around 270kHz from the equation above the ripple current is around 7A.

So the maximum ESR should be:

Eq 19 $$ESR = \frac{\Delta V_{ripple}}{\frac{\Delta I}{2}} = \frac{50mV}{3.5} = 14m\Omega$$

The dynamic specifications are sometime more relaxed than the static requirements so the ESR value around 7mΩ should be enough.

Sometimes can be considered the output capacitor effect also:

Eq 20 $$\Delta Vout = \frac{Iout^2 \cdot L}{2 \cdot Vout} \cdot \frac{1}{Cout}$$

From the above equation can be calculated the minimum output capacitance value. Considering ΔV_{OUT} = 100mV, C_{OUT} > 1600µF should be used.

Five capacitor of 330µF from PANASONIC correspond to the request. To allow the device control loop to properly work, output capacitor ESR zero must be at least ten times smaller than switching frequency. Low ESR tantalum capacitors, which ESR zero is close to 10 kHz, are suitable for output filtering. Output capacitor value COUT and its series resistance, should be large enough and small enough, respectively, to keep output voltage within the accuracy range during a load transient, and to give the device a minimum signal to noise ratio.

The current ripple flows through the output capacitor, so the output capacitors should be calculated also to sustain this ripple: the RMS current value is given from Eq21.

Eq 21 $$Icout_{rms} = \frac{1}{2\sqrt{3}} \Delta I_L$$

But this is usually a negligible constrain when choosing output capacitor.

3.5 Power MOSFET and Schottky Diodes

Since a 5V bus powers the gate drivers of the device, the use of logic-level MOSFET is highly recommended, especially for high current applications. The breakdown voltage V_{BRDSS} must be greater than VINMAX with a certain margin, so the selection will address 20V or 30V devices (depends on applications).

The RDS_{ON} can be selected once the allowable power dissipation has been established. By selecting identical Power MOSFET as the main switch and the synchronous rectifier, the total power they dissipate does not depend on the duty cycle. Thus, if PON is this power loss (few percent of the rated output power), the required RDS_{ON} (@ 25 °C) can be derived from:

Eq 22
$$RDS_{ON} = \frac{P_{ON}}{Iout^2 \cdot (1 + \alpha \cdot \Delta T)}$$

α is the temperature coefficient of RDS(ON) (typically, a = $5*10^{-3}$ $°C^{-1}$ for these low-voltage classes) and T the admitted temperature rise. It is worth noticing, however, that generally the lower RDS_{ON}, the higher is the gate charge Q_G, which leads to a higher gate drive consumption. In fact, each switching cycle, a charge Q_G moves from the input source to ground, resulting in an equivalent drive current:

Eq 23
$$Iq = Qg \cdot F_{SW}$$

The Schottky diode to be placed in parallel to the synchronous rectifier must have a reverse voltage VRRM greater than VINMAX.

For this application are selected: two high side MOSFET STS11NF3LL and two STS17NF3LL for the low side section.

3.6 RSENSE selection

The droop function consists to change the output voltage changing the output current; at high output current the output voltage is lower than the reference voltage. To implement the droop function, for the high current status, we use the R_{SENSE} resistor in series to the inductor. Since inductor current can be very high, so the resistor must be capable to dissipate high power. Moreover we use the sense resistor to measure the output current for the current limit feature, so the R_{SENSE} value must be very accurate also for temperature variation. To ensure higher temperature stability it could possible to split the R_{SENSE} value. To achieve high efficiency also the R_{SENSE} value must be as low as possible, so the Active voltage droop implemented in L6996 is very useful. For this application it are selected two 3mohms resistors from PANASONIC.

3.7 VP Network Design

The voltage-positioning network is selected by the load regulation needed. In this application wit is considered 4mV/A; with a RSENSE resistor around 1.5mohms it can be used a gain around 2.66 and so a rate between R1 and R2 around 1.66 from the Eq6.

It can be selected:

R1=1.66KΩ

R2=1KΩ

A capacitor C_{VP1} is required in parallel with RVP1 to correctly compensate the network response. Its value is given by the following equation:

Eq 24
$$C_{VP1} = ESRC_{OUT} \cdot C_{OUT}\left(\frac{1}{R_{VP1}} + \frac{1}{R_{VP2}}\right)$$

where C_{OUT} is the output capacitor value. When C_{VP1} is well chosen, a step decrease of output voltage should be observed, as an effect of a step load increase. Too small or too large C_{VP1} produces overshoot or undershoot instead of a step waveform.

With our parameter:

C_{VP1} = 7.8pF

No-load offset is obtained by R_{VP3} and of a current source internally connected to VFB+ pin. Thus:

Eq 25 $$R_{VP3} = \frac{V_{OUT,\,I=0} - V_{PROG}}{I_{OFFSET}} \frac{1}{\frac{R_{VP2}}{R_{VP1}} + 1}$$

where I_{OFFSET} = 5µA.

The capacitor C_{VP3} in parallel to R_{VP3} is a filter which time constant can be the same as in Eq22, so

Eq 26 $$C_{VP3} = \frac{ESRC_{OUT} \cdot C_{OUT}}{R_{VP3}}$$

3.8 Input divider

The input divider can be selected with the Eq1, Eq2, Eq3 . Choosing a switching frequency around 270kHz it results: αOSC = 0.048.

R1 = 560KΩ

R2 = 27KΩ

3.9 Current limit resistor

From the Eq12 it can be set the current limit resistor, for the positive current limit; it results:

R10 + R11 = 120KΩ

The negative current limit is set by the time available for the negative dynamic transition; a value around 30KΩ for R10 is a match between negative peak current and time to end the dynamic transition (around 80mS).

R10=150KW

R11=30KW

3.10 Softstart capacitor

The soft start capacitor is selected once the soft start time is imposed. It can be consider a soft start time around 1ms. The soft start capacitor is given by:

Eq 27 $$C_{SS} = \frac{I_{lim} \cdot \Delta T}{\Delta V_{ss}}$$

Where ΔV_{SS} is the soft start active range and ΔT is the soft stat time. From Eq 28 results: C_{SS} = 10nF.

Table 3. Component List

The component list is shared in two sections: the first for logic and general-purpose component, the second for power section:

GENERAL PURPOSE COMPONENTS

Part name	Value	Part number	Manufacturer	Notes
R1, R2, R3, R4, R5, R6, R7, R9, R18, R19, R24	33kΩ			
R8	47kΩ			
R10	120kΩ			Current limit resistors (to set the current limit)
R11	30kΩ			
R12	1.66kΩ			Voltage positioning resistors
R13	1kΩ			
R15	560kΩ			Input resistor divider (to set the switching frequency)
R16	27kΩ			
R20	130kΩ			IMVPII resistor network
R21	39kΩ			
R22	36kΩ			
R23	270kΩ			
C1	47µF			Tantalum/SP
C2, C3	100nF			
C4	220nF			
C5	220nF			
C6	10nF			
C7	220nF			
C8	6.8nF			Voltage positioning capacitor
C9	47pF			
C10	10nF			
C11	47pF			
U2, U6, U8	Or gate	NC7SZ32M5	FAIRCHILD	Logic network
U9, U7	Inverter gate	NC7SZ04P5	FAIRCHILD	
U3,U4,U5	Nor gate	NC7SZ02P5	FAIRCHILD	
D1	BAT54A	BAT54A	PHILIPS	
Q5,Q6,Q7,Q8	BSS131	Q62702-S565	INFINEON	
SW1, SW2	DIP SWITCH		*1	

POWER SECTION

SENSE RESISTOR

Part name	Value	Part number	Manufacturer	Notes
R14, R17	3mΩ	ERJM1WSF3M0U	PANASONIC	1%

It is important, for this component, to keep in mind three factor: it must be able to dissipate high power. Again its variation with the temperature must be small and the precision must be high to ensure high precision with the ST voltage droop function.

INPUT CAPACITOR

Part name	Value	Part number	Manufacturer	Notes
C12,C13,C14,C15,C16,C17	10µF	ECJ5YB1E106M	PANASONIC	25V ceramic
	10µF	ECJ5YF1E106M	PANASONIC	25V ceramic
	10µF	C34Y5U1E106ZTE12	TOKIN	25V ceramic
	10µF	GMK325F106ZH	TAIYO-YUDEN	35V ceramic
	10µF	TMK325F106ZH	TAIYO-YUDEN	25V ceramic
	10µF	TMK432BJ106MM	TAIYO-YUDEN	25V ceramic

For this components can be useful control the temperature coefficient and the equivalent serie resistor and the voltage rated.

OUTPUT CAPACITOR

Part name	Value	Part number	Manufacturer	Notes
C18,C19,C20,C21,C22,C23	270µF	EEFUE0D271R	PANASONIC	2V
C18,C19,C20,C21,C22	330µF	EEFUE0D271R	PANASONIC	2V

For this components can be useful control the temperature coefficient and the equivalent series resistor and the voltage rated.

INDUCTOR

Part name	Value	Part number	Manufacturer	Notes
L1	0.6µF	ETQP6F0R6BFA	PANASONIC	
	0.6µF	A959AS-R60N	TOKO	
	0.6µF	CEP12D38H-0R6	SUMIDA	

For the inductor important factors are the saturation current and the equivalent series resistor (for the efficiency improvements)

POWER MOS

Part name	Value	Part number	Manufacturer	Notes
High side				
Q1, Q2	STS11NF3LL	STS11F3LL	STMicroelectronics	
	STSJ25NF3LL	STSJ25NF3LL	STMicroelectronics	
Low Side				
Q3, Q4	STS17NH3LL	STS17NH3LL	STMicroelectronics	Q5 N.M
	STS25NH3LL	STS25NH3LL	STMicroelectronics	.

Note N.M.=Not Mounted.

For the MOSFET choose is important to know the input voltage and output voltage. The MOSFET must able

dissipate high power (for switching losses or conduction losses).

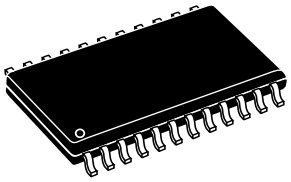
POWER DIODES

Part name	Value	Part number	Manufacturer	Notes
D2	STPS2L25U	STPS2L25U	STMICROELECTRONICS	25V

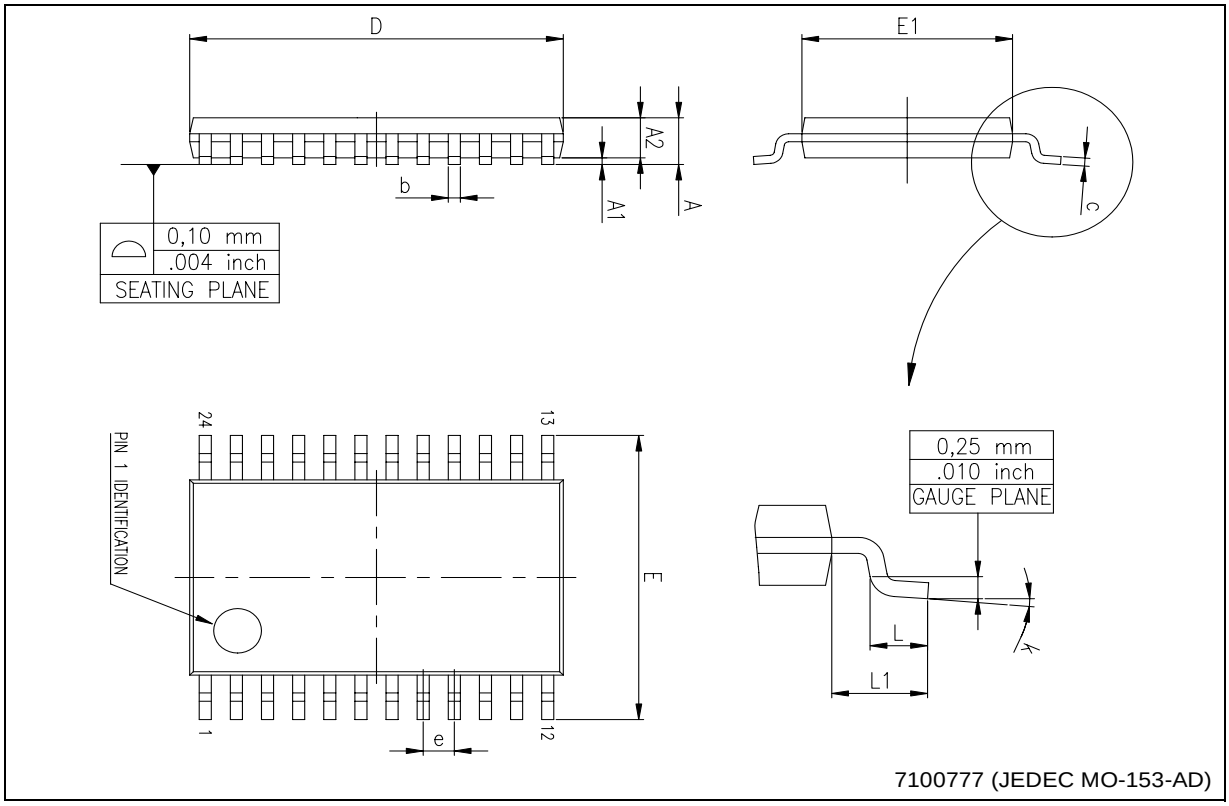
This component must have low forward voltage and must have high reverse voltage (at least equal at the input voltage).

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.003		0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E		6.40			0.252	
E1	4.30	4.40	4.50	0.170	0.173	0.177
e		0.65			0.025	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0° min., 8° max.					

OUTLINE AND MECHANICAL DATA



TSSOP24
Thin Shrink Small Outline Package



7100777 (JEDEC MO-153-AD)