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agere systems

Preliminary Data Sheet
September 2001

L9500A
High-Voltage Ringing SLIC for VoIP Applications

L9500A Introduction

The Agere Systems Inc. L9500A is a subscriber line interface circuit that is optimized for short-loop, power-sensitive applications. This device provides the complete set of line interface functionality (including power ringing) needed to interface to a subscriber loop. This device has the capability to operate with a V_{CC} supply of 3.3 V or 5 V and is designed to minimize external components required at all device interfaces. This device is optimized to interface to data over cable service interface specification (DOCSIS) compliant cable modem gateway, multi-media adaptor, and residential gateway products, such as the *Broadcom*® BCM3351, BCM3352, BCM6352, and BCM1101 and equivalent products.

Features

- Differential ringing and codec interface
- Onboard ringing generation
- Three ringing input options:
  - — Sine wave
  - — PWM
  - — Logic level square wave
- Flexible V_{CC} options:
  - — 5 V or 3.3 V V_{CC}
  - — No –5 V required
- Battery switch to minimize off-hook power
- Eight operating states:
  - — Scan mode for minimal power dissipation
  - — Forward and reverse battery active
  - — On-hook transmission states
  - — Ground start
  - — Ring mode
  - — Disconnect mode
- Ultralow on-hook power:
  - — 27 mW scan mode
  - — 38 mW active mode
- Loop start, ring trip, and ground start detection
- Software-controllable dual current limit option
- 28-pin PLCC package
- 48-pin MLCC package

Applications

- Interface to *Broadcom*:
  - — BCM3351 Cable Modem
  - — BCM3352 Cable Modem
  - — BCM6352 Integrated Multi-Media Adaptor
  - — BCM1101 Residential Gateway
- Cable Modem
- Voice over Internet Protocol (VoIP)
- Voice over DSL
- Remote Subscriber Units
- Broadband Wireless
- Short Loop Access

Description

This device is optimized to provide battery feed, ringing, and supervision on short-loop plain old telephone service (POTS) loops.

This device provides power ring to the subscriber loop through amplification of a low-voltage input. It provides forward and reverse battery feed states, on-hook transmission, a low-power scan state, ground start (tip open), and a forward disconnect state.

The device requires a V_{CC} and battery to operate. V_{CC} may be either a 5 V or a 3.3 V supply. The ringing signal is derived from the high-voltage battery. A battery switch is included to allow for use of a lower-voltage battery in the off-hook mode, thus minimizing short-loop off-hook power.

Ring mode overhead is collapsed, allowing rail-to-rail operation. In this manner, the L9500 can operate from a lower 75 V battery to minimize critical power consumption and at the same time extend subscriber ringing loop lengths to 500 Ω and beyond.

Loop closure, ring trip, and ground start detection is available. The loop closure detector has a fixed threshold with hysteresis. The ring trip detector requires a single-pole filter, thus minimizing external components required.

The dc current limit is set and fixed by a logic-controllable pin. Ground or open applied to this pin sets the current limit at the low or high value.

The device is offered with differential ringing and receive input, making it ideal for direct interface to DOCSIS compliant cable modem gateway products.

Table of Contents

Contents — Page

Table of Contents

Figures

Tables

Features

- On board balanced ringing generation:
  - — No ring relay
  - — No bulk ring generator required
  - — 15 Hz to 70 Hz ring frequency supported
  - — Sine wave input-sine wave output
  - — PWM input-sine wave output
  - — Square wave input-trapezoidal output
- Power supplies requirements:
  - — V_{CC} talk battery and ringing battery required
  - — No –5 V supply required
  - — No high-voltage positive supply required
- Flexible Vcc options:
  - — 5 V or 3.3 V V_{CC} operation
  - — 5 V or 3.3 V V_{CC} interchangeable and transparent to users
- Battery switch via logic control:
  - — Minimize off-hook power dissipation
- Minimal external components required
- Eight operating states:
  - — Forward active, V_{BAT2} applied
  - — Polarity reversal active, V_{BAT2} applied
  - — On-hook transmission, V_{BAT1} applied
  - — On-hook transmission polarity reversal, V_{BAT1} applied
  - — Ground start
  - — Scan
  - — Forward disconnect
  - — Ring mode
- Unlatched parallel data control interface
- Ultralow SLIC power:
  - — Scan 38 mW (V_{CC} = 5 V)
  - — Forward/reverse active 54 mW (V_{CC} = 5 V)
  - — Scan 27 mW (V_{CC} = 3.3 V)
  - — Forward/reverse active 41 mW (V_{CC} = 3.3 V)
- Supervision:
  - — Loop start, fixed threshold with hysteresis
  - — Ring trip, single-pole ring trip filtering, fixed threshold as a function of battery voltage
  - — Ground start fixed threshold with hysteresis
- Adjustable current limit:
  - — 25 mA or 40 mA via ground or open to control input
- Overhead voltage:
  - — Clamped typically <51 V differentially
  - — Clamped maximum <56.5 V single-ended
- Thermal shutdown protection with hysteresis
- Device interfaces:
  - — Differential receive interface
  - — Singled-ended transmit interface
  - — Differential ring input
- Package options:
  - — 28-pin PLCC
  - — 48-pin MLCC
- 90 V CBIC-S technology

Description

The L9500 is designed to provide battery feed, ringing, and supervision functions on short plain old telephone service (POTS) loops. This device is designed for ultralow power in all operating states.

The L9500 offers 8 operating states. The device assumes use of a lower-voltage talk battery, a higher-voltage ringing battery, and a V_{CC} supply.

The L9500 requires only a positive V_{CC} supply. No –5 V supply is needed. The L9500 can operate with a V_{CC} of either 5 V or 3.3 V, allowing for greater user flexibility. The choice of V_{CC} voltage is transparent to the user; the device will function with either supply voltage connected.

Two batteries are used:

1. A high-voltage ring battery (V_{BAT1}).
   V_{BAT1} is a maximum –75 V. V_{BAT1} is used for power ring signal amplification and for scan, on-hook transmission, and ground start modes. This supply is current limited to approximately the maximum power ringing current, typically 50 mA.
2. A lower-voltage talk battery (V_{BAT2}).
   V_{BAT2} is used for active mode powering.

Description (continued)

Forward and reverse battery active modes are used for off-hook conditions. Since this device is designed for short-loop applications, the lower-voltage V_{BAT2} is applied during the forward and reverse active states. Battery reversal is quiet, without breaking the ac path. Rate of battery reversal may be ramped to control switching time.

The magnitude of the overhead voltage in the forward and reverse active modes has a typical default value of 7.0 V, allowing for an on-hook transmission of an undistorted signal of 3.14 dBm into 900 Ω. Additionally, this allows sufficient overhead for 500 mV of meter pulse if desired. This overhead is fixed. The ring trip detector is turned off during active modes to conserve power.

Because on-hook transmission is not allowed in the scan mode, an on-hook transmission mode is defined. This mode is functionally similar to the active mode, except the tip ring voltage is derived from the higher V_{BAT1} rather than V_{BAT2}.

In the on-hook transmission modes with a primary battery whose magnitude is greater than a nominal 51 V, the magnitude of the tip-to-ground and ring-to-ground voltage is clamped at less than 56.5 V.

To minimize on-hook power, a low-power scan mode is available. In this mode, all functions except off-hook supervision are turned off to conserve power. On-hook transmission is not allowed in the scan mode.

In the scan mode with a primary battery whose magnitude is greater than a nominal 51 V, the magnitude of the tip-to-ground and ring-to-ground voltage is clamped at less than 56.5 V.

A forward disconnect mode is provided, where all circuits are turned off and power is denied to the loop.

The device offers a ring mode, in which a power ring signal is provided to the tip/ring pair. During the ring mode, a user-supplied, low-voltage ring signal is differentially input to the device's $RING_{IN}$ input. This signal is amplified to produce the power ring signal. This signal may be a sine wave or filtered square wave to produce a sine wave on trapezoidal output. Ring trip detector and common-mode current detector are active during the ring mode.

With maximum V_{BAT1} and a sine wave input, the L9500 has sufficient power to ring a 5 REN (1386 Ω + 40 μF) ringing load into 500 Ω of physical resistance.

This feature eliminates the need for a separate external ring relay, associated external circuitry, and a bulk ringing generator. See the Applications section of this data sheet for more information.

Both the ring trip and loop closure supervision functions are included. The loop closure has a fixed typical 10.5 mA on- to off-hook threshold in the active mode and a fixed 11.5 mA on- to off-hook threshold from the scan mode. In either case, there is a 2 mA hysteresis. The ring trip detector requires only a single-pole filter at the input, minimizing external components. The ring trip threshold at a given battery voltage is fixed. Typical ring trip threshold is 42.5 mA for a –70 V V_{BAT1}.

The device offers a ground start mode. In this mode the tip drive amplifier is turned off. The device presents a high impedance (>100 kΩ) to PT and a current limited battery (V_{BAT1}) to PR. V_{BAT1} is clamped to less than 56.5 V in this mode at PR. The NSTAT loop current detctor is used for ring ground detection. In the ground start mode, since the loop current is common mode, the loop closure threshold is reduced in half, thus maintaining loop supervision at specified levels.

Upon reaching the thermal shutdown temperature, the device will enter an all off mode. Upon cooling, the device will re-enter the state it was in prior to thermal shutdown. Hysteresis is built in to prevent oscillation.

Data control is via a parallel unlatched control scheme.

The dc current limit is fixed to either 25 mA or 40 mA depending if ground or open is applied to the V_{PROG} current limit programming pin. Programming accuracy is ±8%.

Circuitry is added to the L9500 to minimize the inrush of current from the V_{CC} supply and to the battery supply during an on- to off-hook transition, thus saving in power supply design cost. See the Applications section of this data sheet for more information.

The L9500 uses a voltage feed-current sense architecture; thus the transmit gain is a transconductance. The L9500 transconductance is set via a single external resistor, and this device is designed for optimal performance with a transconductance set at 300 V/A. This interface is single ended. The L9500 offers a differential receive interface with a gain of 8.

The L9500 is internally referenced to 1.5 V. This reference voltage is output at the V_{REF} output of the device. The SLIC output VITR is also referenced to 1.5 V. The SLIC inputs RCVP/RCVN are floating inputs.

The L9500 is packaged in a 28-pin PLCC or a 48-pin MLCC package.

Architecture Diagram

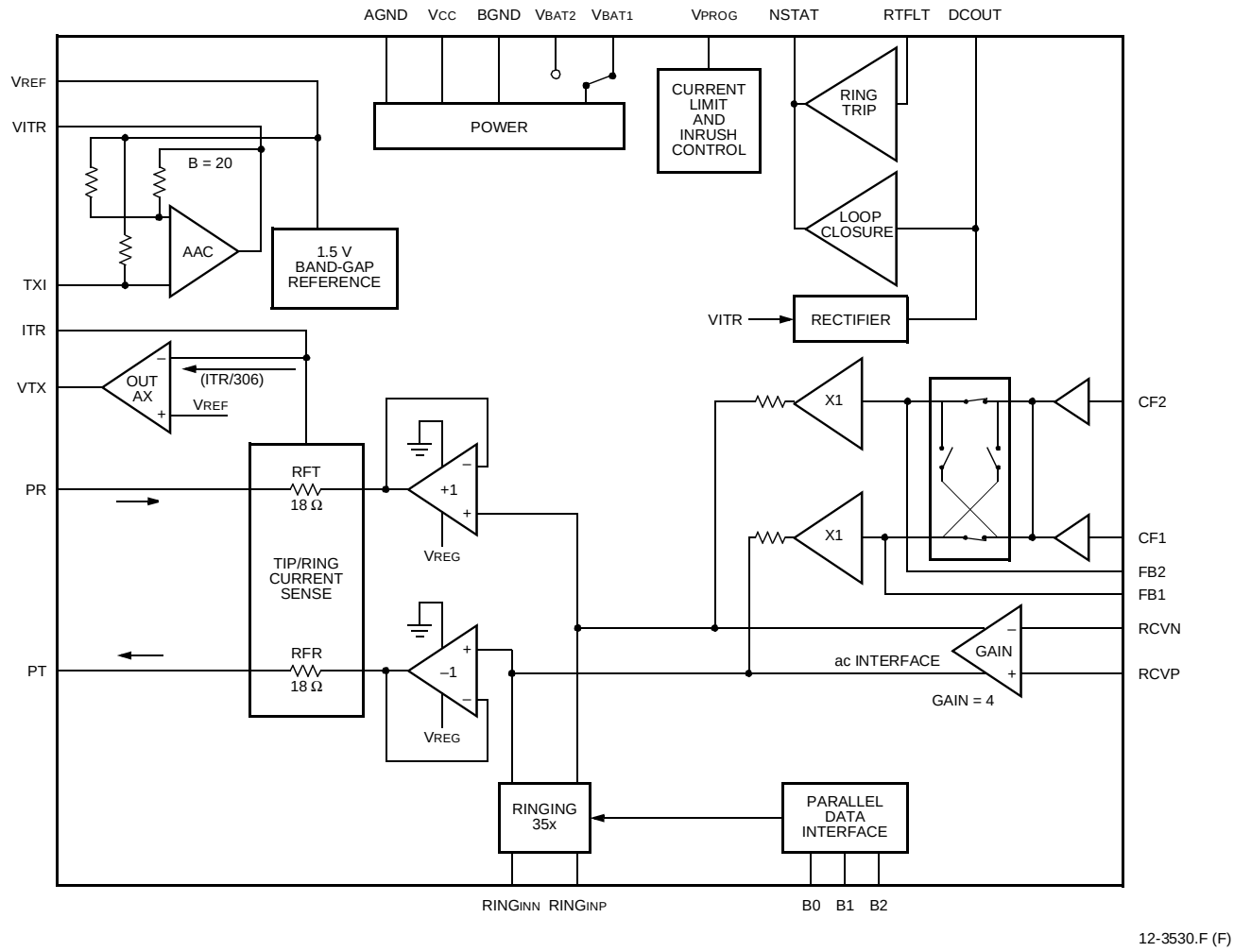

Figure 1. Architecture Diagram

Pin Information

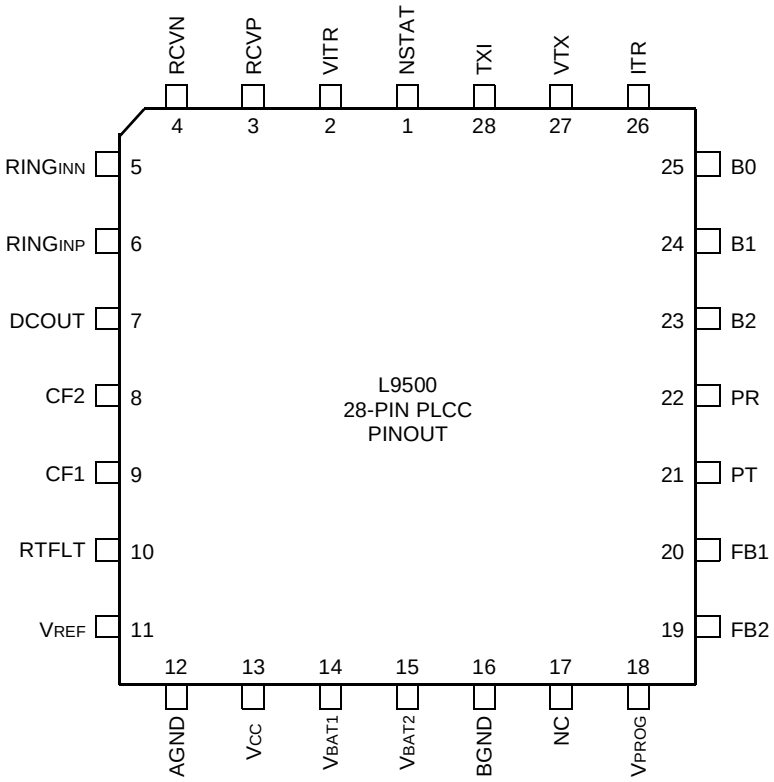

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Figure 2. 28-pin PLCC Diagram

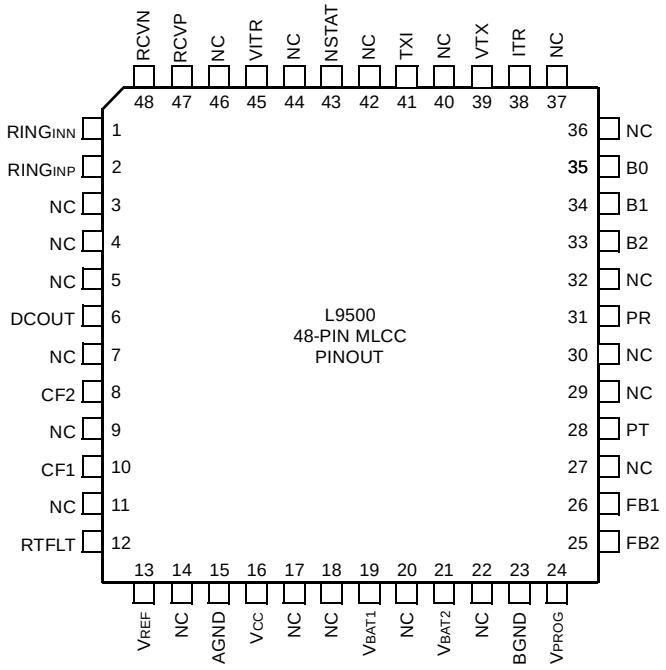

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Figure 3. 48-pin MLF Diagram

Pin Information (continued)

Table 1. Pin Descriptions

28-Pin PLCC	48-Pin MLCC	Symbol	Type	Name/Function
1	43	NSTAT	O	**Loop Closure Detector Output—Ring Trip Detector Output.** When low, this logic output indicates that an off-hook condition exists or ringing is tripped or a ring ground has occurred.
2	45	VITR	O	**Transmit ac Output Voltage.** Output of internal AAC amplifier. This output is a voltage that is directly proportional to the differential ac tip/ring current.
3	47	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls to ac differential voltage on tip and ring. This node is a floating input.
4	48	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls to ac differential voltage on tip and ring. This node is a floating input.
5	1	$RING_{INN}$	I	**Power Ring Signal Input.** Couple to a sine wave or lower crest factor low-voltage ring signal. The input here is amplified to provide the full power ring signal at tip and ring. This signal may be applied continuously, even during nonringing states.
6	2	$RING_{INP}$	I	**Power Ring Signal Input.** Couple to a sine wave or lower crest factor low-voltage ring signal. The input here is amplified to provide the full power ring signal at tip and ring. This signal may be applied continuously, even during nonringing states.
7	6	DCOUT	O	**dc Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current. This is used to set ring trip threshold.
8	8	CF2	—	**Filter Capacitor.** Connect a capacitor from this node to ground.
9	10	CF1	—	**Filter Capacitor.** Connect a capacitor from this node to CF2.
10	12	RTFLT	—	**Ring Trip Filter.** Connect this lead to DCOUT via a resistor and to AGND with a capacitor to filter the ring trip circuit to prevent spurious responses. A single-pole filter is needed.
11	13	V_{REF}	O	**SLIC Internal Reference Voltage.** Output of internal 1.5 V reference voltage.
12	15	AGND	GND	**Analog Signal Ground.**
13	16	V_{CC}	PWR	**Analog Power Supply.** User choice of 5 V or 3.3 V nominal power or supply.
14	19	V_{BAT1}	PWR	**Battery Supply 1.** High-voltage battery.
15	21	V_{BAT2}	PWR	**Battery Supply 2.** Lower-voltage battery.
16	23	BGND	GND	**Battery Ground.** Ground return for the battery supplies.
17	3, 4, 5, 7, 9, 11, 14, 17, 18, 20, 22, 27, 29, 30, 32, 36, 37, 40, 42, 44, 46	NC	—	**No Connection.**
18	24	V_{PROG}	I	**Current-Limit Program Input.** Connect ground to this pin to set current limit to 25 mA; leave this pin open to set current limit to 40 mA.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

28-Pin PLCC	48-Pin MLCC	Symbol	Type	Name/Function
19	25	FB2	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. If ramped battery reversal is not desired, this pin is left open.
20	26	FB1	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. If ramped battery reversal is not desired, this pin is left open.
21	28	PT	I/O	**Protected Tip.** The output drive of the tip amplifier and input to the loop sensing circuit. Connect to loop through overvoltage and overcurrent protection.
22	31	PR	I/O	**Protected Ring.** The output drive of the ring amplifier and input to the loop sensing circuit. Connect to loop through overvoltage and overcurrent protection.
23	33	B2	I^u	**State Control Input.** These pins have an internal 100 kΩ pull-up.
24	34	B1	I^u	**State Control Input.** These pins have an internal 100 kΩ pull-up.
25	35	B0	I^u	**State Control Input.** These pins have an internal 100 kΩ pull-up.
26	38	ITR	I	**Transmit Gain.** Input to AX amplifier. Connect a 4.75 kΩ resistor from this node to VTX to set transmit gain. Gain shaping for termination impedance with a first generation codec is also achieved with a network from this node to VTX.
27	39	VTX	O	**ac Output Voltage.** Output of internal AX amplifier. The voltage at this pin is directly proportional to the differential tip/ring current.
28	41	TXI	I	**ac/dc Separation.** Input to internal AAC amplifier. Connect a 0.1 μF capacitor from this pin to VTX.

Operating States

Table 2. Control States

B0	B1	B2	State
0	0	1	Forward active
0	1	1	Reverse active
0	0	0	On-hook transmission forward battery
0	1	0	On-hook transmission reverse battery
1	1	0	Ground start
1	0	0	Scan
1	1	1	Disconnect—device will power up in this state
1	0	1	Ring

Table 3. Supervision Coding

NSTAT
0 = off-hook or ring trip or thermal shutdown or ring ground. 1 = on-hook and no ring trip and no thermal shutdown and no ring ground.

State Definitions

Forward Active

- Pin PT is positive with respect to PR.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- Overhead is set to nominal 6.0 V for undistorted transmission of 3.14 dBm into 900 Ω.

Reverse Active

- Pin PR is positive with respect to PT.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- Overhead is set to nominal 6.0 V for undistorted transmission of 3.14 dBm into 900 Ω.

Scan

- Except for loop closure, all circuits (including ring trip and common-mode detector) are powered down.
- On-hook transmission is disabled.
- Pin PT is positive with respect to PR, and V_{BAT1} is applied to tip/ring.
- The tip to ring on-hook differential voltage will be typically between –44 V and –51 V with a –70 V primary battery.

On-Hook Transmission—Forward Battery

- Pin PT is positive with respect to PR.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is allowed.
- The tip-to-ring on-hook differential voltage will be typically between –41 V and –49 V with a –70 V primary battery.

On-Hook Transmission—Reverse Battery

- Pin PR is positive with respect to PT.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is allowed.
- The tip-to-ring on-hook differential voltage will be typically between –41 V and –49 V with a –70 V primary battery.

Disconnect

- The tip/ring amplifiers and all supervision are turned off.
- The SLIC goes into a high-impedance state.
- NSTAT is forced high (on-hook).
- Device will power up in this state.

Ring

- Power ring signal is applied to tip and ring.
- Input waveform at $RING_{IN}$ is amplified.
- Ring trip supervision and common-mode current supervision are active; loop closure is inactive.
- Overhead voltage is reduced to typically 4 V.
- Current is limited by saturation current of the amplifiers themselves, typically 100 mA at 125 °C.

Ground Start

- Tip drive amplifer is turned off.
- Device presents a high impedance (>100 kΩ) to pin PT.
- Device presents a clamped (<56.5 V) current-limited battery (V_{BAT1}) to PR.
- Output pin RGDET indicates current flowing in the ring lead.

Thermal Shutdown

- Not controlled via truth table inputs.
- This mode is caused by excessive heating of the device, such as may be encountered in an extended power-cross situation. NSTAT output is forced low or off hook during a thermal shutdown event.

Absolute Maximum Ratings (@ T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
dc Supply (V_{CC})	—	–0.5	7.0	V
Battery Supply (V_{BAT1})	—	—	–80	V
Battery Supply (V_{BAT2})	—	—	V_{BAT1}	V
Logic Input Voltage	—	–0.5	V_{CC} + 0.5	V
Logic Output Voltage	—	–0.5	V_{CC} + 0.5	V
Operating Temperature Range	—	–40	125	°C
Storage Temperature Range	—	–40	150	°C
Relative Humidity Range	—	5	95	%
PT or PR Fault Voltage (dc)	V_{PT}, V_{PR}	V_{BAT} – 5	3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	V_{BAT} – 15	15	V
Ground Potential Difference (BGND to AGND)	—	—	±1	V

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. For example, inductance in a supply lead could resonate with the supply filter capacitor to cause a destructive overvoltage.

Table 4. Recommended Operating Characteristics

Parameter	Min	Typ	Max	Unit
5 V dc Supplies (V_{CC})	—	5.0	5.25	V
3 V dc Supplies (V_{CC})	3.13	3.3	—	V
High Office Battery Supply (V_{BAT1})	–60	–70	–75	V
Auxiliary Office Battery Supply (V_{BAT2})	–12	—	V_{BAT1}	V
Operating Temperature Range	–40	25	85	°C

Table 5. Thermal Characteristics

Parameter	Min	Typ	Max	Unit
Thermal Protection Shutdown (Tjc)	150	165	—	°C
28 PLCC Thermal Resistance Junction to Ambient (θ_{JA})[1, 2]:				
Natural Convection 2S2P Board	—	35.5	—	°C/W
Natural Convection 2S0P Board	—	50.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S2P Board	—	31.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S0P Board	—	42.5	—	°C/W
48 MLF Thermal Resistance Junction to Ambient (θ_{JA})[1, 2]:	—	38	—	°C/W

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. Airflow, PCB board layers, and other factors can greatly affect this parameter.

Electrical Characteristics

Table 6. Environmental

Parameter	Min	Typ	Max	Unit
Temperature Range	–40	—	85	°C
Humidity Range[1]	5	—	95[1]	%RH

1. Not to exceed 26 grams of water per kilogram of dry air.

Table 7. 5 V Supply Currents

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 5 V.

Parameter	Min	Typ	Max	Unit
Supply Currents (scan state; no loop current):				
I_{VCC}	—	4.30	4.80	mA
I_{VBAT1}	—	0.24	0.35	mA
I_{VBAT2}	—	3	6	µA
Supply Currents (forward/reverse active; no loop current, with or without PPM, V_{BAT2} applied):				
I_{VCC}	—	5.95	7.0	mA
I_{VBAT1}	—	25	85	µA
I_{VBAT2}	—	1.2	1.40	mA
Supply Currents (on-hook transmission mode; no loop current, with or without PPM, V_{BAT1} applied):				
I_{VCC}	—	6.0	7.0	mA
I_{VBAT1}	—	1.5	1.9	mA
I_{VBAT2}	—	1.5	6	µA
Supply Currents (disconnect mode):				
I_{VCC}	—	2.7	3.75	mA
I_{VBAT1}	—	15	110	µA
I_{VBAT2}	—	3.5	25	µA
Supply Currents (ground start mode, no loop current):				
I_{VCC}	—	4.0	—	mA
I_{VBAT1}	—	0.24	—	mA
I_{VBAT2}	—	2	—	µA
Supply Currents (ring mode; no load):				
I_{VCC}	—	5.9	6.5	mA
I_{VBAT1}	—	1.8	2.2	mA
I_{VBAT2}	—	2	6	µA

Table 8. 5 V Powering

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 5 V.

Parameter	Min	Typ	Max	Unit
Power Dissipation (scan state; no loop current)	—	38	46	mW
Power Dissipation (forward/reverse active; no loop current, V_{BAT2} applied)	—	57	64	mW
Power Dissipation (on-hook transmission mode; no loop current, V_{BAT1} applied)	—	135	165	mW
Power Dissipation (disconnect mode)	—	14	23	mW
Power Dissipation (ground start mode)	—	37	—	mW
Power Dissipation (ring mode; no load)	—	156	184	mW

Electrical Characteristics (continued)

Table 9. 3.3 V Supply Currents

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 3.3 V.

Parameter	Min	Typ	Max	Unit
Supply Currents (scan state; no loop current):				
I_{VCC}	—	3.2	3.6	mA
I_{VBAT1}	—	0.24	0.35	mA
I_{VBAT2}	—	3	6	µA
Supply Currents (forward/reverse active; no loop current, V_{BAT2} applied):				
I_{VCC}	—	4.8	5.7	mA
I_{VBAT1}	—	25	85	µA
I_{VBAT2}	—	1.2	1.4	mA
Supply Currents (on-hook transmission mode; no loop current, V_{BAT1} applied):				
I_{VCC}	—	4.9	5.7	mA
I_{VBAT1}	—	1.5	1.9	mA
I_{VBAT2}	—	1.5	6	µA
Supply Currents (disconnect mode):				
I_{VCC}	—	1.8	2.5	mA
I_{VBAT1}	—	8	110	µA
I_{VBAT2}	—	2	25	µA
Supply Currents (ground start mode, no loop current):				
I_{VCC}	—	3.1	—	mA
I_{VBAT1}	—	0.24	—	mA
I_{VBAT2}	—	2	—	µA
Supply Currents (ring mode; no load):				
I_{VCC}	—	4.70	5.4	mA
I_{VBAT1}	—	1.8	2.2	mA
I_{VBAT2}	—	2	6	µA

Table 10. 3.3 V Powering

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 3.3 V.

Parameter	Min	Typ	Max	Unit
Power Dissipation (scan state; no loop current)	—	27	36.5	mW
Power Dissipation (forward/reverse active; no loop current, V_{BAT2} applied)	—	42	53	mW
Power Dissipation (on-hook transmission mode; no loop current, V_{BAT1} applied)	—	121	151	mW
Power Dissipation (disconnect mode)	—	6.5	15	mW
Power Dissipation (ground start mode)	—	27	—	mW
Power Dissipation (ring mode; no loop current)	—	141	172	mW

Electrical Characteristics (continued)

Table 11. 2-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents	105	—	—	mAp
Tip or Ring Drive Current = Ringing + Longitudinal	65	—	—	mAp
Signal Current	10	—	—	mArms
Longitudinal Current Capability per Wire (Longitudinal current is independent of dc loop current.)	8.5	15	—	mArms
Ringing Current (R_{LOAD} = 1386 Ω + 40 µF)	29	—	—	mArms
Ringing Current Limit (R_{LOAD} = 100 Ω)	—	—	50	mAp
dc Loop Current—I_{LIM} (V_{BAT2} applied, R_{LOOP} = 100 Ω):				
V_{PROG} = 0	—	25	—	mA
V_{PROG} = Open	—	40	—	mA
dc Current Variation	—	—	±8	%
dc Feed Resistance (does not include protection resistors)	—	50	—	Ω
Open Loop Voltages:				
Scan Mode:				
$\|V_{BAT1}\|$ > 51 V $\|V_{TIP}\| - \|V_{RING}\|$	44	51	—	V
PR to Battery Ground	—	—	56.5	V
PT to Battery Ground	—	—	56.5	V
OHT Mode:				
$\|V_{BAT1}\|$ > 51 V $\|V_{TIP}\| - \|V_{RING}\|$	41	49	—	V
PR to Battery Ground	—	—	56.5	V
PT to Battery Ground	—	—	56.5	V
Active Mode:				
$\|PT - PR\| - \|V_{BAT2}\|$	5.75	6.25	7.75	V
Ring Mode:				
$\|PT - PR\| - \|V_{BAT1}\|$	—	4	—	V

Electrical Characteristics (continued)

Table 11. 2-Wire Port (continued)

Parameter	Min	Typ	Max	Unit
Loop Closure Threshold:				
Active/On-hook Transmission Modes	—	10.5	—	mA
Scan Mode	—	11.5	—	mA
Loop Closure Threshold Hysteresis:				
V_{CC} = 5 V	—	2	—	mA
V_{CC} = 3.3 V	—	2	—	mA
Longitudinal to Metallic Balance at PT/PR				
Test Method: Q552 (11/96) Section 2.1.2 and *IEEE*® 455:				
300 Hz to 600 Hz	52	—	—	dB
600 Hz to 3.4 kHz	52	—	—	dB
Metallic to Longitudinal (harm) Balance:				
200 Hz to 1000 Hz	40	—	—	dB
100 Hz to 4000 Hz	40	—	—	dB
PSRR 500 Hz—3000 Hz:				
V_{BAT1}, V_{BAT2}	45	—	—	dB
V_{CC} (5 V operation)	35	—	—	dB

Table 12. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
TXI (input impedance)	—	100	—	kΩ
Output Offset (VTX)	—	—	±10	mV
Output Offset (VITR)	—	—	100	mV
Output Drive Current (VTX)	±300	—	—	µA
Output Drive Current (VITR)	±10	—	—	µA
Output Voltage Swing:				
Maximum (VTX, VITR)	AGND	—	V_{CC}	V
Minimum (VTX)	AGND + 0.25	—	V_{CC} – 0.5	V
Minimum (VITR)	AGND + 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current	—	—	±50	mA
Output Load Resistance	10	—	—	kΩ
Output Load Capacitance	—	20	—	pF
RCVN and RCVP:				
Input Voltage Range (V_{CC} = 5 V)	0	—	V_{CC} – 0.5	V
Input Voltage Range (V_{CC} = 3.3 V)	0	—	V_{CC} – 0.3	V
Input Bias Current	—	0.05	—	µA
Differential PT/PR Current Sense (DCOUT):				
Gain (PT/PR to DCOUT)	—	67	—	V/A
Offset Voltage at I_{LOOP} = 0	–10	—	10	mV

Electrical Characteristics (continued)

Table 13. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	600	1400	Ω
Total Harmonic Distortion (200 Hz—4 kHz)[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain (f = 1004 Hz, 1020 Hz)[3]:				
PT/PR Current to VITR	300 – 3%	300	300 + 3%	V/A
Receive Gain, f = 1004 Hz, 1020 Hz Open Loop				
RCVP or RCVN to PT—PR	7.76	8	8.24	—
Gain vs. Frequency (transmit and receive)[2] 600 Ω Termination, 1004 Hz, 1020 Hz reference:				
200 Hz—300 Hz	–0.3	0	0.05	dB
300 Hz—3.4 kHz	–0.05	0	0.05	dB
3.4 kHz—20 kHz	–3.0	0	0.05	dB
20 kHz—266 kHz	—	—	2.0	dB
Gain vs. Level (transmit and receive)[2] 0 dBV Reference:				
–55 dB to +3.0 dB	–0.05	0	0.05	dB
Idle-channel Noise (tip/ring) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn
Idle-channel Noise (VTX) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn

1. Set externally either by discrete external components or a third- or fourth-generation codec. Any complex impedance R1 + R2 || C between 150 Ω and 1400 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. VITR transconductance depends on the resistor from ITR to VITR. This gain assumes an ideal 4750 Ω, the recommended value. Positive current is defined as the differential current flowing from PT to PR.

Electrical Characteristics (continued)

Table 14. Logic Inputs and Outputs (V_{CC} = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.4	0.7	V
High Level	V_{IH}	2.0	2.4	V_{CC}	V
Input Current:					
Low Level (V_{CC} = 5.25 V, V_I = 0.4 V)	I_{IL}	—	—	±100	µA
High Level (V_{CC} = 5.25 V, V_I = 2.4 V)	I_{IH}	—	—	±75	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 4.75 V, I_{OL} = 360 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{CC} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Table 15. Logic Inputs and Outputs (V_{CC} = 3.3 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.2	0.5	V
High Level	V_{IH}	2.0	2.5	V_{CC}	V
Input Current:					
Low Level (V_{CC} = 3.46 V, V_I = 0.4 V)	I_{IL}	—	—	±50	µA
High Level (V_{CC} = 3.46 V, V_I = 2.4 V)	I_{IH}	—	—	±50	µA
Output Voltages (open collector with internal 60 kΩ pull-up resistor):					
Low Level (V_{CC} = 3.13 V, I_{OL} = 360 µA)	V_{OL}	0	0.2	0.5	V
High Level (V_{CC} = 3.13 V, I_{OH} = –5 µA)	V_{OH}	2.2	—	V_{CC}	V

Table 16. Ground Start

Parameter	Min	Typ	Max	Unit
Tip Open Mode—Tip Input Impedance	150	—	—	kΩ
Threshold	—	13	—	mA
Hysteresis:				
V_{CC} = 5 V	—	2	—	mA
V_{CC} = 3.3 V	—	2	—	mA

Electrical Characteristics (continued)

Table 17. Ringing Specifications

Parameter	Min	Typ	Max	Unit
$RING_{INN/P}$:				
Input Voltage Swing	0	—	V_{CC}	V
Input Impedance	—	100	—	kΩ
Ring Signal Isolation: PT/PR to VTX Ring Mode	—	60	—	dB
Ring Signal Isolation: $RING_{IN}$ to PT/PR Nonring Mode	—	80	—	dB
Ring Signal Distortion: 5 REN 1380 Ω, 40 µF Load, 100 Ω Loop	—	3	—	%
Differential Gain: $RING_{INN/P}$ to PT/PR—$VRING_{INN/P}$ = 0.7 Vp, V_{BAT1} = –70 V, R_{LOAD} = 1400 Ω	115	128	140	—

Table 18. Ring Trip

Parameter	Min	Typ	Max	Unit
Ring Trip (NSTAT = 0): Loop Resistance (total) V_{BAT1} applied	100	—	600	Ω
Ring Trip (NSTAT = 1): Loop Resistance (total) V_{BAT1} applied	—	—	10	kΩ
Trip Time (f = 20 Hz)	—	—	100	ms
Hysteresis	—	7	—	mA

Ringing will not be tripped by the following loads:

- 10 kΩ resistor in parallel with a 6 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.
- 100 Ω resistor in series with a 2 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.

Test Configurations

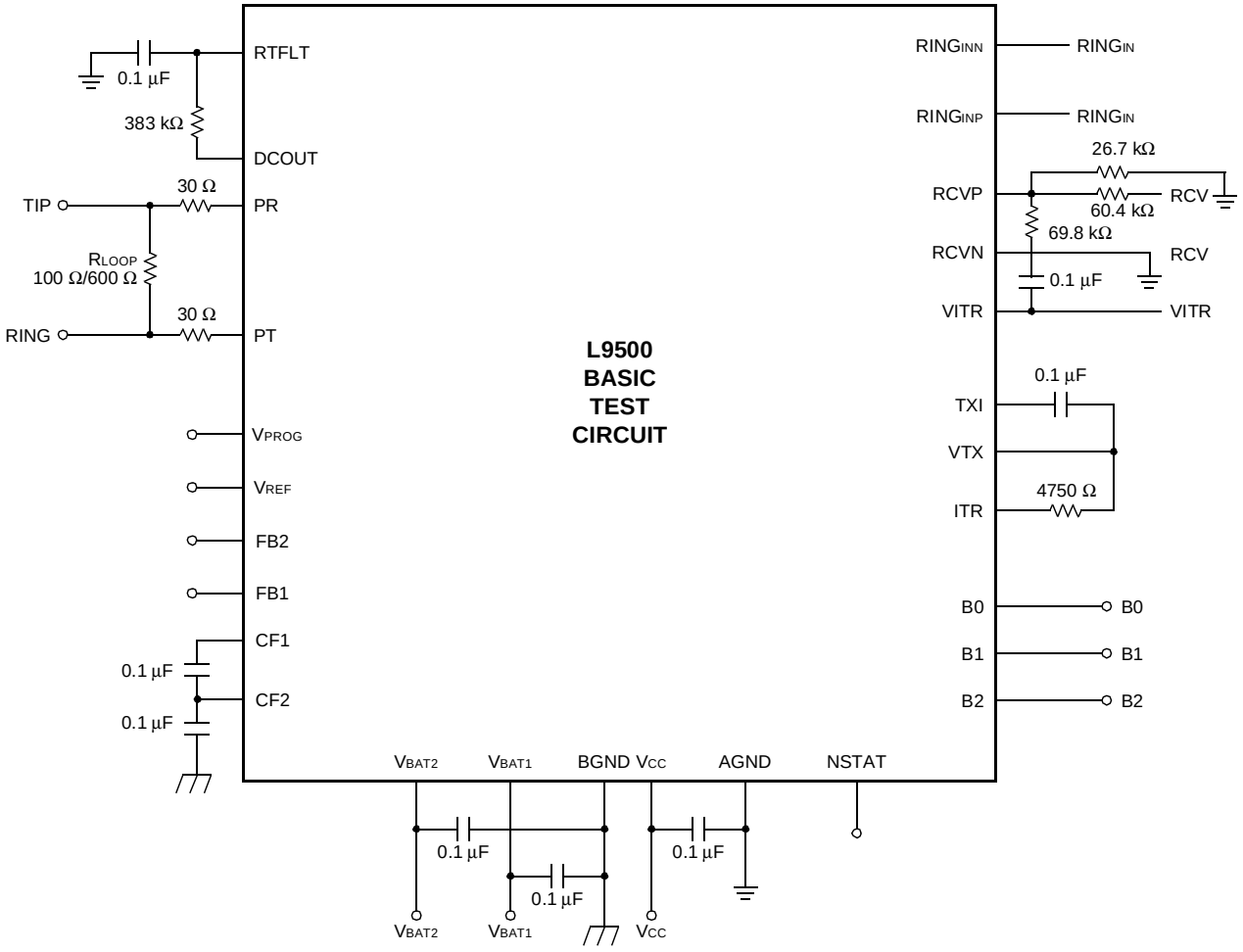


Figure 4. Basic Test Circuit

Test Configurations (continued)

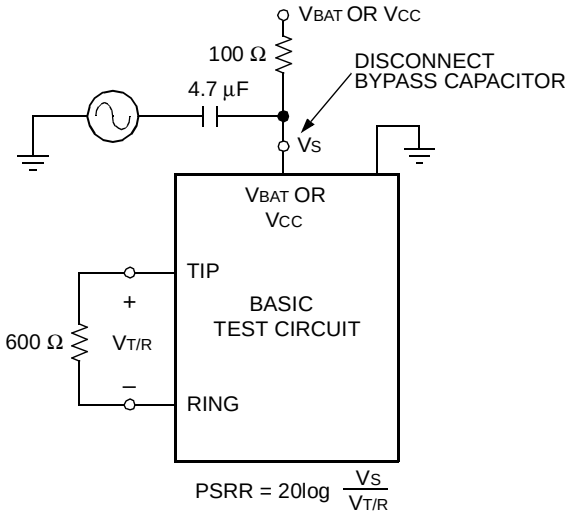


Figure 5. Metallic PSRR

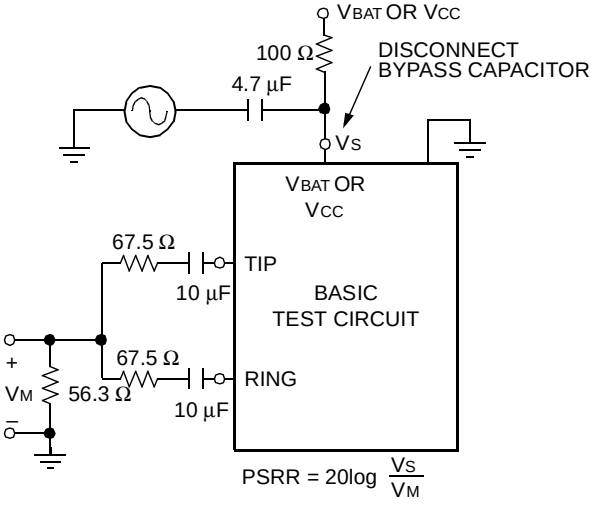


Figure 6. Longitudinal PSRR

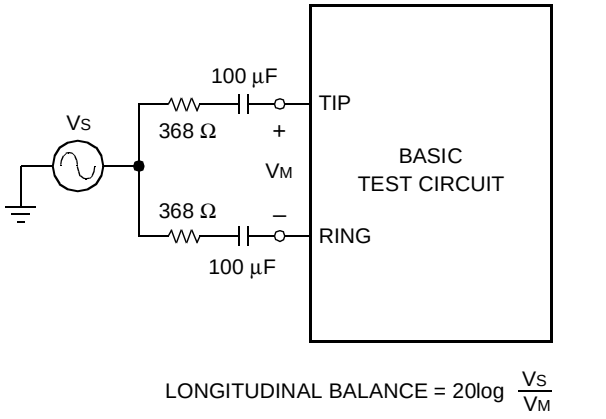


Figure 7. Longitudinal Balance

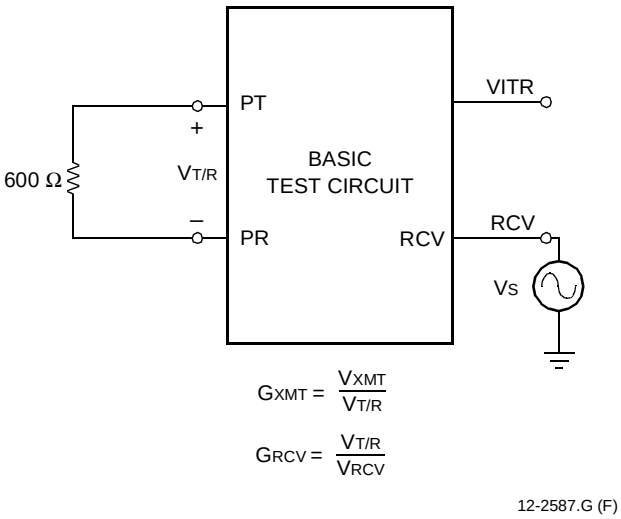


Figure 8. ac Gains

Applications

Power Control

Under normal device operating conditions, power dissipation on the device must be controlled to prevent the device temperature from rising above the thermal shutdown and causing the device to shut down. Power dissipation is highest with higher battery voltages, higher current limit, and under shorter dc loop conditions. Additionally, higher ambient temperature will also reduce thermal margin.

To support required power ringing voltages, this device is meant to operate with a high-voltage primary battery (–65 V to –75 V typically). Thus, power control is normally achieved by use of the battery switch and an auxiliary lower absolute voltage battery. Operating temperature range, maximum current limit, maximum battery voltage, minimum dc loop length and protection resistors values, airflow, and number of PC board layers will influence the overall thermal performance. The following example illustrates typical thermal design considerations.

The thermal resistance of the 28-pin PLCC package is typically 35.5 °C/W, which is representative of the natural airflow as seen in a typical switch cabinet with a multilayer board.

The L9500 will enter thermal shutdown at a typical temperature of 150°C. The thermal design should ensure that the SLIC does not reach this temperature under normal operating conditions.

For this example, assume a maximum ambient operating temperature of 85 °C, a designed current limit of 30 mA, a maximum battery of –75 V, and an auxiliary battery of –21 V. Assume a (worst-case) minimum dc loop of 20 Ω of wire resistance, 30 Ω protection resistors, and 200 Ω for the handset. Additionally, include the effects of parameter tolerance.

1. $T_{TSD} – T_{AMBIENT(max)}$ = allowed thermal rise.
   150°C – 85 °C = 65 °C.
2. Allowed thermal rise = package thermal impedance • SLIC power dissipation.
   65 °C = 35.5°C/W • SLIC power dissipation
   SLIC power dissipation (P_D) = 1.83 W.

Thus, if the total power dissipated in the SLIC is less than 1.83 W, it will not enter the thermal shutdown state. Total SLIC power is calculated as:

Total P_D = maximum battery • maximum current limit + SLIC quiescent power.

For the L9500A, the worst-case SLIC on-hook active power is 64 mW. Thus,

Total off-hook power = (I_{LOOP})(current-limit tolerance) * ($V_{BATAPPLIED}$) + SLIC on-hook power
Total off-hook power = (0.030 A)(1.08) * (21) + 75 mW
Total off-hook power = 744.4 mW

The power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

SLIC P_D = Total power – loop power
Loop off-hook power = $(I_{LOOP} * 1.08)^2$ • ($R_{LOOP(dc)}$ min + $2R_{PROTECTION}$ + $R_{HANDSET}$)
Loop off-hook power = $((0.030\ A)(1.08))^2$ • (20 Ω + 60 Ω + 200 Ω)
Loop off-hook power = 293.9 mW
SLIC off-hook power = Total off-hook power – loop off-hook power
SLIC off-hook power = 744.4 mW – 293.9 mW
SLIC off-hook power = 450.5 mW < 1.83 W

Thus, under the worst-case normal operating conditions of this example, the thermal design, using the auxiliary, is adequate to ensure the device is not driven into thermal shutdown under worst-case operating conditions.

Applications (continued)

dc Loop Current Limit

Current limit may be chosen from two discrete values, 25 mA or 40 mA, depending on if V_{PROG} is grounded (25 mA) or left floating (40 mA). Note that there is a 12.5 kΩ slope to the I/V characteristic in the current-limit region; thus, once in current limit, the actual loop current will increase slightly, as loop length decreases.

The above describes the active mode steady-state current-limit response. There will be a transient response of the current-limit circuit upon an on- to off-hook transition. Typical active mode transient current-limit response is given in Table 19.

Table 19. Typical Active Mode On- to Off-Hook Tip/ Ring Current-Limit Transient Response

Parameter	Value	Unit
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 5 ms	I_{LIM} + 60	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 50 ms	I_{LIM} + 20	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 300 ms	I_{LIM}	mA

Overhead Voltage

Active Mode

Overhead is fixed to a nominal 7.0 V, which is adequate for an on-hook transmission of 3.14 dBm into 900 Ω with additional head room for a 500 mV PPM signal.

Scan Mode

If the magnitude of the primary battery is greater than 51 V, the magnitude of the open loop tip-to-ring open loop voltage is clamped typically between 44 V and 51 V. If the magnitude of the primary battery is less than a nominal 51 V, the overhead voltage will track the magnitude of the battery voltage, i.e., the magnitude of the open circuit tip-to-ring voltage will be 4 V to 6 V less than battery. In the scan mode, overhead is unaffected by V_{OVH}.

On-Hook Transmission Mode

If the magnitude of the primary battery is greater than 51 V, the magnitude of the open loop tip-to-ring open loop voltage is clamped typically between 41 V and 49 V. If the magnitude of the primary battery is less than a nominal 51 V, the overhead voltage will track the magnitude of the battery voltage, i.e., the magnitude of the open circuit tip-to-ring voltage will be 6 V to 8 V less than battery. In the scan mode, overhead is unaffected by V_{OVH}.

Ring Mode

In the ring mode, to maximize ringing loop length, the overhead is decreased to the saturation of the tip ring drive amplifiers, a nominal 4 V. The tip to ground voltage is 1 V, and the ring to V_{BAT1} voltage is 3 V. In the ring mode, overhead is unaffected by V_{OVH}.

During the ring mode, to conserve power, the receive input at RCVN/RCVP is deactivated. During the ring mode, to conserve power, the ACC amplifier in the transmit direction at VITR is deactivated. However, the AX amplifier at VTX is active during the ring mode; differential ring current may be sensed at VTX during the ring mode.

Loop Range

The dc loop range is calculated using:

$$R_L = \frac{|V_{BAT2}| - V_{OH}}{I_{LIMIT}} - 2R_P - R_{DC}$$

V_{BAT2} is typically applied under off-hook conditions for power conservation and SLIC thermal considerations. The L9500 is intended for short-loop applications and, therefore, will always be in current limit during off-hook conditions. However, note that the ringing loop length rather than the dc loop length will be the factor to determine operating loop length.

Applications (continued)

Battery Reversal Rate

The rate of battery reverse is controlled or ramped by capacitors FB1 and FB2. A chart showing FB1 and FB2 values vs. typical ramp time is given below. Leave FB1 and FB2 open if it is not desired to ramp the rate of battery reversal.

Table 20. FB1 and FB2 Values vs. Typical Ramp Time

C_{FB1} and C_{FB2}	Transition Time
0.01 µF	20 ms
0.1 µF	220 ms
0.22 µF	440 ms
0.47 µF	900 ms
1.0 µF	1.8 s
1.22 µF	2.25 s
1.3 µF	2.5 s
1.4 µF	2.7 s
1.6 µF	3.2 s

Supervision

The L9500 offers the loop closure and ring trip supervision functions. Internal to the device, the outputs of these detectors are multiplexed into a single package output (NSTAT). The ring trip detector is valid on NSTAT during the ring mode and loop closure detector is valid on NSTAT during active and on-hook transmission modes. Additionally, common-mode current is detected for ground start applications. This status is output onto NSTAT and is valid during ground start mode.

Loop Closure

The loop closure has a fixed typical 10.5 mA on- to off-hook threshold in the active mode and a fixed 11.5 mA on- to off-hook threshold from the scan mode. In either case, there is a 2 mA hysteresis with V_{CC} = 5 V and a 2 mA hysteresis with V_{CC} = 3.3 V.

Ring Trip

The ring trip detector requires only a single-pole filter at the input, minimizing external components. An R/C combination of 383 kΩ and 0.1 µF, for a filter pole at 5.15 Hz, is recommended.

The ring trip threshold is internally fixed as a function of battery voltage and is given by:

$RT\ (mA) = 67 * \{(0.0045 * V_{BAT1}) + 0.317\}$

where:

RT is ring trip current in mA.
V_{BAT1} is the magnitude of the ring battery in V.
There is a 6 mA to 8 mA hysteresis.

Ground Start

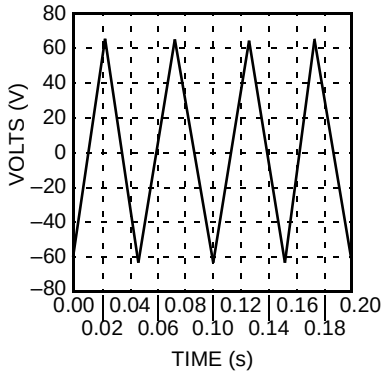
In the ground start applications, the loop closure detector detector is also used to indicate that ring-ground has occurred. During ground start mode, loop current will be common mode, rather than differential as in loop start mode. Thus, in ground start the threshold of the loop closure detector is reduced by one half the threshold seen in the loop start mode.This ouput is seen at the NSTAT output pin.

Applications (continued)

Power Ring

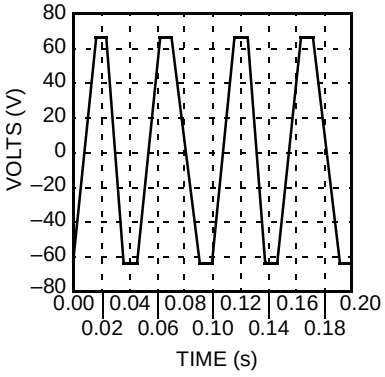
The device offers a ring mode, in which a balanced power ring signal is provided to the tip/ring pair. During the ring mode, a user-supplied low-voltage ring signal is input to the device's RINGIN input. This signal is amplified to produce the balanced power ring signal. The user may supply a sine wave input, PWM input, or a square wave to produce sinusoidal or trapezoidal ringing at tip and ring.

Various crest factors are shown below for illustrative purposes.



Note: Slew rate = 5.65 V/ms; trise = tfall = 23 ms; pwidth = 2 ms; period = 50 ms.

Figure 9. Ringing Waveform Crest Factor = 1.6



Note: Slew rate = 10.83 V/ms; trise = tfall = 12 ms; pwidth = 13 ms; period = 50 ms.

Figure 10. Ringing Waveform Crest Factor = 1.2

Sine Wave Input Signal and Sine Wave Power Ring Signal Output

The low-voltage sine wave input is applied differentially or single ended to the L9500 at pins RINGINP and RINGINN. During the ring mode, the signals at pins RINGINP and RINGINN are amplified and presented to the subscriber loop. The differential gain from RINGIN to tip and ring is a nominal 70.

When the device enters the ring mode, the tip/ring overhead set at OVH and the scan clamp circuit are disabled, allowing the voltage magnitude of the power ring signal to be maximized. Additionally, in the ring mode, the loop current limit is increased 2.5X the value set by the VPROG voltage.

The magnitude of the power ring voltage will be a function of the gain of the ring amplifier, the high-voltage battery, and the input signal at RINGIN. The input range of the signal at RINGIN is 0 V to Vcc. As the input voltage at RINGIN is increased, the magnitude of the power ring voltage at tip and ring will increase linearly, per the gain of 70, until the tip and ring drive amplifiers begin to saturate. Once the tip and ring amplifiers reach saturation, further increases of the input signal will cause clipping distortion of the power ring signal at tip and ring. The ring signal will appear balanced on tip and ring. That is, the power ring signal is applied to both tip and ring, with the signal on tip 180° out of phase from the signal on ring.

It is recommended that the input level at RINGIN be adjusted so that the power ring signal at tip and ring is just at the edge or slightly clipping. This gives maximum power transfer with minimal distortion of the sine wave. The tip side will saturate at a nominal 1 V above ground. The ring side will saturate at a nominal 3 V above battery. The input circuit for a sine wave along with waveforms to illustrate the tip and ring saturation is shown in Figure 9.

The point at which clipping of the power ring signal begins at tip and ring is a function of the battery voltage, the input capacitor at RINGIN, and the input signal at RINGIN and Vcc. During nonring modes, the sinusoidal ringing waveform may be left on at RINGIN. Via the state table, the ring signal will be removed from tip and ring even if the low-voltage input is still present at RINGIN.

Applications (continued)

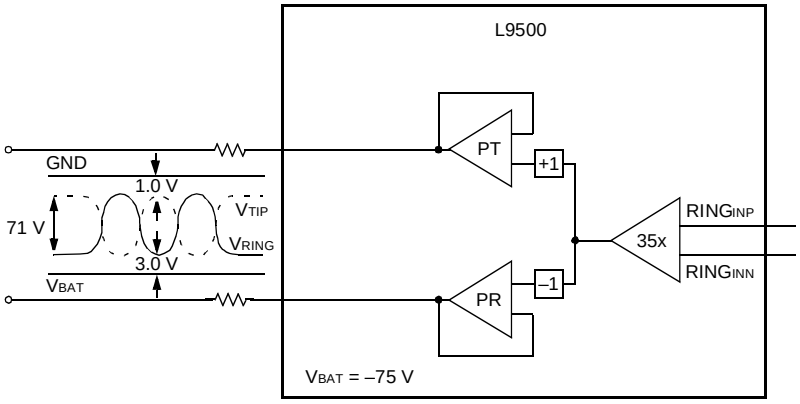


Figure 11. RINGIN Operation

ac Applications

ac Parameters

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Transmit and receive gains may be specified in terms of an actual gain, or in terms of a transmission level point (TLP), that is the actual ac transmission level in dBm. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the CODEC input.

ac Applications (continued)

Design Examples

Broadcom 3352 Interface Network

The following reference circuit shows the complete SLIC schematic for interface to the *Broadcom* BCM3352 as designed on the *Broadcom* BCM93352SV application reference design and board.

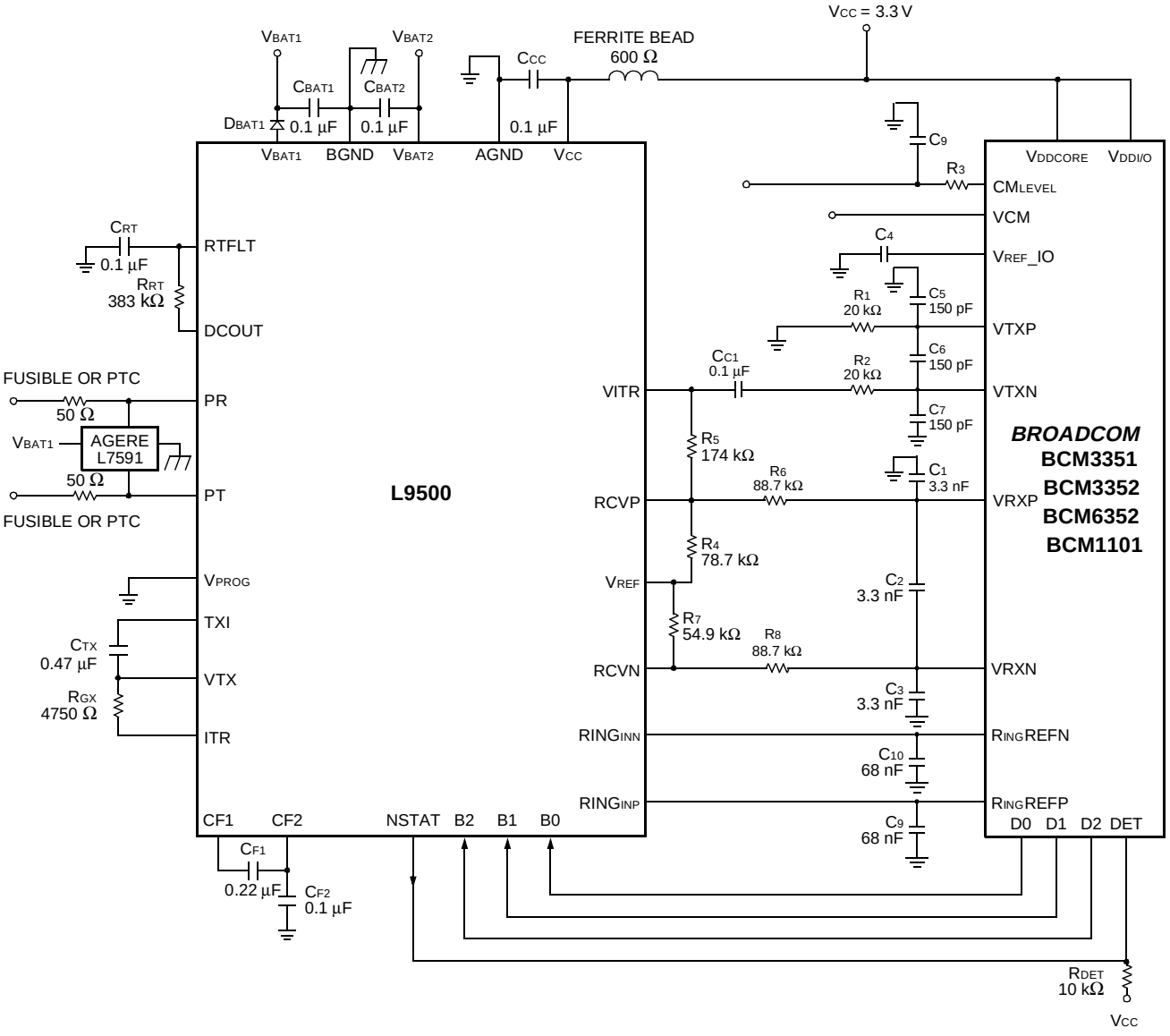


Figure 12. Reference Schematic with *Broadcom* BCM Embedded Codec Devices and Agere L9500 SLIC

ac Applications (continued)

Design Examples (continued)

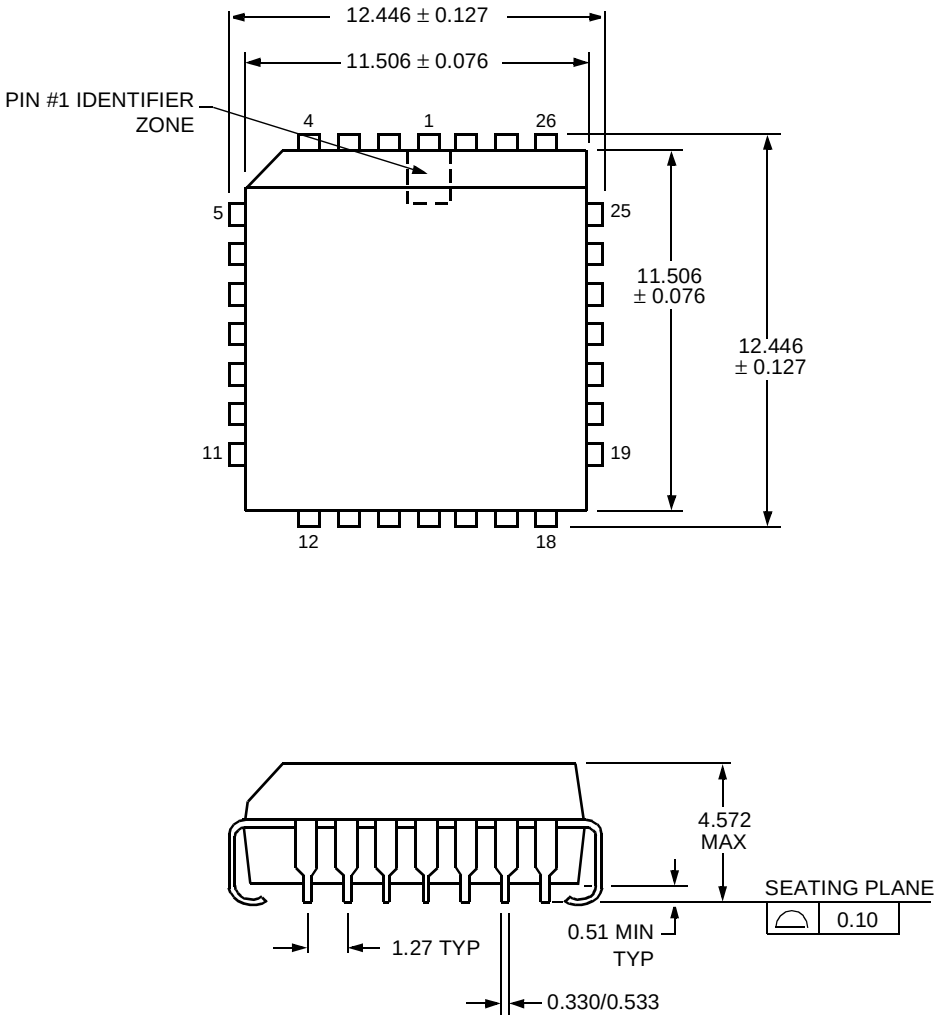
Table 21. Parts List L9500; Agere L9500 and *Broadcom* BCM3352 (per *Broadcom* BCM93552SV Application Board—SLIC Daughter Boad Components); Fully Programmable

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PT}	50 Ω	1%	Fusible or PTC	Protection resistor.
R_{PR}	50 Ω	1%	Fusible or PTC	Protection resistor.
Protector	Agere L7591	—	—	Secondary protection.
Power Supply				
C_{BAT1}	0.1 µF	20%	100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 µF	20%	50 V	V_{BAT} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{BAT1}	1N4004	—	—	Reverse current.
C_{CC}	0.47 µF	20%	10 V	Ceramic bypass capacitor.
Ferrite Bead	600 Ω, *Murata*® BLM11A601SPB	—	—	Filtering.
C_{F1}	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	0.1 µF	20%	100 V	Filter capacitor.
Ring Trip				
C_{RT}	0.1 µF	20%	10 V	Ring trip filter capacitor.
R_{RT}	383 kΩ	1%	1/16 W	Ring trip filter resistor.
ac Interface				
R_{GX}	4750 Ω	1%	1/16 W	Sets T/R to VITR transconductance.
C_{TX}	0.47 µF	20%	10 V	ac/dc separation.
C_{C1}	0.1 µF	20%	10 V	dc blocking capacitor.
R_4	78.7 kΩ	1%	1/16 W	ac interface.
R_5	174 kΩ	1%	1/16 W	ac interface.
R_6	88.7 kΩ	1%	1/16 W	ac interface.
R_7	54.9 kΩ	1%	1/16 W	ac interface.
R_8	88.7 kΩ	1%	1/16 W	ac interface.
R_{DET}	10 kΩ	1%	1/16 W	Control.

Outline Diagrams

28-Pin PLCC

Dimensions are in millimeters.



5-2506r.8(F)

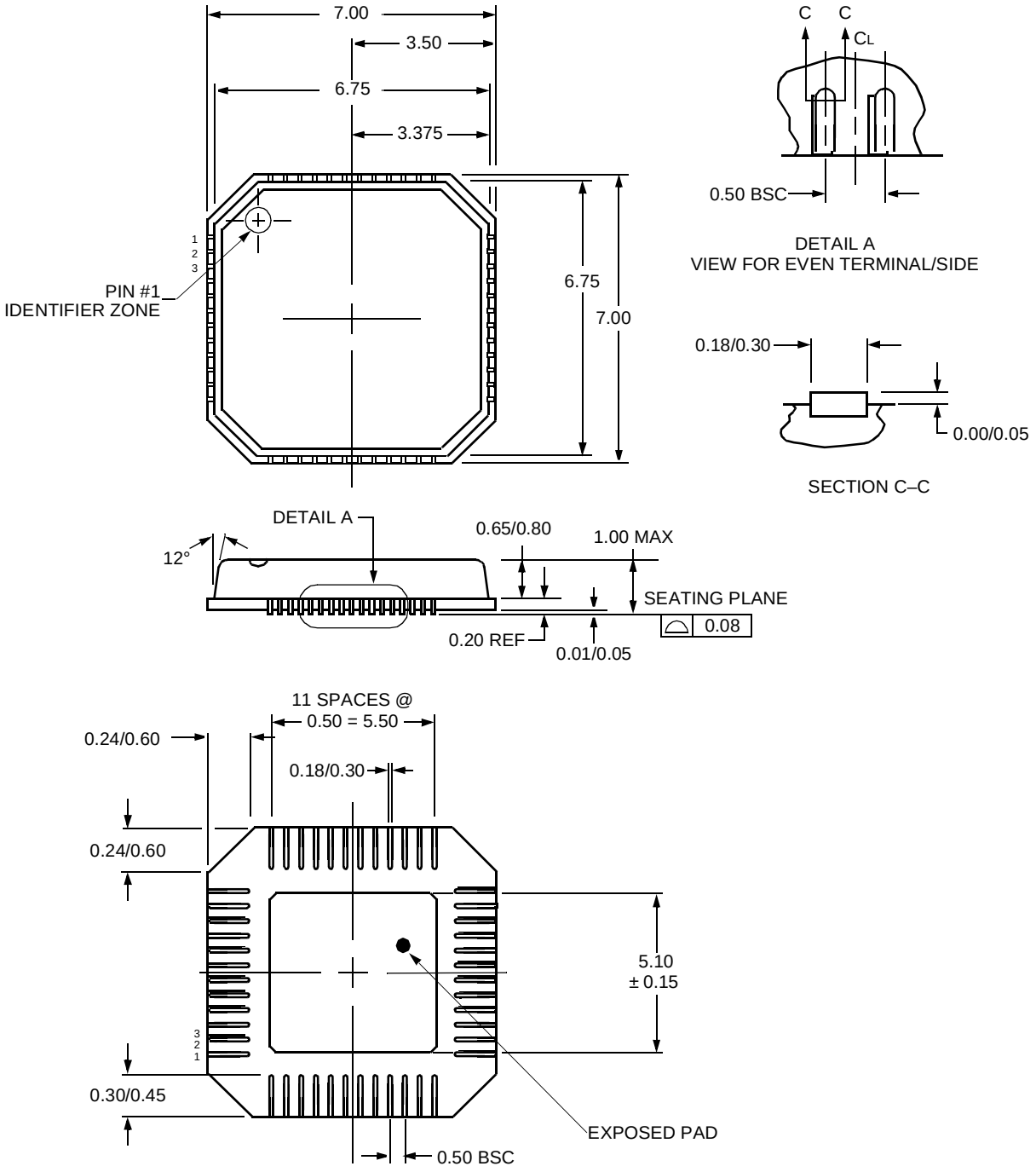
Outline Diagrams (continued)

48-Pin MLCC

Dimensions are in millimeters.

Notes: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

The exposed pad on the bottom of the package will be at V_{BAT1} potential.



0195mod

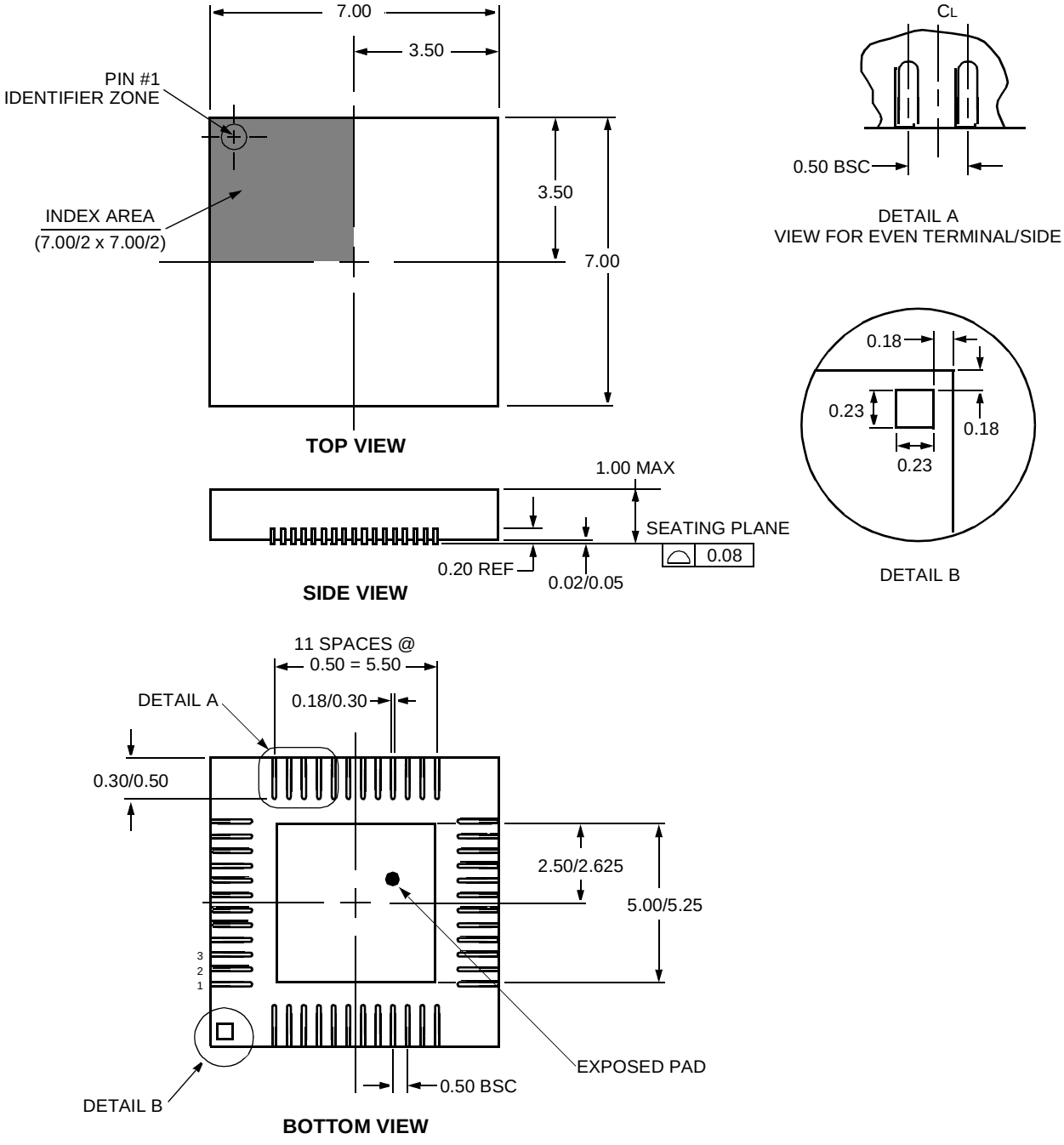
Outline Diagrams (continued)

48-Pin MLCC, JEDEC MO-220 VKKD-2

Dimensions are in millimeters.

Notes: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

The exposed pad on the bottom of the package will be at V_{BAT1} potential.



0195a

Ordering Information

Device Part Number	Description	Package	Comcode
LUCL9500AGF-D	SLIC	28-Pin PLCC, dry-bagged	108955501
LUCL9500AGF-DT	SLIC	28-Pin PLCC, dry-bagged, tape and reel	108955519
LUCL9500ARG-D	SLIC	48-Pin MLF, dry-bagged	108955485

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