

Ordering number : EN5661

Monolithic Linear IC



LA4585M

3-V Preamplifier + Power Amplifier for Headphone Stereo Products

Overview

The LA4585M is a preamplifier plus power amplifier IC that supports auto-reverse and was developed for use in 3-V headphone stereo products.

Features

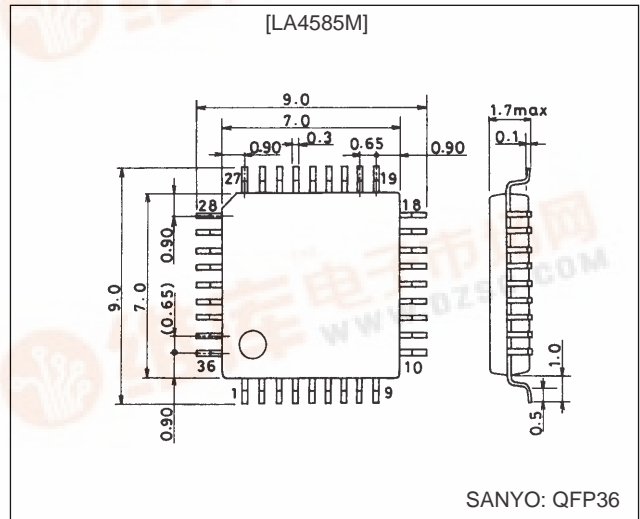
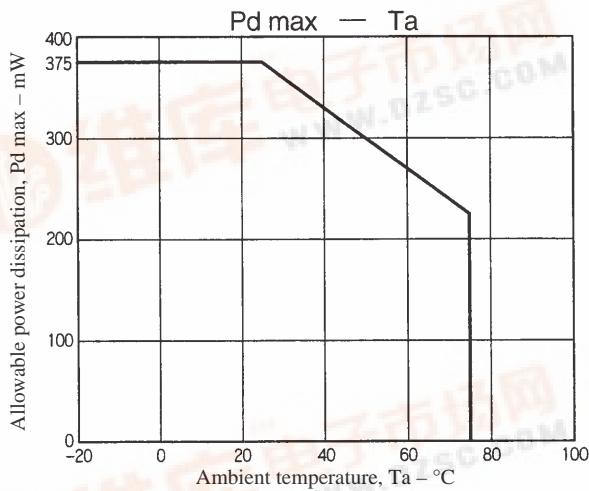
- The LA4585M is designed for use in playback-only compact cassette players. In addition to preamplifier and power amplifier functions, the LA4585M also provides low boost and automatic power output limiter (PVSS:Peak Volume Select System) functions.

- Provided in a mini-flat 36-pin quad package (0.65 mm lead pitch) optimal for miniature end products.
- Two auto-reverse playback preamplifiers
- Two headphone power amplifiers (16 Ω)
- Low boost function (auto-loudness effect)
- Output limiter function (PVSS)
- Two radio input switches (pre-muting switches)
- Power muting switch

Package Dimensions

unit: mm

3162B-QFP36



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		4.5	V
Allowable power dissipation	Pd max		375	mW
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		3.0	V
Operating supply voltage range	V _{CCop}		1.8 to 3.6	V



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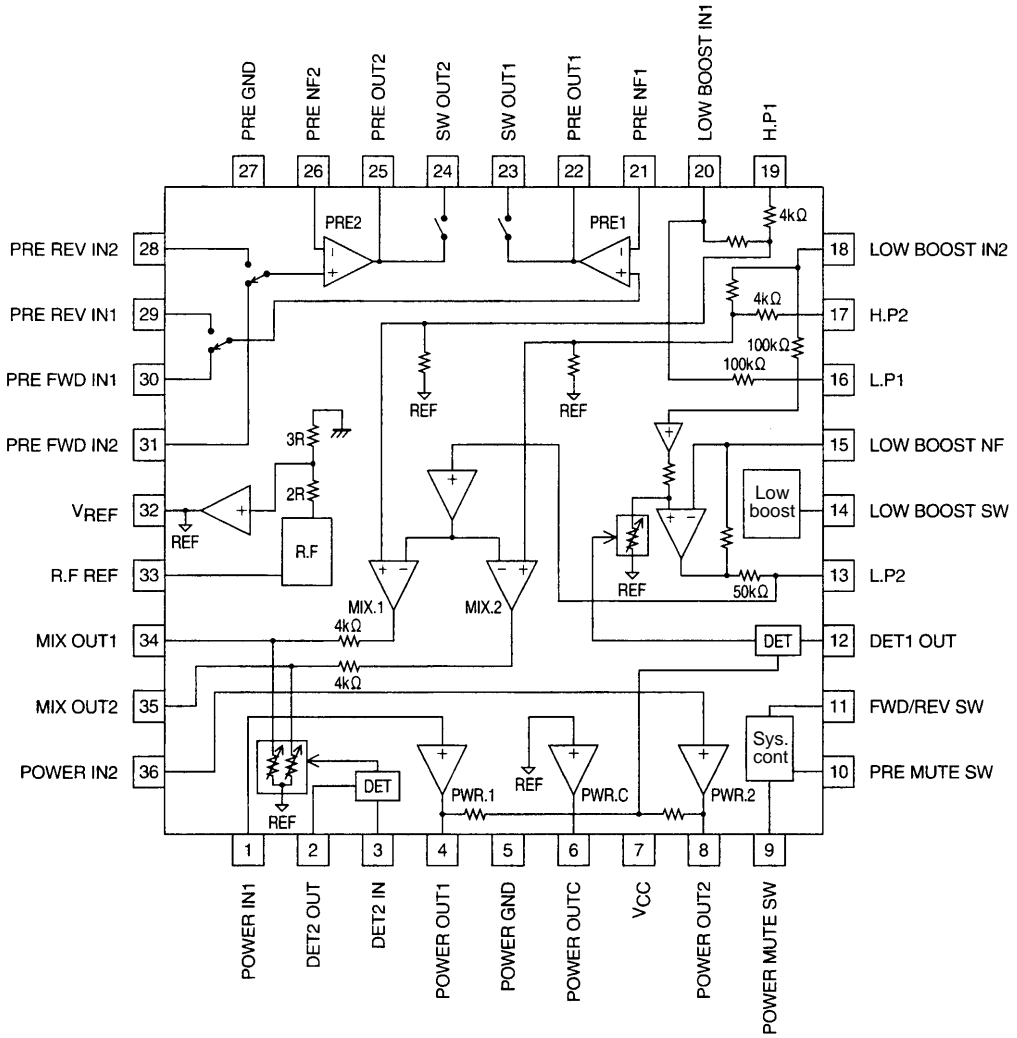
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$, $f_i = 1\text{ kHz}$, $0.775 = 0\text{ dBm}$, preamplifier $R_L = 10\text{ k}\Omega$, low boost, power amplifier $R_L = 10\ \Omega$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PRE + LOW BOOST + PVSS + PWR]						
Quiescent current	I_{CCO1}	$R_g = 2.2\text{ k}\Omega$, low boost off, PVSS off	12	15	21	mA
	I_{CCO2}	$R_g = 2.2\text{ k}\Omega$, low boost on, PVSS on	12	15	21	μA
Voltage gain (closed loop)	V_{GT}	$V_O = -5\text{ dBm}$	62	64	67	dB
[PRE AMP]						
Voltage gain (open loop)	V_{G0}	$V_O = -5\text{ dBm}$	70	83		dB
Voltage gain (closed loop)	V_{G1}	$V_O = -5\text{ dBm}$		40		dB
Maximum output voltage	$V_{O\text{ max}1}$	THD = 1%, $V_{CC} = 1.8\text{ V}$	0.1	0.2		V
Total harmonic distortion	THD1	$V_O = 0.2\text{ V}$, $V_G = 40\text{ dB/NAB}$		0.05	0.5	%
Equivalent input noise voltage	V_{NI}	$R_g = 2.2\text{ k}\Omega$, BPF = 20 Hz to 20 kHz		1.3	2.0	μV
Crosstalk	CT1	$R_g = 2.2\text{ k}\Omega$, TUNE 1 kHz	60	80		dB
Ripple rejection ratio	SVRR	$R_g = 2.2\text{ k}\Omega$, $V_{CC} = 1.8\text{ V}$, $V_r = -20\text{ dBm}$, $f_r = 100\text{ Hz}$	40	50		dB
[POWER AMP]						
Output voltage	P_O	THD = 10%	23	34		mW
Voltage gain	V_{G2}	$V_O = -5\text{ dBm}$	27	29	32	dB
Total harmonic distortion	THD2	$P_O = 1\text{ mW}$		0.4	1.0	%
Interchannel crosstalk	CT2	$V_O = -5\text{ dBm}$, $R_V = 0\ \Omega$	30	40		dB
Output noise voltage	V_{NO1}	$R_V = 0\ \Omega$, BPF = 20 Hz to 20 kHz		25	40	μV
Ripple rejection ratio	R_r2	$R_V = 0\ \Omega$, $V_r = -20\text{ dBm}$, $f_r = 100\text{ Hz}$, $V_{CC} = 1.8\text{ V}$	45	55		dB
Input resistance	R_i		22	30	38	$\text{k}\Omega$
DC offset voltage	$V_{ODC\text{ OFF}}$	Between pin 6 and pins 4 and 8	-90		+90	mV
[LOW BOOST]						
Voltage gain	V_{G3}	$V_i = -30\text{ dBm}$, boost on/off	-2.3	-3.8	-5.3	dB
Boost*	BST1	$V_{i\text{BST}} = -30\text{ dBm}$, $f = 100\text{ Hz}$, boost on	11.2	14.7	18.2	dB
	BST2	$V_{i\text{BST}} = -30\text{ dBm}$, $f = 10\text{ kHz}$, boost on	7.0	8.5	10	dB
Maximum output voltage	$V_{O\text{ max}2}$	THD = 1%, boost on	0.25	0.4		V
Total harmonic distortion	THD3	$V_O = 0.1\text{ V}$, boost on		0.1	0.5	%
Interchannel crosstalk	CT3	$V_O = -20\text{ dBm}$, $R_g = 0$, boost on	25	32		dB
Output noise voltage	V_{NO2}	$R_g = 0$, BPF = 20 Hz to 20 kHz, boost on		2.0	5.0	μV
Ripple rejection ratio	R_r3	$R_g = 0$, $f_r = 100\text{ Hz}$, $V_r = -20\text{ dBm}$, $V_{CC} = 1.8\text{ V}$, boost on	45	53		dB
[LOW BOOST + PVSS + POWER] The following items are measured at an R_V of 10 $\text{k}\Omega$ maximum.						
Voltage gain	V_{G4}	$V_i = -40\text{ dBm}$, $f = 1\text{ kHz}$, boost off/on	22	24	27	dB
LOW BOOST output voltage	V_{O1}	$V_i = -43\text{ dBm}$, $f = 100\text{ Hz}$, boost on	0.13	0.23	0.33	V
LOW BOOST output voltage	V_{O2}	$V_i = -28\text{ dBm}$, $f = 100\text{ Hz}$, boost on	0.25	0.40	0.55	V
LOW BOOST total harmonic distortion	THD4	$V_i = -40\text{ dBm}$, $f = 100\text{ Hz}$, boost on		0.5	1.2	%
Output noise voltage	V_{NO3}	$R_g = 0$, CCIR-ARM, boost off, with the power input switch K18 set to B.	-88	-85	-82	dBm
PVSS voltage	V_{O3}	$V_i = -40\text{ dBm}$, PVSS 2	-40	-37	-34	dBm
PVSS width	W_{PVSS}	The input amplitude between the start point and the point where the output is +4 dB. PVSS on	30	40		dB
PVSS harmonic distortion	THD5	$V_i = -40\text{ dBm}$, PVSS 2		0.5	1.2	%
PVSS start input level	V_{OPi}	PVSS 2	-67	-63	-59	dBm

Note: *The amount of boost for a 1-kHz input.

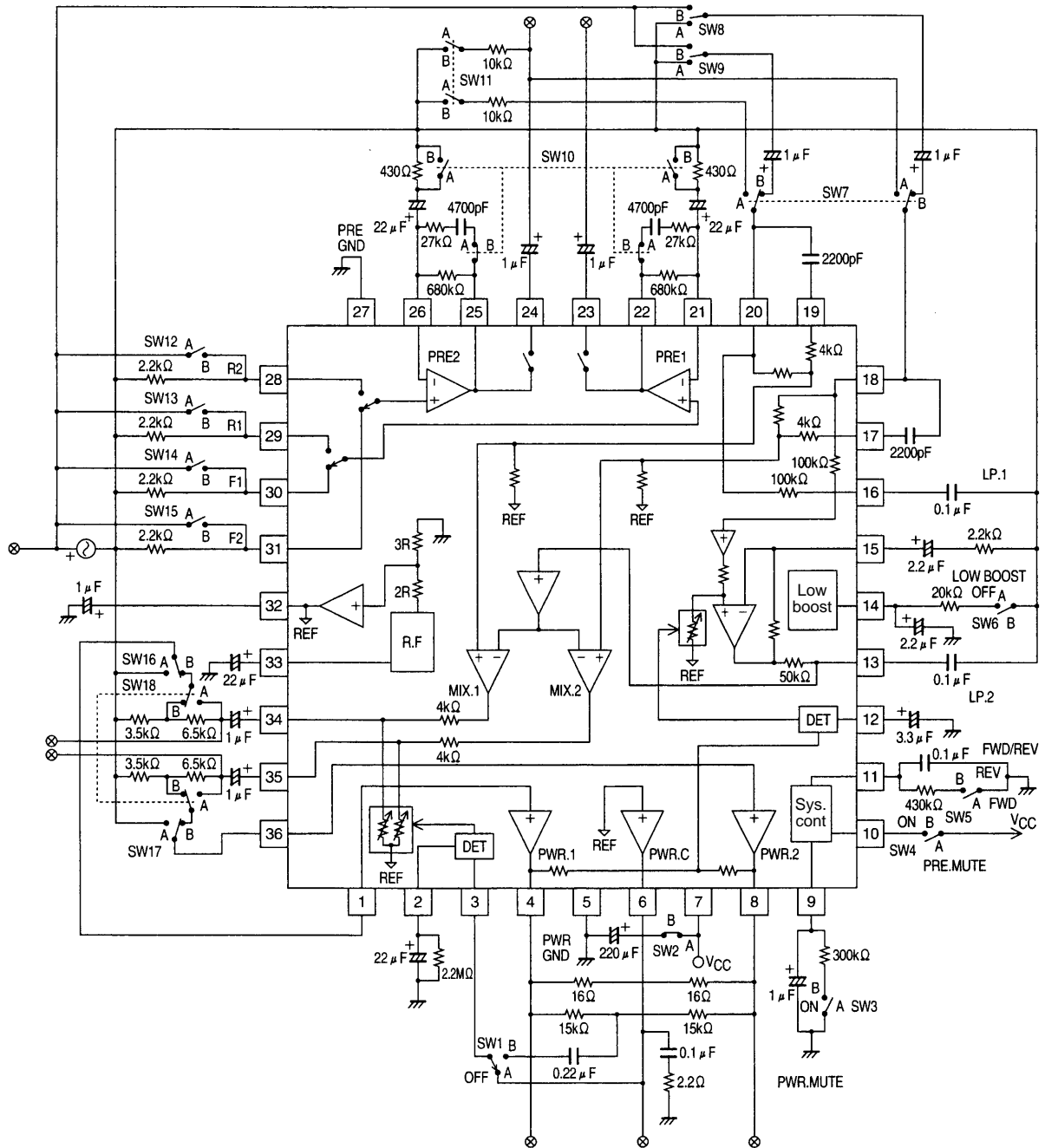
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Block Diagram



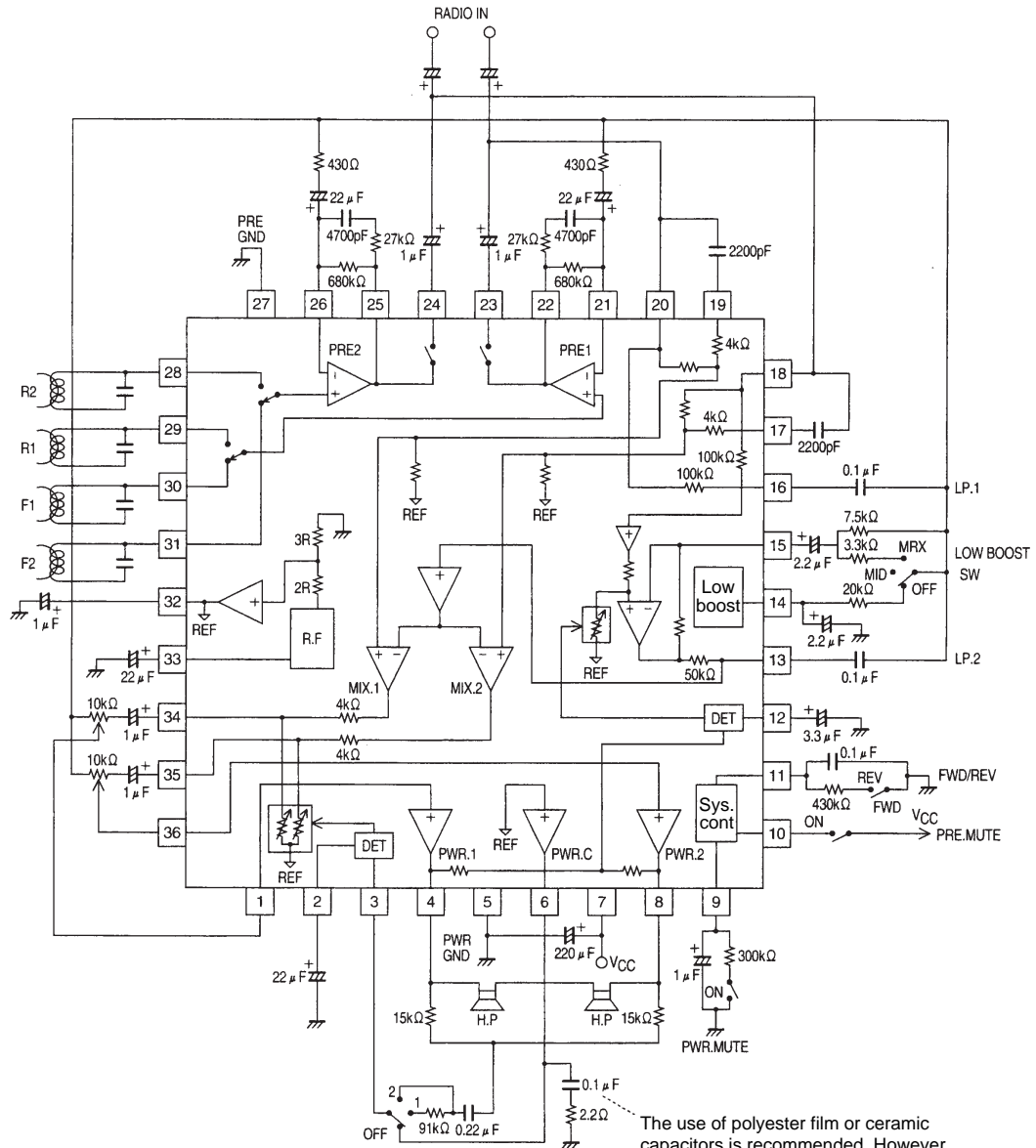
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Test Circuit Diagram



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Sample Application Circuit



The use of polyester film or ceramic capacitors is recommended. However, capacitors whose capacitances are guaranteed for the operating temperature range of the end product should be used.

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