



Monolithic Linear IC

LA5314

**Variable Divided Voltage Generator
for LCD Use**

Overview

The LA5314 is a variable divided voltage generator IC for multiple drive of LCD matrix.

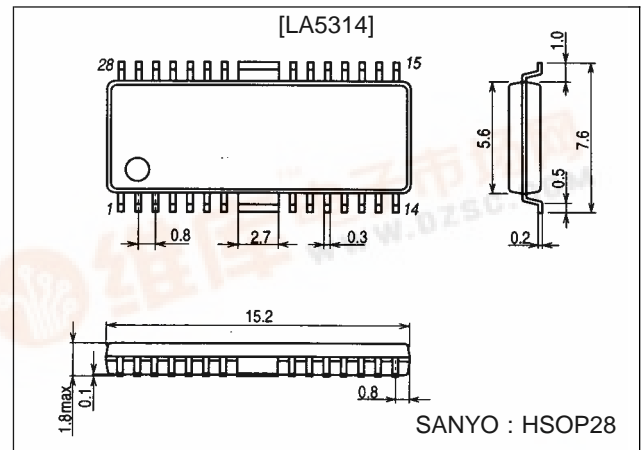
Features

- Power supply for variable bias LCD matrix. (1/5 to 1/20 bias available by built-in resistances)
- Five operational amplifiers to deliver 5 voltage outputs
- Low current drain (1.6 mA typ)
- Miniflat package for miniturization

Package Dimensions

unit : mm

3222-HSOP28



Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	V _{CC} - V _{EE}	38	V
Maximum output current	I _{OUT} max	V ₀ to V ₄	*±25	mA
Allowable power dissipation	P _d max		600	mW
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-30 to +150	°C

- Note: 1. Continuous operation (non breakdown) is guaranteed when operated at the maximum ratings shown above.
 2. *The maximum output current is a value specified under the conditions otherwise specified separately.

Operating Conditions at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}	V _{CC} - V _{EE}	10 to 35	V
Output current	I _{OUT0, 1}	V ₀ , V ₁	-0.5 to +10	mA
	I _{OUT2, 3}	V ₂ , V ₃	-10 to +10	mA
	I _{OUT4}	V ₄	-15 to +0.5	mA

Note: 3. Set V_{CC} and V_{EE} so that |V₀-V₁| and |V₄| become 1V or greater.

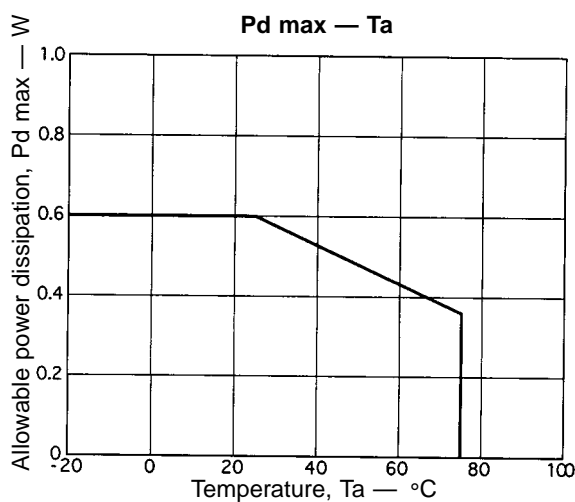


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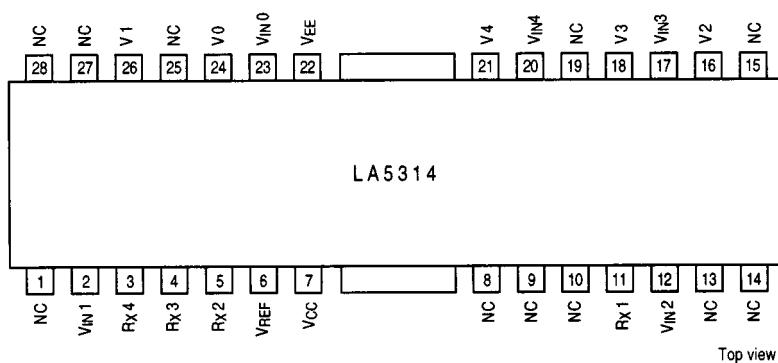
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} - V_{EE} = 20\text{ V}$, $V_{REF} = V_{CC}$, $R_X = 8R$

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{CC}, I_{EE}	$V_{CC}, V_{EE}: V_{CC} - V_{EE} = 20\text{ V}, R_X = 8R$		1.6	3	mA
Output voltage difference 1	Vd1	$(V_0 - V_1) - (V_1 - V_2)$	-30		+30	mV
Output voltage difference 2	Vd2	$(V_3 - V_4) - (V_4 - V_{EE})$	-30		+30	mV
Output voltage ratio 1	Rb1	$V_0/(V_0 - V_1)$	11.64	12.00	12.36	—
Output voltage ratio 2	Rb2	$V_0/(V_0 - V_2)$	5.82	6.00	6.18	—
Output voltage ratio 3	Rb3	V_0/V_3	5.82	6.00	6.18	—
Output voltage ratio 4	Rb4	V_0/V_4	11.64	12.00	12.36	—
Internal resistnace ratio 1	8R	$R_{X1} - R_{X2}^*$		8		—
Internal resistance ratio 2	12R	$R_{X1} - R_{X3}^*$		12		—
Internal resistance ratio 3	14R	$R_{X1} - R_{X4}^*$		14		—
Internal resistance ratio 4	15R	$R_{X1} - V_{IN3}^*$		15		—
Resistance	R	R value when 0.6 V is applied across $R_{X5} - R_{X6}$:		20		k Ω
Load regulation 1	ΔV_0	$V_0: -0.2\text{ mA} < I_{OUT0} < +10.0\text{ mA}$	-20		+20	mV
Load regulation 2	ΔV_1	$V_1: -0.2\text{ mA} < I_{OUT1} < +10.0\text{ mA}$	-20		+20	mV
Load regulation 3	ΔV_2	$V_2: -10.0\text{ mA} < I_{OUT2} < +10.0\text{ mA}$	-20		+20	mV
Load regulation 4	ΔV_3	$V_3: -10.0\text{ mA} < I_{OUT3} < +10.0\text{ mA}$	-20		+20	mV
Load regulation 5	ΔV_4	$V_4: -10.0\text{ mA} < I_{OUT4} < +0.2\text{ mA}$	-20		+20	mV

Note* : Referenced to R between R_{X4} and V_{IN3}

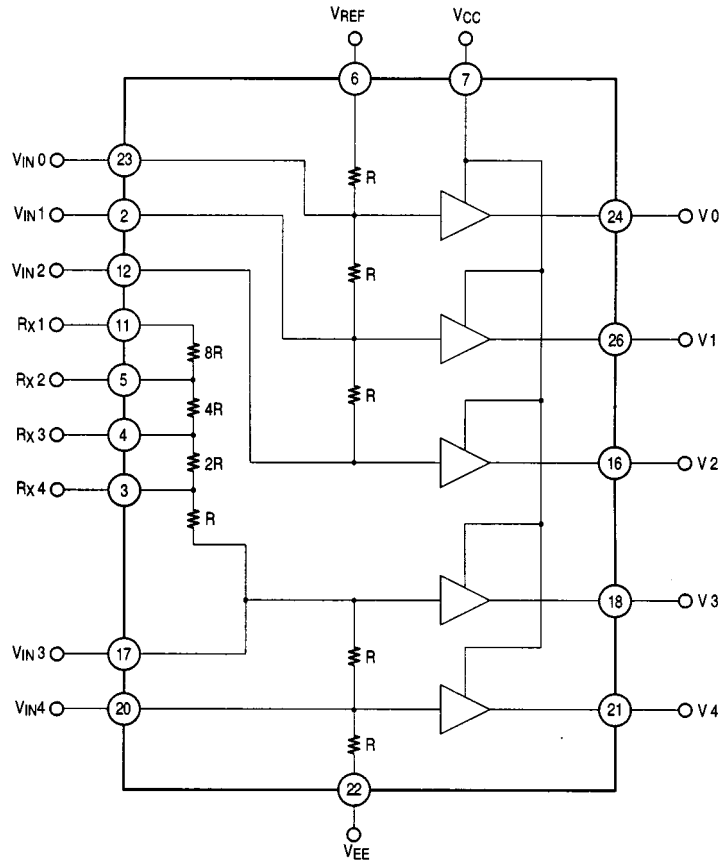


Pin Assignment



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Block Diagram

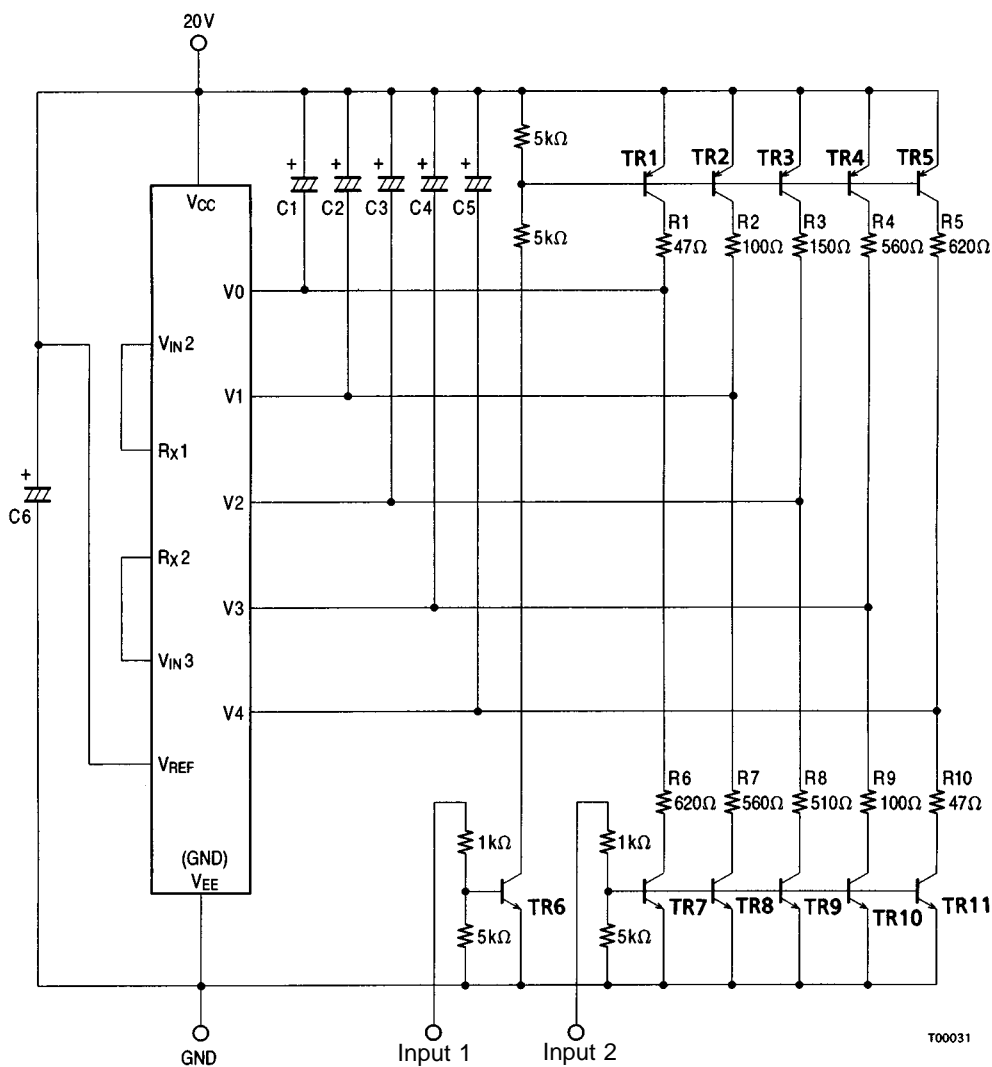


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Note: Use the IC so that $V_{RX1} \cong V_{RX2} \cong V_{RX3} \cong V_{RX4}$ is obeyed.

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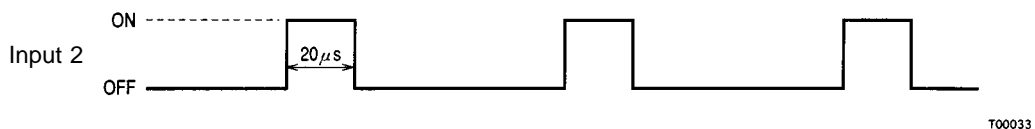
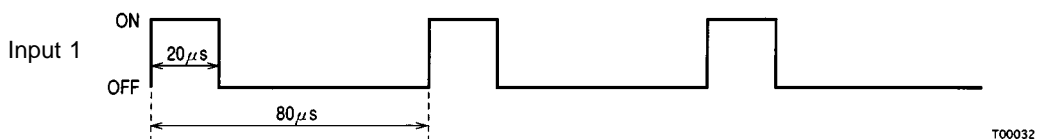
Maximum Output Current Load Test Conditions



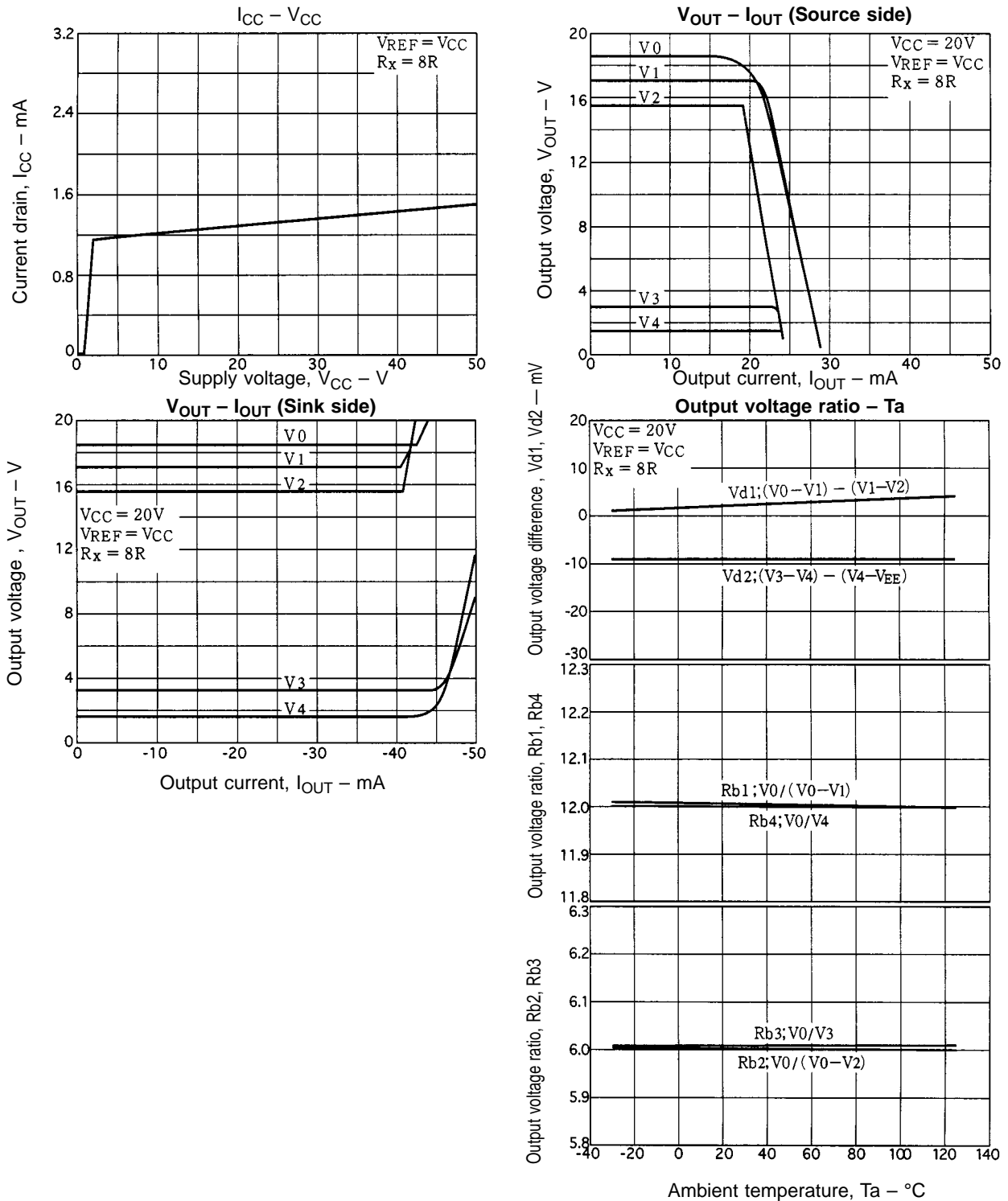
$V_{CC} - V_{EE} = 20 \text{ V}$, $R_X = 8R$
 $C1 = 5 \mu\text{F}$, $C2 = 10 \mu\text{F}$, $C3 = 10 \mu\text{F}$, $C4 = 5 \mu\text{F}$, $C5 = 10 \mu\text{F}$, $C6 = 33 \mu\text{F}$
 TR1 to TR5: 2SA984 E or F rank
 TR6 to TR11: 2SC2274 E or F rank

Unit (resistance: Ω , capacitance: F)

Output load resistances R1 to R10 are set in order that current of 30 mA max. are supplied to both source and sink sides when an on-level input is applied to the inputs 1 or 2.



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