Ordering number : EN5670

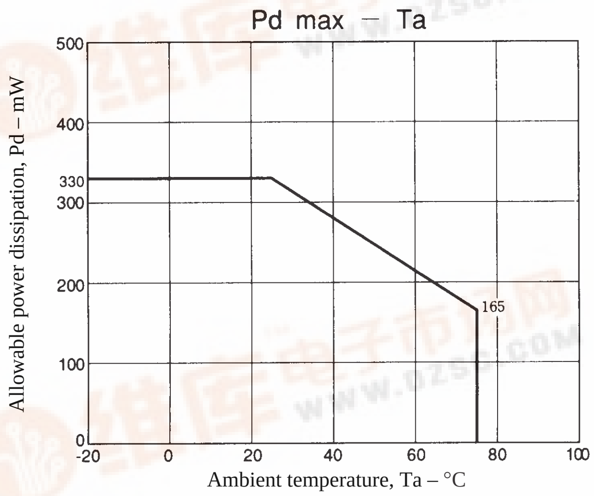
Monolithic Linear IC

LA5318V

Voltage-Dividing Voltage Generator for Multi-Voltage LCD Matrix Drive

Overview

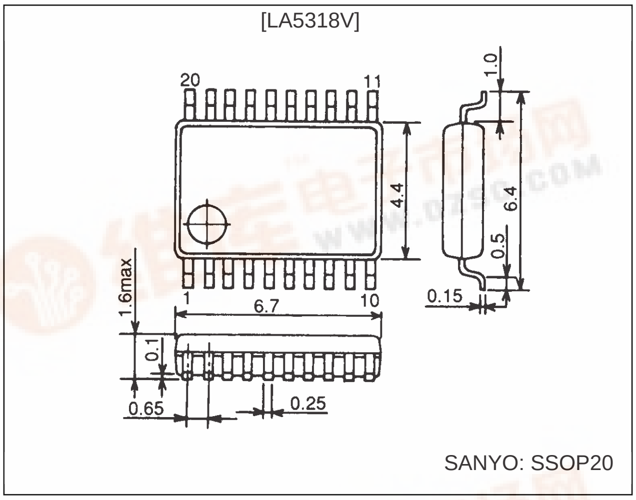
The LA5318V is a variable voltage-dividing voltage generator IC designed for driving LCD matrixes that require multiple voltages.



Package Dimensions

unit: mm

3179A-SSOP20



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{EE} max	$V_{CC} – V_{EE}$	36	V
Maximum output current	I_{OUT} max	V1 to V4	Internal*	mA
Allowable power dissipation	Pd max		330	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–30 to +125	°C

Notes: *The value stipulated in the conditions listed in the separate document shall be used as the maximum output current.
1. Continuous operation (without damage to the device) is guaranteed in the above ranges.
2. The output pins V1 to V4 may be shorted to the power supply or to ground for periods of up to 1 ms. (When $|V_{CC} – V_{EE}| < 35$ V)

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{EE}	$V_{CC} – V_{EE}$	–35.5 to –6	V
Input voltage	V_{REF}	$V_{CC} – V_{REF}$: $V_{REF} \geq V_{EE}$	–35 to –6	V
Input current	I_{INR}	INR	–0.2 to 0	mA
Output current	I_{OUTR}	OUTR	0 to 50	mA
	$I_{OUT}1, 2$	V1, V2	–5 to +5	mA
	$I_{OUT}3,4$	V3, V4	–10 to +5	mA

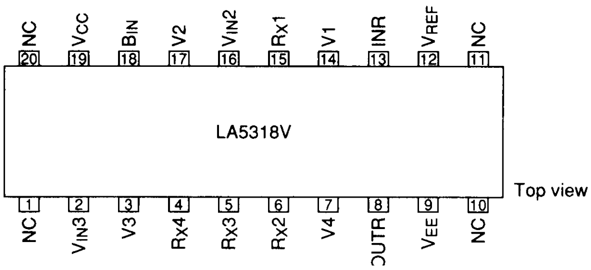
Note: V_{CC} and V_{EE} must be set up so that |V1| and $|V_{EE} – V4|$ are at least 1 V.

Operating Characteristics at Ta = 25°C, $V_{CC} - V_{EE} = -20$ V, $V_{REF} = V_{EE}$, $R_X = 8R$, B_{IN} = OPEN

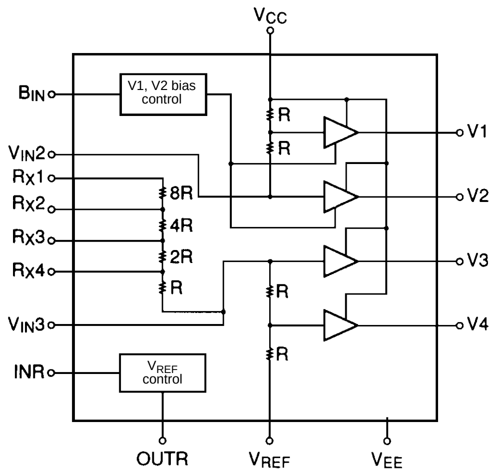
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}, I_{EE}	$V_{CC} - V_{EE} = -20$ V, $R_X = 8R$, INR = V_{CC} : V_{CC}, V_{EE}		0.35	0.5	mA
Output voltage ratio 1	Ra1	V2/V1	1.96	2.00	2.04	
Output voltage ratio 2	Ra2	$(V_{REF} - V3)/(V_{REF} - V4)$	1.96	2.00	2.04	
Output voltage ratio 3	Rb1	$V_{REF}/V1$	11.64	12.00	12.36	
Output voltage ratio 4	Rb2	$V_{REF}/V2$	5.82	6.00	6.18	
Output voltage ratio 5	Rb3	$V_{REF}/(V_{REF} - V3)$	5.82	6.00	6.18	
Output voltage ratio 3	Rb4	$V_{REF}/(V_{REF} - V4)$	11.64	12.00	12.36	
Internal resistance ratio 1	R_X1	$R_X1 - R_X2$ (Referenced to the resistance R between R_X4 and $V_{IN}3$)		8		
Internal resistance ratio 2	R_X2	$R_X1 - R_X3$ (Referenced to the resistance R between R_X4 and $V_{IN}3$)		12		
Internal resistance ratio 3	R_X3	$R_X1 - R_X4$ (Referenced to the resistance R between R_X4 and $V_{IN}3$)		14		
Internal resistance ratio 4	R_X4	$R_X1 - V_{IN}3$ (Referenced to the resistance R between R_X4 and $V_{IN}3$)		15		
Resistance	R	The value of R when the voltage across R_X4 and $V_{IN}3$ is 0.5 V.		30		kΩ
Load regulation 1	ΔV1	$+0.1$ mA < $I_{OUT}1$ < $+5$ mA : V1			±20	mV
Load regulation 2	ΔV2	$+0.1$ mA < $I_{OUT}2$ < $+5$ mA : V2			±20	mV
Load regulation 3	ΔV3	$+0.1$ mA < $I_{OUT}3$ < $+5$ mA : V3			±20	mV
Load regulation 4	ΔV4	$+0.1$ mA < $I_{OUT}4$ < $+5$ mA : V4			±20	mV
Load regulation –1A	–ΔV1A	-0.5 mA < $I_{OUT}1$ < -0.1 mA : V1			±20	mV
Load regulation –2A	–ΔV2A	-0.5 mA < $I_{OUT}2$ < -0.1 mA : V2			±20	mV
Load regulation –3	–ΔV3	-10 mA < $I_{OUT}3$ < -0.1 mA : V3			±20	mV
Load regulation –4	–ΔV4	-10 mA < $I_{OUT}4$ < -0.1 mA : V4			±20	mV
Load regulation –1B	–ΔV1B	-5 mA < $I_{OUT}1$ < -0.1 mA, B_{IN} = GND : V1			±20	mV
Load regulation –2B	–ΔV2B	-5 mA < $I_{OUT}2$ < -0.1 mA, B_{IN} = GND : V2			±20	mV
OUTR pin saturation voltage	V_{OUTR}	I_{OUT} = 20 mA, V_{CC} – INR = 2.7 : OUTR – V_{EE}			0.5	V

Note: For I_{OUT}, minus (–) indicates source current and plus (+) indicates sink current.

Pin Assignment

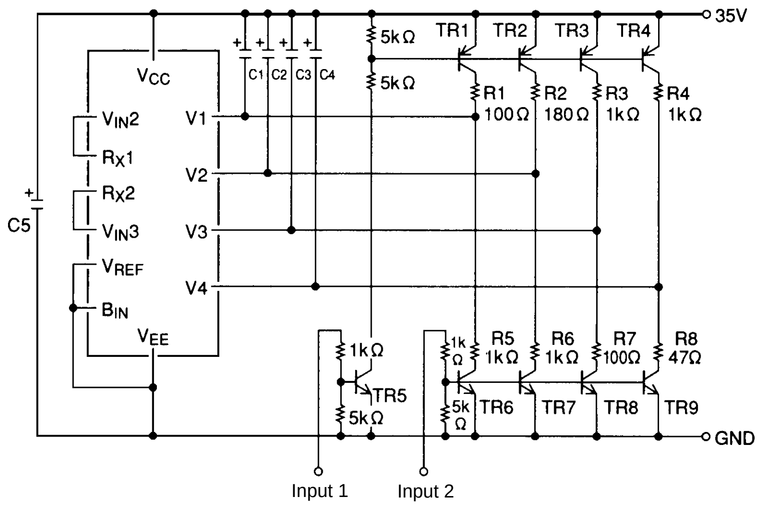


Block Diagram



(This circuit must be used with $V_{RX}1 \geq V_{RX}2 \geq V_{RX}3 \geq V_{RX}4$.)

Maximum Output Current Load Test Conditions

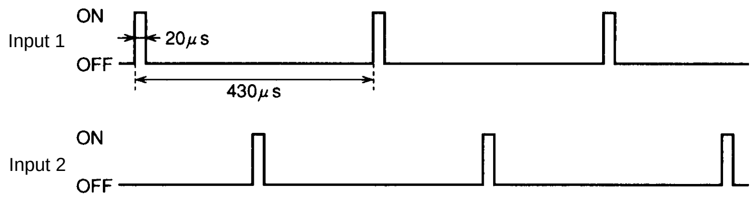


$V_{CC} - V_{EE} = 35$ V, $R_X = 8R$, C1 to C4 = 10 µF, C5 = 33 µF, All resistors must be rated 1 W or higher.

TR1 to TR4; 2SA984 Rank E or F

TR5 to TR9; 2SC2274 Rank E or F

Set the output load resistors (R1 to R8) so that currents of 25 to 30 mA maximum (except for the V3 and V4 source sides, which can handle about 60 mA) flow in the sink and source sides when high (on state) levels are input to inputs 1 and 2.



· V_{REF} control block

Determining the TR1 drive current

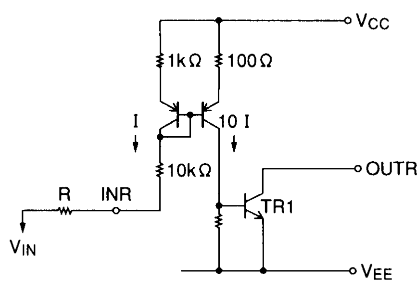
$$I = \frac{V_{CC} - V_{BE} - V_{IN}}{11\,k + R}$$

$(V_{BE} \approx 0.7\ V)$

Drive current

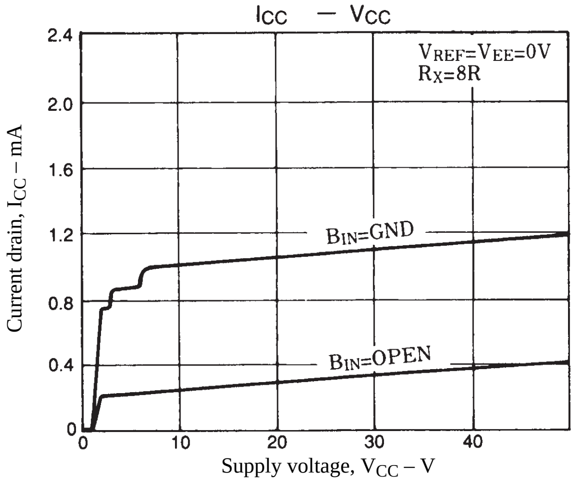
$$I_O \approx 10I = \frac{V_{CC} - 0.7 - V_{IN}}{11\,k + R} \times 10$$

Assume that the $TR1_{hFE}$ is 50 for this calculation.

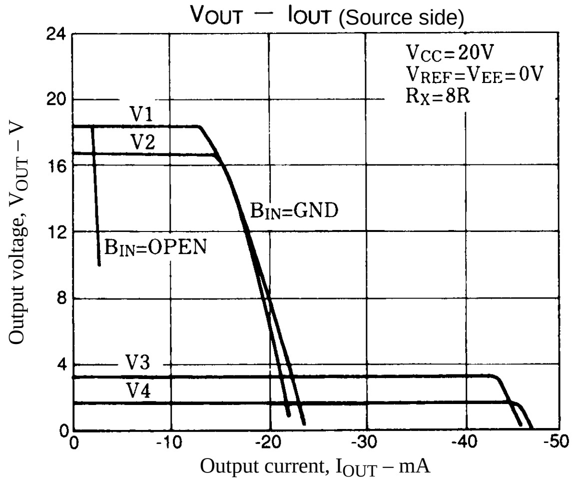


Note: Connect INR to V_{CC} when INR and OUTR are not used.

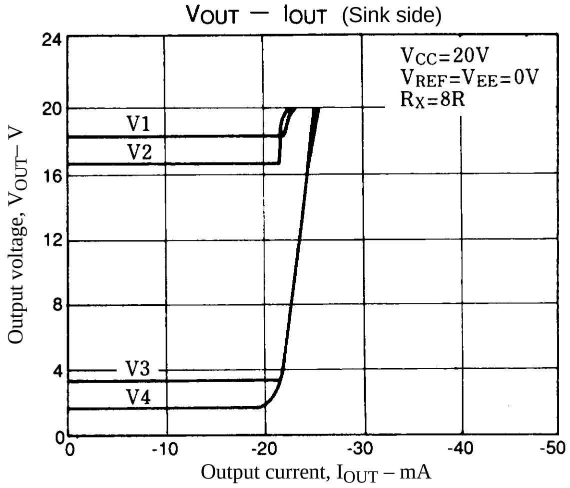
I_{CC} — V_{CC}



V_{OUT} — I_{OUT} (Source side)



V_{OUT} — I_{OUT} (Sink side)



Output Voltage Ratio – Ta