Ordering number : ENN5998

Monolithic linear IC

LA5632

Multiple Power Supply System Regulator

Overview

The LA5632 is a multiple power supply IC that provides two 3.3-V regulator circuits as well as two 5-V regulator circuits. This device is optimal for MD players and similar applications.

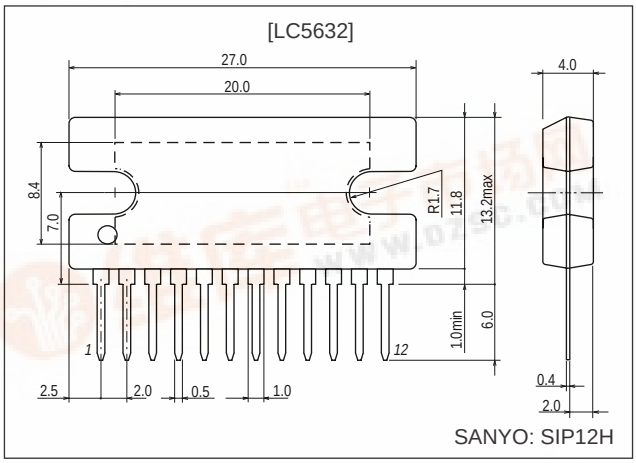
Functions and Features

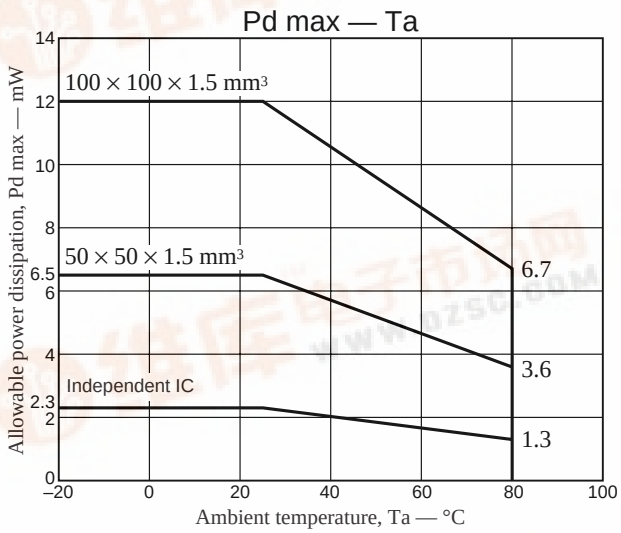
- Two built-in 3.3-V regulator circuits (I_O = 60 mA, 150 mA)
- Two built-in 5-V regulator circuits (I_O = 1000 mA, 100 mA)
- Power on/off detection circuit included
- The reset circuit operates from the B.BAK voltage.
- The reset circuit current drain is extremely low (3.5 µA (typical) in backup mode)

Package Dimensions

unit: mm

3149A-SIP12H





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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{CC} max		14	V
AC input voltage	AC max		2	V
Allowable power dissipation	Pd max	Independent IC	2.3	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{CC}		6.25 to 12	V
Reset circuit input voltage	$V_{B.BAK}$		1.4 to 3.5	V
PH5 output current	I_{PH5}		0 to 1000	mA
B.BAK output current	$I_{B.BAK}$		0 to 60	mA
ANA5 output current	I_{ANA5}		0 to 100	mA
SYS3.3 output current	$I_{SYS3.3}$		0 to 150	mA
S.RESET sink current	I_{SINKS}		0 to 0.2	mA
P.DOWN sink current	I_{SINKP}		0 to 1	mA
AC input current	I_{AC}		0 to 1	mA

Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PH5 Regulator Block] V_{CC} = 10 V, I_{PH5} = 1000 mA						
Output voltage	V_O PH5		4.75	5	5.25	V
Dropout voltage	V_{DROP} PH5			0.5	1	V
Line regulation	ΔV_{OLN} PH5	V_{CC} = 6.25 to 12 V			200	mV
Load regulation	ΔV_{OLD} PH5	I_{PH5} = 5 to 1000 mA			200	mV
Peak output current	I_{OP} PH5		1000	1400		mA
Output shorted current	I_{OSC} PH5			400	1000	mA
Current drain	I_Q PH5			70	112	mA
[SYS3.3 Regulator Block] V_{CC} = 10 V, $I_{SYS3.3}$ = 150 mA						
Output voltage	V_O SYS3.3		3.13	3.3	3.47	V
Dropout voltage	V_{DROP} SYS3.3			2	3.5	V
Line regulation	ΔV_{OLN} SYS3.3	V_{CC} = 6.25 to 12 V			200	mV
Load regulation	ΔV_{OLD} SYS3.3	$I_{SYS3.3}$ = 5 to 150 mA			200	mV
Peak output current	I_{OP} SYS3.3		150	210		mA
Output shorted current	I_{OSC} SYS3.3			200	450	mA
Current drain	I_Q SYS3.3			17.5	28	mA
[ANA5 Regulator Block] V_{CC} = 10 V, I_{ANA5} = 1000 mA						
Output voltage	V_O ANA5		4.75	5	5.25	V
Dropout voltage	V_{DROP} ANA5			0.5	1	V
Line regulation	ΔV_{OLN} ANA5	V_{CC} = 6.25 to 12 V			200	mV
Load regulation	ΔV_{OLD} ANA5	I_{ANA5} = 5 to 100 mA			200	mV
Peak output current	I_{OP} ANA5		100	140		mA
Output shorted current	I_{OSC} ANA5			40	100	mA
Current drain	I_Q ANA5			17.5	28	mA
Output noise voltage	V_{NO} ANA	10 Hz ≤ f ≤ 100 kHz		120		μV

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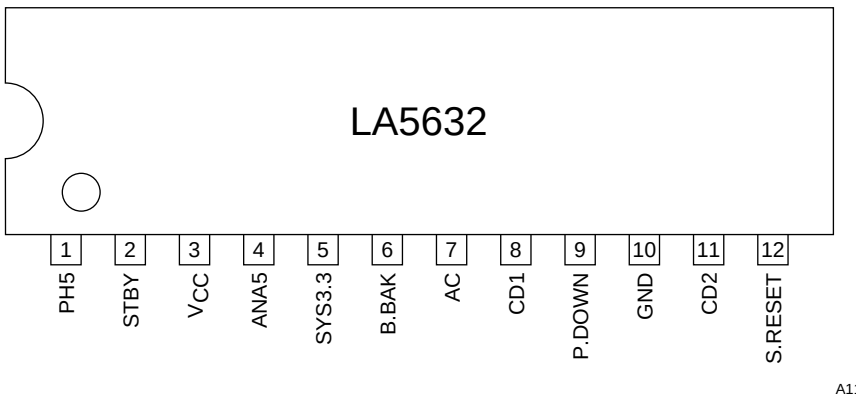
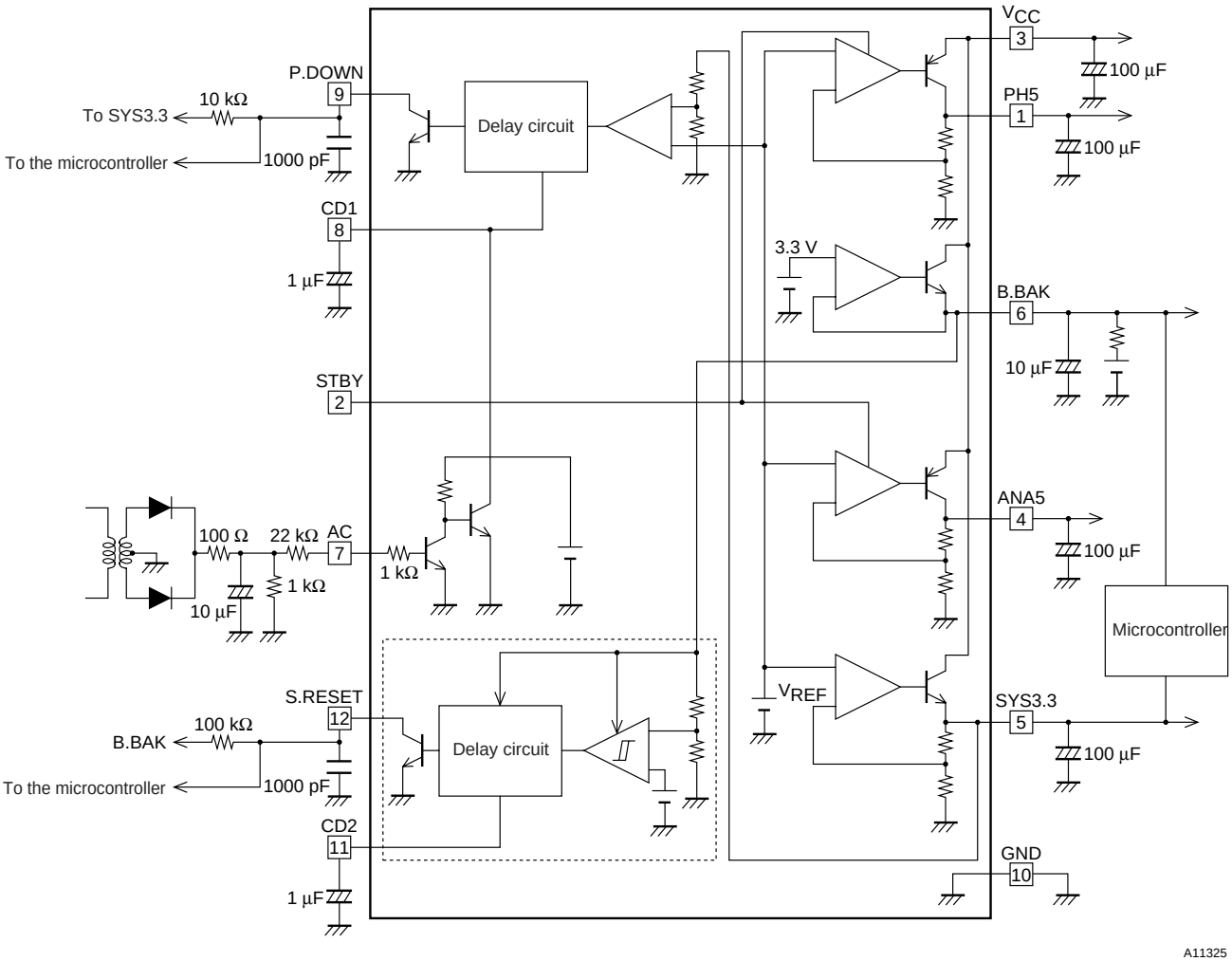
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[B.BAK Regulator Block] V_{CC} = 10 V, I_{BAK} = 60 mA						
Output voltage	V_O BAK		3.13	3.3	3.47	V
Dropout voltage	V_{DROP} BAK			2	2.5	V
Line regulation	ΔV_{OLN} BAK	V_{CC} = 6.25 to 12 V			200	mV
Load regulation	ΔV_{OLD} BAK	I_{BAK} = 5 to 60 mA			200	mV
Peak output current	I_{OP} BAK		60	84		mA
Output shorted current	I_{OSC} BAK			60	180	mA
Current drain	I_Q BAK			15	24	mA
[P.DOWN Detection Circuit] V_{CC} = 10 V						
Threshold voltage	V_{TH} P.DOWN		3.0	3.16	3.32	V
Residual voltage	Vsat P.DOWN	With the cd1 pin shorted P.DOWN pin current = 1 mA			200	mV
Delay time	td1	cd1 = 1 µF	75	100	125	ms
[S.RESET Block] V_{CC} = 0 V, B.BAK = 3.3 V						
Threshold voltage1	V_{TH}1 S.RESET		2.56	2.7	2.84	V
Threshold voltage2	V_{TH}2 S.RESET		1.9	2.0	2.1	V
Reset output undefined voltage	V_{UNS} S.RESET				1.4	
Backup mode current drain	I_{IN}1 BAK	B.BAK = 3.1 V		3.5	5	µA
Low-level output current drain	I_{IN}2 BAK	B.BAK = 1.8 V		0.36		mA
Residual voltage	Vsat S.RESET	With the cd2 pin shorted S.RESET pin current = 0.2 mA			200	mV
Delay time	td2	cd2 = 1 µF	75	100	125	ms
[AC Detection Circuit] V_{CC} = 10 V						
Threshold voltage	V_{TH} AC		0.5	0.7	0.9	V
[STBY Detection Circuit] V_{CC} = 10 V						
Threshold voltage	V_{TH} STBY		1.3	1.8	2.3	V

Pin Assignment

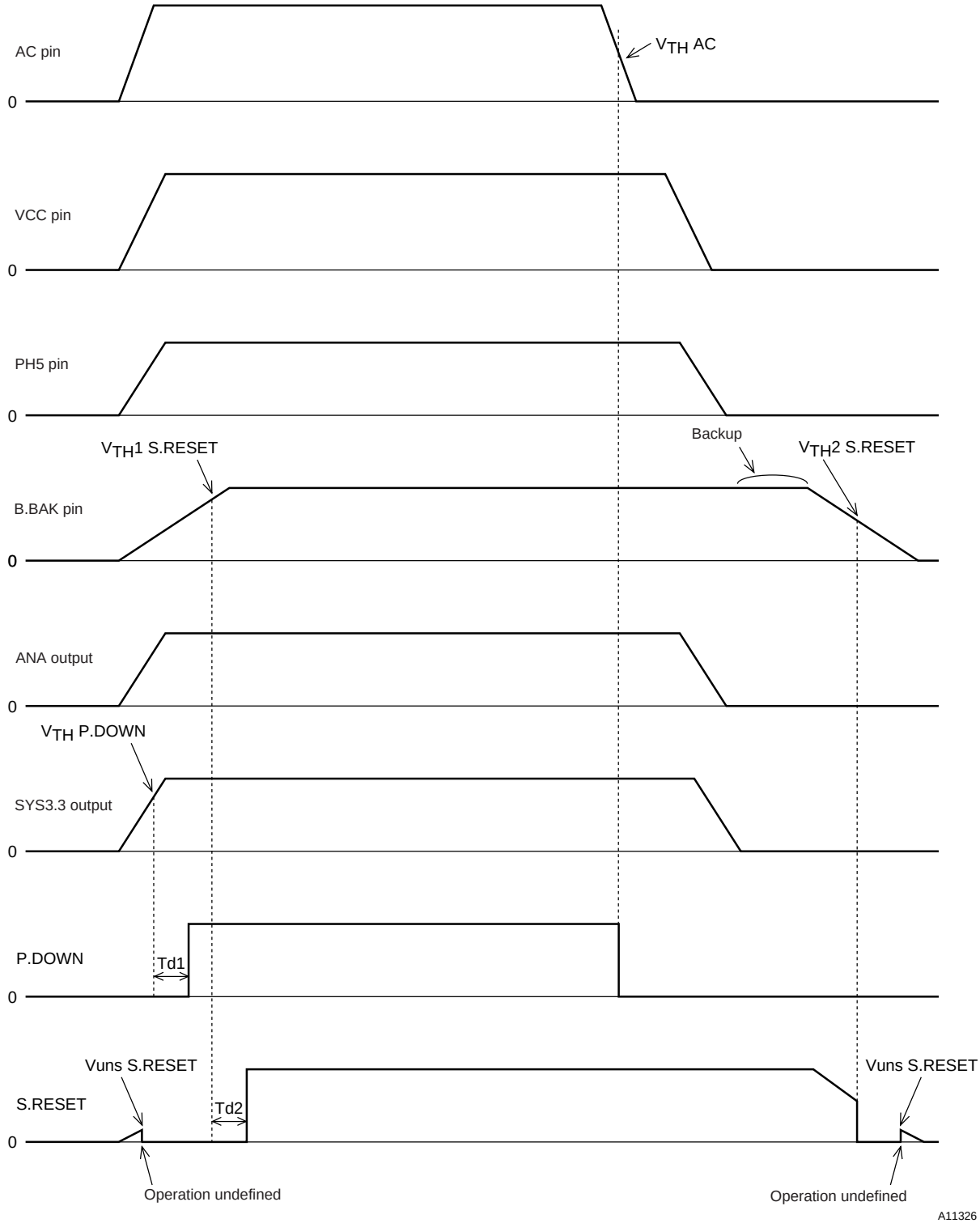


Block Diagram



Note: Use capacitors with low capacitance temperature coefficients for all capacitors.

Timing Chart



Note: The S.RESET output has an undefined operating state, so care is required in application design.