Monolithic Linear IC

SANYO

No.1774E

**LA7530N** 

# IF Signal Processing (VIF+SIF) Circuit for TV / VCR Use

The LA7530N is an IC containing the VIF section and SIF section on a single chip in the DIP20S package. The use of the small-sized package serves to make VTR tuner units smaller.

As compared with the LA7530, the LA7530N is provided with 2 pins for IF AGC, permitting higher AGC speed. The LA7530N can substitute for the LA7530, but the LA7530 cannot substitute for the LA7530N. For 9V supply, use the LA7533.

# Functions

- · VIF section: VIF AMP, VIDEO DET, PEAK IF AGC, B/W NOISE CANCELLER, RF AGC, AFT, VIDEO MUTE.
- · SIF section: SIF LIMITER AMP, FM DET, SND MUTE.

## **Features**

- · High-gain VIF amp requiring no preamp.
- · Higher AGC speed.
- · Adjustment-free FM detector because of ceramic discriminator-used quadrature detection.
- · Possible to mute video, sound for VTR.
- · Small-sized package.
- · Minimum number of external parts required.

Maximum	Ratings	at Ta =	25°C
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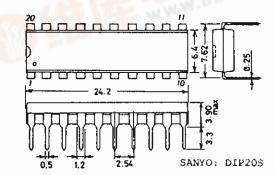
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Maximum Supply Voltage	$ m V_{CC}$ max		14	V
Flow-out Current	I <sub>16</sub> max		5	mA
Maximum Applied Voltage	$V_{20}$ max		$V_{CC}$	V
Allowable Power Dissipation	Pd max	Ta≦40°C	1.1	W
Operating Temperature	Topr		-20  to  + 70	°C
Storage Temperature	Tstg		-55  to  + 125	°C

#### Operating Conditions at Ta = 25°C

perating Conditions at Ta = 25	C	
Recommended Supply Voltage	V <sub>CC</sub>	12
Operating Voltage Range	V <sub>CC</sub> op	9 to 13.2

### **Package Dimensions**

(unit:mm) 3021B



unit

unit

V



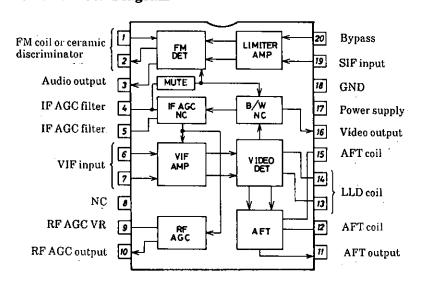
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Operating Characteristics at $Ta = 25$ °C, $V_{CC} = 12V$ , $fp = 58.75$ MHz, $fs = 54.25$ MHz(VIF),						
	0 = 4.5 MHz(SI)	<b>F</b> )	$\mathbf{min}$	typ	max	unit
Total Circuit Current	$I_{17}$	DC	47	58	74	mA
Maximum RF AGC Voltage	$V_{10H}$	DC	8.5	8.9	9.2	V
Minimum RF AGC Voltage	$V_{10L}$	DC			0.5	V
Quiescent Video Output Voltage	9 V 16	DC	5.7	6.1	6.5	v
Quiescent AFT Ouptut Voltage	$V_{11}$	DC	4.5	6.5	7.5	V
Input Sensitivity	Vi	fm = 400Hz, 40%AM,	30	36	42	dΒμ
		$V_0 = 0.8V_{p-p}$				•
AGC Range	GR	fm = 400Hz, 40%AM,	57	65		$d\mathbf{B}$
		Vo = 0.8Vp-p				
Maximum Allowable Input	Vi max	fm = 15kHz, $78%AM$ ,	100	200		mVrms
7711		$V_0 = \pm 1 dB$				
Video Output Amplitude	Vo(VIDEO)	Vi = 10 mVrms,	1.9	2.2	2.5	Vp-p
0		fm = 15kHz, $78%AM$				
Output S/N	S/N	Vi=10mVrms CW	<b>4</b> 8	54		dB
Carrier Leak	$\mathbf{CL}$	Vi = 100 mVrms,	50	55		$d\mathbf{B}$
B.F. A ATSMITT I.	**	fm = 15kHz, $78%AM$				
Maximum AFT Voltage	$\mathbf{v}_{\scriptscriptstyle 11H}$	Vi=10mVrms CW SWEEP	11	11.4		$\mathbf{v}$
Minimum AFT Voltage	$V_{11L}$ Sf	Vi=10mVrms CW SWEEP		0.5	1.0	V
AFT Detection Sensitivity	Sf	Vi=10mVrms CW SWEEP	80	110		mV/kHz
White Noise Threshold Level	$\mathbf{v}_{\mathbf{wrh}}$	Vi=10mVrms SWEEP	6.4	6.8	7.2	V
White Noise Clamp Level	Vwci.	Vi=10mVrms SWEEP	4.2	4.6	5.0	V
Black Noise Threshold Level	VBTH	Vi=10mVrms SWEEP	2.1	2.4	2.7	V
Black Noise Clamp Level	V <sub>BCL</sub> Vo (SIF)	Vi=10mVrms SWEEP	3.8	4.2	4.6	V
SIF Output Signal Voltage	Vo (SIF)	P/S = 20dB	80	1 <b>4</b> 0	210	mVrms
Frequency Characteristic	$_{ m DG}^{ m f_{ m C}}$	-3dB	5	7		$\mathbf{MHz}$
Differential Gain	DG	Vi = -27dBm (peak) 87.5%		3		%
D:00	D.D.	VIDEOMOD				
Differential Phase	DP	$V_i = -27 dBm \text{ (peak) } 87.5\%$		3		deg
Inner Designation	т.	VIDEOMOD			_	
Input Resistance	Ri		1.0	1.5	2.0	kΩ
Input Capacitance	Ci	0.170		3.0	6.0	$\mathbf{pF}$
SIF Limiting Voltage	Vi (lim)	-3dB		200	500	$\mu Vrms$
Detection Output Voltage	Vo (DET)	Vi = 100 mVrms,fm = 400 Hz,	450	680	850	mVrms
Watal Hammania Distantia	mith (Dem)	$\Delta f = \pm 25 \text{kHz}$				
Total Harmonic Distortion	THD (DET)	$V_i = 100 \text{mVrms, fm} = 400 \text{Hz},$		0.5	1.3	%
AM Dejection	AMD	$\Delta f = \pm 25 \text{kHz}$	~ .			
AM Rejection	AMR	Vi = 100 mVrms, fm = 400 Hz,	50	60		dB
		$\Delta f = \pm 25 \text{kHz}, 30\% \text{AM}$				

- Usage Note: 1. Protective circuits must be inserted when using this IC with lines directly connecting the IC pins to external circuits.

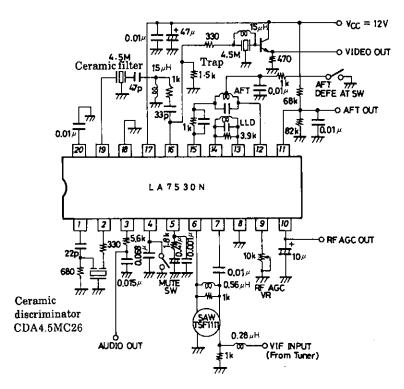
  (For example, this applies to pins 12 and 15.)
  - 2. A 1000pF capacitor must be connected between either pin 5 and ground or between pin 5 and pin 8 to prevent VIF amplifier oscillation.

## **Equivalent Circuit Block Diagram**



## Sample Application Circuit (Japan)

 The LA7530N differs from the LA7530 in the circuit externaly connected to pins 5, 8



Unit (resistance:  $\Omega$ , capacitance: F)

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