

| | | |
|--|----------|----------------------|
| SANYO | No. 5188 | Monolithic Linear IC |
| | | LA9220M |
| Analog Signal Processing Circuit (ASP) for CD players | | |

Overview

The LA9220M is an analog signal processing and servo control bipolar IC designed for use in compact disc players; a compact disc player can be configured by combining this IC, a CD-DSP such as the LC78681KE, and a small number of additional components.

Functions

I/V amplifier, RF amplifier (with AGC), SLC, APC, VCOC amplifier, VCO (supports double-speed playback), FE, TE (with VCA and auto-balance function), tracking servo amplifier (with offset cancellation function), spindle servo amplifier (with gain switching function), sled servo amplifier (with off function), focus detection (DRF, FZD), track detection (HFL, TES), defect detection, and shock detection.

Features

The following automatic adjustment functions are built in.

- Focus offset auto cancel
- Tracking offset auto cancel
- EF balance auto adjustment
- RF level AGC function
- Tracking servo gain RF level following function

Specifications

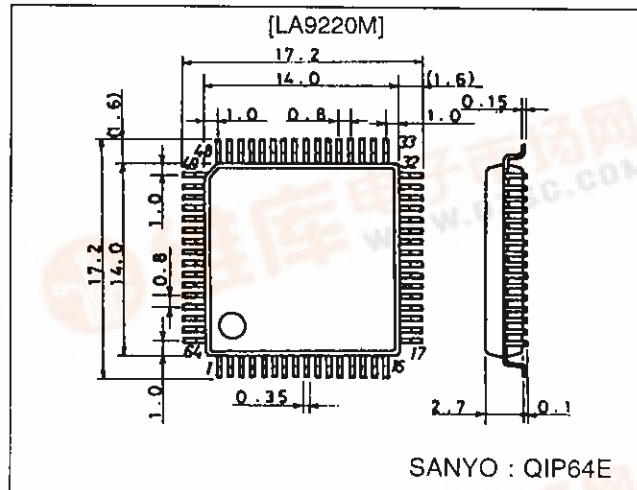
Absolute Maximum Ratings at Ta = 25 °C, Pins 22, 45 = GND

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|----------|------------|-------------|------|
| Maximum supply voltage | Vsup max | Pin 56, 64 | 7 | V |
| Allowable power dissipation | Pd max | | 350 | mW |
| Operating temperature | Topr | | -25 to +75 | °C |
| Storage temperature | Tstg | | -40 to +150 | °C |

Package Dimensions

unit : mm

3159-QFP64E



LA9220M

Operating Conditions at Pins 22, 45 = GND

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------------|--------------|------------|------------|------|
| Recommended supply voltage | V_{CC} | | +5 | V |
| Operating supply voltage | $V_{CC\ op}$ | | 3.6 to 5.5 | V |

Operating Characteristics at $T_a = 25\ ^\circ\text{C}$, Pins 22, 45 = GND, V_{CC} (pins 56, 64) = 5 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|------------------------|---------------|---|-------|-------|-------|------|
| Current drain | I_{CCO} | V_{CC1} (pin 64) + V_{CC2} (pin 56) | 25 | 40 | 55 | mA |
| Reference voltage | V_{ref} | VR | 2.3 | 2.5 | 2.7 | V |
| [Interface] | | | | | | |
| CE-Vth | CE_{vth} | CE | | 0.8 | | V |
| CL-Vth | CL_{vth} | CL | | 0.8 | | V |
| DAT-Vth | DAT_{vth} | DAT | | 0.8 | | V |
| Maximum CL frequency | CL_{max} | | 500 | | | kHz |
| [RF amplifier] | | | | | | |
| RFSM no signal voltage | $RFSM_o$ | | 1.35 | 1.60 | 1.85 | V |
| Minimum gain | $RFSM_{Gmin}$ | FIN1, FIN2 : 1 M Ω -input, PH1 = 4 V freq = 200 kHz, RFSM | -14.0 | -12.5 | -11.0 | dB |
| [Focus amplifier] | | | | | | |
| FDO gain | FD_G | FIN2 : 1 M Ω -input, FDO | 3.5 | 5.0 | 6.5 | dB |
| FDO offset | FD_{ost} | Difference from reference voltage, servo on | -170 | 0 | +170 | mV |
| Off time offset | FD_{ofost} | Difference from reference voltage, servo off | -40 | 0 | +40 | mV |
| Offset adjustment step | FD_{step} | FDO | | 50 | | V |
| F search voltage H | FS_{max} | FDO | | 0.8 | | V |
| F search voltage L | FS_{min} | FDO | | -0.8 | | V |
| [Tracking amplifier] | | | | | | |
| TE gain MAX | TE_{Gmax} | f = 10 kHz, E: 1 M Ω -input, PH1 = 4 V | 5.0 | 6.5 | 8.0 | dB |
| TE gain MIN | TE_{Gmin} | f = 10 kHz, E: 1 M Ω -input, PH1 = 1 V | -0.5 | +1.8 | +4.0 | dB |
| TE-3 dB | TE_{fc} | E: 1 M Ω -input | | 60 | | kHz |
| TO gain | TO_G | TH \rightarrow TO gain, THLD mode | 4.0 | 6.0 | 8.0 | dB |
| TGL offset | TGL_{ost} | Servo on, TGL = H, TO | -250 | 0 | +250 | mV |
| TGH offset | TGH_{ost} | TGL = L, difference from TGL offset, TO | -50 | 0 | +50 | mV |
| THLD offset | $THLD_{ost}$ | THLD mode, difference from TGL offset, TO | -50 | 0 | +50 | mV |
| Off 1 offset | $OFF1_{ost}$ | TOFF = H | -50 | 0 | +50 | mV |
| Off 2 offset | $OFF2_{ost}$ | TOFF2 off (IF) | -50 | 0 | +50 | mV |
| Offset adjustment step | TO_{step} | TO | | 60 | | mV |
| Balance range H | BAL-H | Δ gain E/F input, TB = 5 V | | +3.5 | | dB |
| Balance range L | BAL-L | Δ gain E/F input, TB = 0 V | | -3.5 | | dB |
| TOFF-VTH | $TOFF_{vth}$ | | 1.0 | 2.5 | 3.0 | V |
| TGL-VTH | TGL_{vth} | | 1.0 | 2.5 | 3.0 | V |
| [PH] | | | | | | |
| No signal voltage | PH_o | Difference from RFSM | -0.85 | -0.65 | -0.45 | V |
| [BH] | | | | | | |
| No signal voltage | BH_o | Difference from RFSM | 0.45 | 0.65 | 0.85 | V |
| [DRF] | | | | | | |
| Detection voltage | DRF_{vth} | Difference from VR at RFSM | -0.60 | -0.35 | -0.20 | V |
| Output voltage H | DRF-H | | 4.5 | 4.9 | | V |
| Output voltage L | DRF-L | | | 0 | +0.5 | V |
| [FZD] | | | | | | |
| Detection voltage 1 | FZD1 | FE, difference from VR | 0 | +0.2 | | V |
| Detection voltage 2 | FZD2 | FE, difference from VR | | 0 | | V |

Continued on next page.

LA9220M

Continued from preceding page.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--------------------------------|----------|--|-------|-------|-------|------|
| [HFL] | | | | | | |
| Detection voltage | HFLvth | Difference from VR at RFSM | -0.35 | -0.2 | -0.05 | V |
| Output voltage H | HFL-H | | 4.5 | 4.9 | | V |
| Output voltage L | HFL-L | | | 0 | +0.5 | V |
| [TES] | | | | | | |
| Detection voltage LH | TES-LH | TESI, difference from VR | -0.15 | -0.10 | -0.05 | V |
| Detection voltage HL | TES-HL | TESI, difference from VR | 0.05 | 0.10 | 0.15 | V |
| Output voltage H | TES-H | | 4.5 | 4.9 | | V |
| Output voltage L | TES-L | | | 0 | +0.5 | V |
| [JP] | | | | | | |
| Output voltage H | JP-H | Difference from JP ⁺ = 0 V, JP ⁻ = 0 V at JP ⁺ = 0 V, JP ⁻ = 5 V, TO | 0.35 | 0.5 | 0.65 | V |
| Output voltage L | JP-L | Difference from JP ⁺ = 0 V, JP ⁻ = 0 V at JP ⁺ = 5 V, JP ⁻ = 0 V, TO | -0.65 | -0.5 | -0.35 | V |
| [Spindle amplifier] | | | | | | |
| Offset 12 | SPD12ost | Difference from VR at SPD, 12 cm mode | -40 | 0 | +40 | mV |
| Offset 8 | SPD8ost | Difference from VR at SPD, 8 cm mode | -40 | 0 | +40 | mV |
| Offset off | SPDof | Difference from VR at SPD, OFF mode | -30 | 0 | +30 | mV |
| Output voltage H12 | SPD-H12 | Difference from offset-12, 12 cm mode CV ⁺ = 5 V, CV ⁻ = 0 V | 0.75 | 1.0 | 1.25 | V |
| Output voltage L12 | SPD-L12 | Difference from offset-12, 12 cm mode CV ⁺ = 0 V, CV ⁻ = 5 V | -1.25 | -1.0 | -0.75 | V |
| Output voltage H8 | SPD-H 8 | Difference from offset-8, 8 cm mode CV ⁺ = 5 V, CV ⁻ = 0 V | 0.35 | 0.5 | 0.65 | V |
| [Sled amplifier] | | | | | | |
| SLEQ offset | SLEQost | Difference from TO at SLEQ | -30 | 0 | +30 | mV |
| Offset SLD | SLDost | SLEQ = VR, difference from VR | -100 | 0 | +100 | mV |
| Offset off | SLDof | Off mode | -40 | 0 | +40 | mV |
| Off VTH | SLOFvth | SLOF | 1.0 | 1.4 | 2.0 | V |
| [SLC] | | | | | | |
| No signal voltage | SLCo | SLC | 2.25 | 2.5 | 2.75 | V |
| [Shock] | | | | | | |
| No signal voltage | SCIo | SCI, difference from VR | -40 | 0 | +40 | mV |
| Detection voltage H | SClvthH | SCI, difference from VR | 60 | 100 | 140 | mV |
| Detection voltage L | SClvthL | SCI, difference from VR | -140 | -100 | -60 | mV |
| [DEF] | | | | | | |
| Detection voltage | DEFvth | Difference between LF2 voltage when RFSM = 3.5 V and DEF is detected, and LF2 voltage when RFSM = 3.5 V | 0.20 | 0.35 | 0.50 | V |
| Output voltage H | DEF-H | | 4.5 | 4.9 | | V |
| Output voltage L | DEF-L | | | 0 | +0.5 | V |
| [APC] | | | | | | |
| Reference voltage | LDS | LDS voltage at which LDD = 3 V | 150 | 180 | 210 | mV |
| Off voltage | LDDof | LDD | 3.9 | 4.3 | 4.6 | V |
| [VCO] | | | | | | |
| Free-running frequency fo | VCOfo | CLK = 4.23 MHz | 8.14 | 8.64 | 9.14 | MHz |
| Upper limit variable width ΔfH | VCOΔfH | Difference from fo | 1.4 | 2.1 | 2.8 | MHz |
| Lower limit variable width ΔfL | VCOΔfL | Difference from fo | -2.5 | -1.9 | -1.3 | MHz |
| Output level 1 | VCOv1 | Normal mode | 0.5 | 1.0 | | Vp-p |
| Output level 2 | VCOv2 | 2FREQ mode | 0.5 | 1.0 | | Vp-p |

LA9220M

Pin Functions

| Pin No. | Symbol | Contents |
|---------|------------------|--|
| 1 | FIN2 | Pickup photodiode connection pin. Added to pin FIN1 to generate the RF signal, subtracted from pin FIN1 to generate the FE signal. |
| 2 | FIN1 | Pickup photodiode connection pin. |
| 3 | E | Pickup photodiode connection pin. Subtracted from pin F to generate the TE signal. |
| 4 | F | Pickup photodiode connection pin. |
| 5 | TB | TE signal DC component input pin. |
| 6 | TE ⁻ | Pin to which the TE signal gain setting resistor is connected between this pin and TE pin. |
| 7 | TE | TE signal output pin. |
| 8 | TESI | TES (Track Error Sense) comparator input pin. The TE signal is input through a bandpass filter. |
| 9 | SCI | Shock detection input pin. |
| 10 | TH | Tracking gain time constant setting pin. |
| 11 | TA | Pin to connect to the servo high-pass elimination capacitor. |
| 12 | TD ⁻ | Pin for configuring the tracking phase compensation constant between the TD and VR pins. |
| 13 | TD | Tracking phase compensation setting pin. |
| 14 | JP | Tracking jump signal (kick pulse) amplitude setting pin. |
| 15 | TO | Tracking control signal output pin. |
| 16 | FD | Focusing control signal output pin. |
| 17 | FD ⁻ | Pin for configuring the focusing phase compensation constant between the FD and FA pins. |
| 18 | FA | Pin for configuring the focusing phase compensation constant between the FD ⁻ and FA ⁻ pins. |
| 19 | FA ⁻ | Pin for configuring the focusing phase compensation constant between the FA and FE pins. |
| 20 | FE | FE signal output pin. |
| 21 | FE ⁻ | Pin to which the FE signal gain setting resistor is connected between this pin and FE pin. |
| 22 | AGND | Analog signal GND. |
| 23 | SP | CV ⁺ and CV ⁻ pin input signal single-end output. |
| 24 | SPI | Spindle amplifier input. |
| 25 | SPG | 12 cm spindle mode gain setting resistor connection pin. |
| 26 | SP ⁻ | Spindle phase compensation constant connection pin, along with the SPD pin. |
| 27 | SPD | Spindle control signal output pin. |
| 28 | SLEQ | Sled phase compensation constant connection pin. |
| 29 | SLD | Sled control signal output pin. |
| 30 | SL ⁻ | Input pin for sled movement signal from microprocessor. |
| 31 | SL ⁺ | Input pin for sled movement signal from microprocessor. |
| 32 | JP ⁻ | Input pin for tracking jump signal from DSP. |
| 33 | JP ⁺ | Input pin for tracking jump signal from DSP. |
| 34 | TGL | Input pin for tracking gain control signal from DSP. Gain is low when TGL is high. |
| 35 | TOFF | Input pin for tracking off control signal from DSP. Tracking servo is off when TOFF is high. |
| 36 | TES | Output pin for TES signal to DSP. |
| 37 | HFL | The High Frequency Level is used to determine whether the main beam is positioned over a bit or over the mirrored surface. |
| 38 | SLOF | Sled servo off control input pin |
| 39 | CV ⁻ | Input pin for CLV error signal from DSP. |
| 40 | CV ⁺ | Input pin for CLV error signal from DSP. |
| 41 | RFSM | RF output pin. |
| 42 | RFS ⁻ | RF gain setting and EFM signal 3T compensation constant setting pin, along with the RFSM pin. |
| 43 | SLC | Slice Level Control is an output pin that controls the data slice level used by the DSP for the RF waveform. |
| 44 | SLI | Input pin used by DSP for controlling the data slice level. |
| 45 | DGND | Digital system GND pin. |
| 46 | VC ⁻ | VCO control amplifier input pin. Configures PLL loop filter along with VCOC and PDO of DSP. |
| 47 | VCOC | VCO control output pin. |
| 48 | VCO | VCO output pin. |
| 49 | DEF | Disc defect detection output pin. |
| 50 | CLK | Reference clock input pin. 4.23 MHz signal from the DSP is input. |
| 51 | CL | Microprocessor command clock input pin. |

Continued on next page.

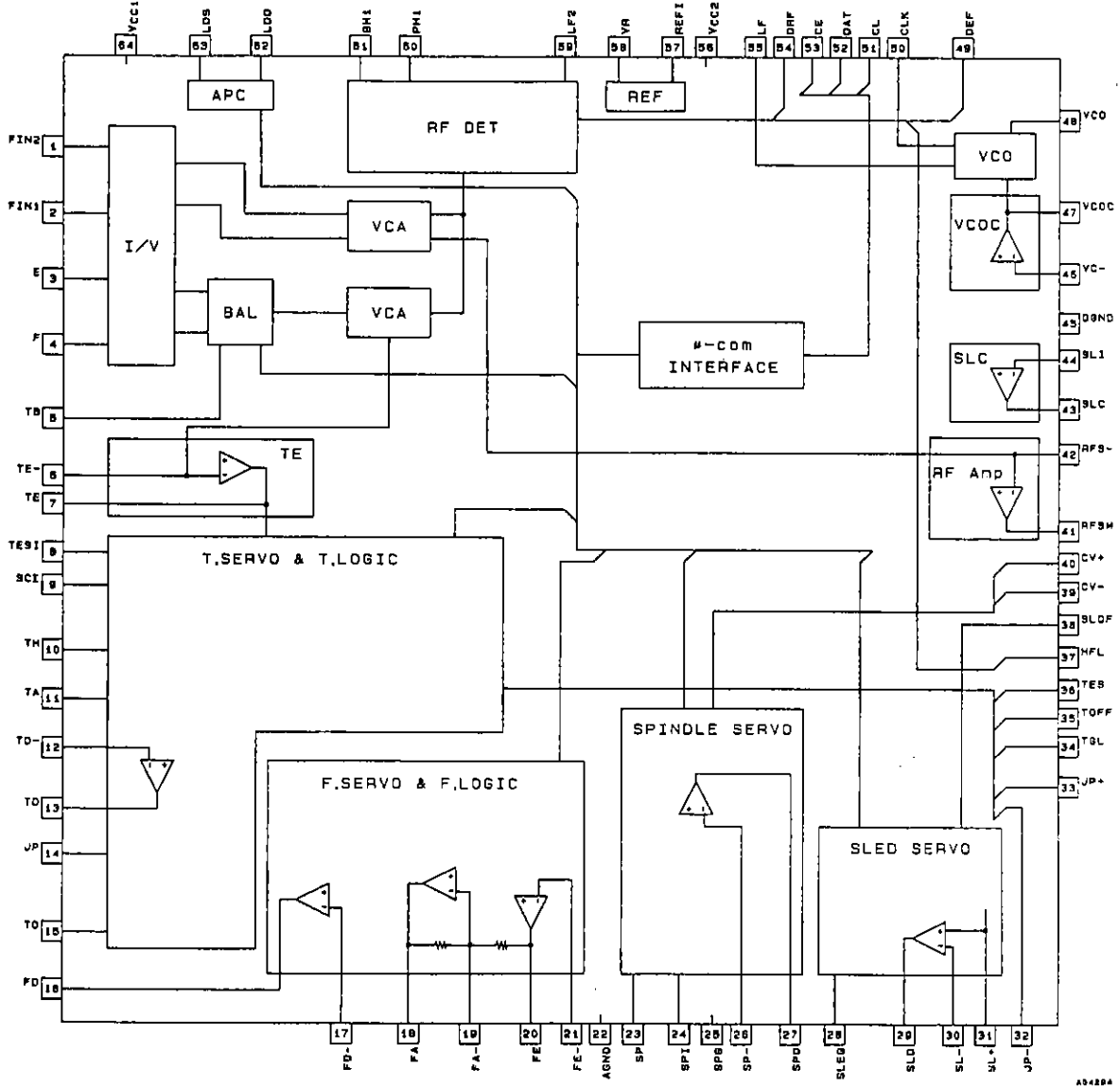
LA9220M

Continued from preceding page.

| Pin No. | Symbol | Contents |
|---------|------------------|--|
| 52 | DAT | Microprocessor command data input pin. |
| 53 | CE | Microprocessor command chip enable input pin. |
| 54 | DRF | RF level detection output (Detect RF). |
| 55 | LF | VCO free-running adjustment pin. |
| 56 | V _{CC2} | Servo system and digital system V _{CC} pin. |
| 57 | REF1 | Bypass capacitor connection pin for reference voltage. |
| 58 | VR | Reference voltage output pin. |
| 59 | LF2 | Disc defect detection time constant setting pin. |
| 60 | PH1 | RF signal peak hold capacitor connection pin. |
| 61 | BH1 | RF signal bottom hold capacitor connection pin. |
| 62 | LDD | APC circuit output pin. |
| 63 | LDS | APC circuit input pin. |
| 64 | V _{CC1} | RF system V _{CC} pin. |

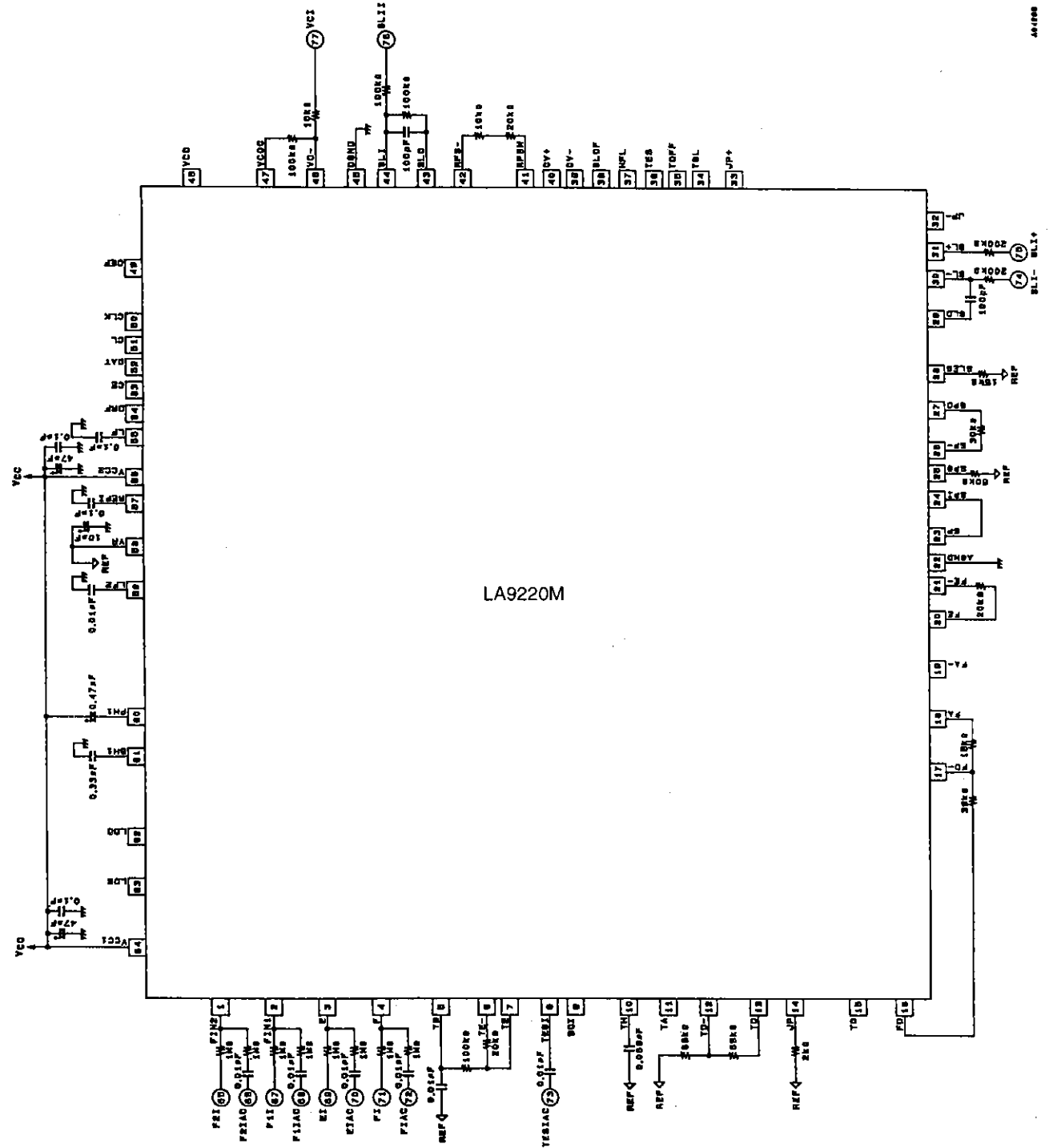
LA9220M

Block Diagram



LA9220M

Test Circuit



LA9220M

Description of Operation

- **APC (auto laser power control)**
This circuit controls the pickup laser power. The laser is turned on and off by commands from the microprocessor.
- **RF amplifier (eye pattern output)**
The pickup photodiode output current ($A + C$) is input to FIN2 (pin 1), and ($B + D$) is input to FIN1 (pin 2). The current that is input is converted to the voltage, passes through the AGC circuit, and is then output from the RFSM amplifier output RFSM (pin41). The internal AGC circuit has a variable range of ± 3 dB, and the time constant can be changed through the external capacitor connected to PH1 (pin 60). In addition, this circuit also controls the bottom level of the EFM signal (RFSM output), and the response can be changed through the external capacitor connected to BH1 (pin 61). The center gain setting for the AGC variable range is set by the resistance between RFSM (pin 41) and RFS⁻ (pin 42); if necessary, this resistance is also used for 3T compensation for the EFM signal.
- **SLC (slice level control)**
The SLC sets the duty ratio for the EFM signal that is input to the DSP to 50%. The DC level is determined by integrating the EFMO signal output from the DSP to determine the duty ratio.
- **Focus servo**
The focus error signal is derived by detecting the difference between ($A + C$) and ($B + D$), which is $(B + D) - (A + C)$, and is then output from FE (pin 20). The focus error signal gain is set by the resistance between FE (pin 20) and FE⁻ (pin 21). The FA amplifier is the pickup phase compensation amplifier, and the equalizer curve is set by the external capacitor and resistance. Furthermore, this amplifier has a mute function which is applied when V_{CC} is turned on, when the F-SERVO OFF command is sent, and during F-SEARCH. In order to turn the focus servo on, send either the LASER ON command or the F-SERVO ON command.
The FD amplifier has a phase compensation circuit, a focus search signal composition function, and an offset cancellation function. Focus search is initiated by the F-SEARCH command, and a ramp waveform is generated by the internal clock. This waveform is used for focus detection (focus zero cross) with the focus error signal and then turn the focus servo on. The ramp waveform amplitude is set by the resistance between FD (pin 16) and FD⁻ (pin 17). Offset cancellation cancels the IC offset; adjustment is started by the FOCUS-OFFSET ADJUST START command, and is completed in about 250ms.
To cancel even the offset for the IV amplifier, etc., it is necessary to send the F-SERVO ON (LASER OFF) command. The FOCUS-OFFSET ADJUST OFF command is used to return to the state prior to offset cancellation.
- **Tracking servo**
The pickup photodiode output current is input to E (pin 3) and F (pin 4). The current that is input is converted to the voltage, passes through the balance adjustment VCA circuit and then the VCA circuit that follows the gain in the RFAGC circuit, and is then output from TE (pin 7). The tracking error gain is set by the resistance between TE⁻ (pin6) and TE (pin7).
The TH amplifier alters the servo response characteristics according to the THLD signal, etc., generated internally after detection of the TGL signal from the DSP or the JP signal. When a defect is detected, the THLD mode goes into effect internally. To avoid this, short DEF (pin 49) to L = GND. By inserting an external bandpass filter to remove the shock component from the tracking error signal at SCI (pin 9), the gain is automatically boosted when a defect is detected.
The TOFF amplifier that is positioned immediately after TD (pin 13) functions to turn off the servo in response to the TOFF signal from the DSP.
The TD amplifier performs servo loop phase compensation; the characteristics are set by external CR. Furthermore, this amplifier has a mute function, which is applied when V_{CC} is turned on or the TRACK-SERVO OFF command is issued. The muting function is released by the TRACK-SERVO ON command.
The TO amplifier has a JP pulse composition function and a tracking offset cancellation function. The JP pulse is set by JP (pin 14). (THLD detection is performed internally.) Offset cancellation is completed in about 30 ms. The TRACK-SERVO ON command and setting the TOFF pin (pin 35) low are required for offset cancellation.
Note: The LC78681KE TOFF ON/OFF command is valid only when disc motor control is in CLV mode. Accordingly, tracking offset is cancelled in normal CLV mode. Note that when performed in STOP mode, external control of the TOFF pin is required.
- **Sled servo**
The response characteristics are set by SLEQ (pin 28). The amplifier positioned after SLEQ (pin 28) has a mute function that is applied either when SLOF (pin 38) goes high or the SLED OFF command is issued. The sled is moved by inputting current to SL⁻ (pin 30) and SL⁺ (pin 31); specifically, the pins are connected to the microprocessor output ports via resistors, and the movement gain is set by the resistance value of that resistor. It is important to note that if there is a deviation in the resistance values for SL⁻ (pin 30) and SL⁺ (pin 31), an offset will arise in the SLD output.

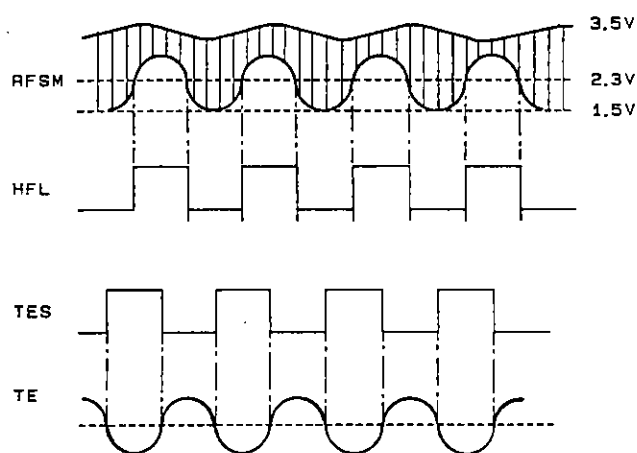
LA9220M

- Spindle servo

This configures the servo circuit, which maintains the linear velocity of the disc at a constant speed, along with the DSP. This circuit accepts signals from the DSP through CV⁻ (pin 39) and CV⁺ (pin 40) and sets the equalizer characteristics through SP (pin 23), SP⁻ (pin 36), and SPD (pin 27), which are output to SPD (pin 27). The 12-cm mode amplifier gain is set by the resistor connected between SPG (pin 25) and the reference voltage. In 8-cm mode, this amplifier serves as an internal buffer, and SPG (pin 25) is ignored. Note that the gain setting is made for 8-cm mode first, and then 12-cm mode. If SPG (pin 25) is left open, the gain is forcibly set for 8-cm mode, regardless of whether 8-cm or 12-cm mode is in effect.

- TES and HFL (traverse signals)

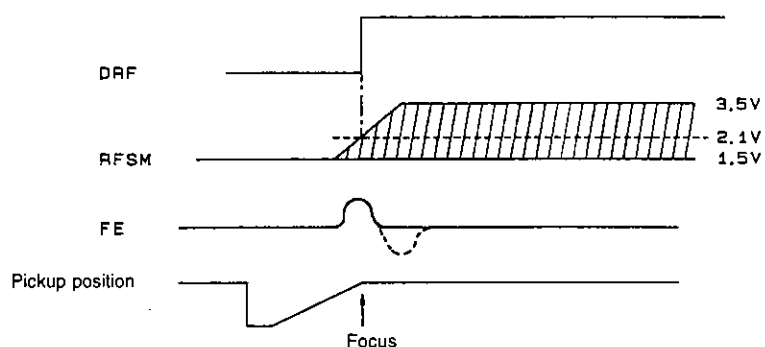
When moving the pickup from the outer track to the inner track, the EF output from the pickup must be connected so that the phase relationship of TES and HFL is as shown in the diagram below. For the TES1 input, the TES comparator has negative polarity and hysteresis of approximately ± 100 mV. An external bandpass filter is needed in order to extract only the required signal from the TE signal.



A04297

- DRF (luminous energy determination)

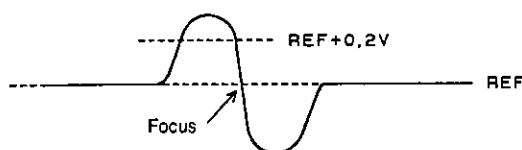
DRF goes high when the peak of the EFM signal (RFSM output) held by the PH1 (pin 60) capacitor exceeds approximately 2.1 V. The PH1 (pin 60) capacitor affects the DRF detection time constant and the RFAGC response bidirectional setting.



A04298

- Focus determination

Focus is assumed to be obtained when the focus error signal "S" curve reaching REF + 0.2 V is detected, and the "S" curve subsequently returns to REF.

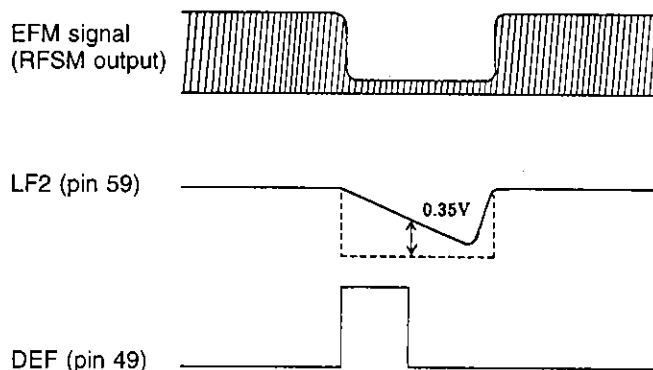


A04299

LA9220M

- **DEFECT**

The mirrored surface level is maintained by the capacitor for LF2 (pin 59); when a drop in the EFM signal (RFSM output) reaches 0.35 V or more, a high signal is output to DEF (pin 49). If DEF (pin 49) goes high, the tracking servo enters THLD mode. In order to prevent the tracking servo from entering THLD mode when a defect is detected, prevent DEFECT from being output by either shorting DEF (pin 49) to GND, or shorting LF2 (pin 59) to GND. The DEFECT output is driven by constant current (approximately 100 μ A).



- V_{CC} /REF/GND
 - V_{CC} 1 (pin 64) : RF system
 - V_{CC} 2 (pin 56) : SERVO system, DIGITAL system
 - AGND (pin 22) : RF system, SERVO system
 - DGND (pin 45) : DIGITAL system

A04300

- **PLL circuit**

VCOC is the loop filter setting amplifier for the EFM signal PLL, and equalizes the PLL phase comparison output from the DSP, and outputs it to the internal VCO.

VCO is the VCO circuit for the EFM signal PLL, and requires the reference clock from the DSP (4.23 MHz only; does not support 2.1609 MHz for the LC7860KA, etc.). The VCO free-running frequency can be varied according to the current input to LF (pin 55). The VCO output can be turned on or off by using the VCO-OUT ON/OFF command.

| Command | VCO output frequency |
|--------------|----------------------|
| Normal speed | Average: 8.6436 MHz |
| Double speed | Average: 17.2872 MHz |

- **Reset circuit**

The power-on reset is released when V_{CC} exceeds approximately 2.8 V.

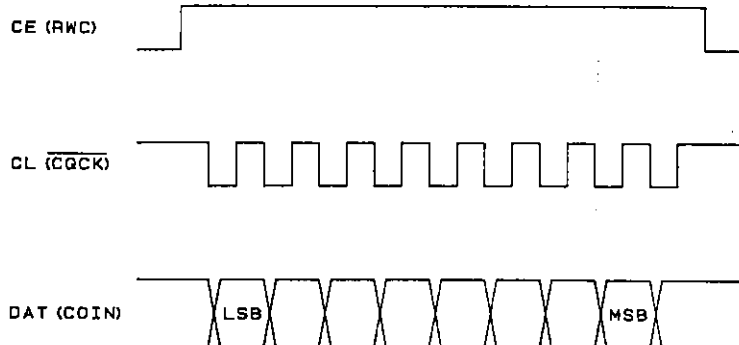
- **Microprocessor interface**

Because the Reset (Nothing) command initializes the LA9220M, it must be used carefully.

The LA9220M command acceptance (mode switching) timing is defined by the internal clock (4.23 MHz divided to 130 kHz) after the falling edge of CE (RWC); therefore, when commands are sent consecutively, CE must go low for at least 10 μ s. For this reason, the 4.23 MHz clock is required even when VCO of LA9220M is not used. 2BYTE-COMMAND RESET is used only for the purpose of masking two-byte data.

All instructions can be input by setting CE high and sending commands synchronized with the CL clock from the microprocessor to DAT (pin 52) in LSB first format. Note that the command is executed at the falling edge of CE.

Timing chart



*The DSP pin names are shown in parentheses.

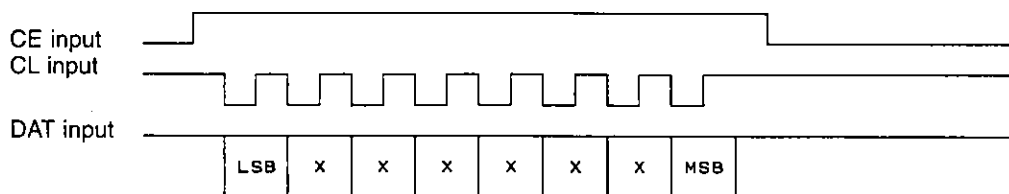
A04301

LA9220M

Command List

| MSB | LSB | Command | Reset mode Power on mode | DSP |
|-----|----------|---------------------------|-----------------------------|------------------------|
| 0 | 0000000 | RESET | | RESET(NOTHING) |
| 0 | 0001000 | FOCUS START | | FOCUS START #1 |
| 1 | 0001110 | VCO-OUT ON | ○ | OSC ON |
| 1 | 0001101 | VCO-OUT OFF | | OSC OFF |
| 1 | 1000001 | VCO-2FREQ | | 2TIMES-SPEED PLAY MODE |
| 1 | 1000010 | VCO-NORMAL | ○ | NORMAL-SPEED PLAY MODE |
| 1 | 11110000 | 2BYTE-COMMAND DETECT | | 2BYTE-COMMAND DETECT |
| 1 | 11111000 | 2BYTE-COMMAND DETECT | | 2BYTE-COMMAND DETECT |
| 1 | 11111111 | 2BYTE-COMMAND RESET | | 2BYTE-COMMAND RESET |
| | | | | |
| 1 | 0010000 | FOCUS-OFFSET ADJUST START | | — |
| 1 | 0010001 | FOCUS-OFFSET ADJUST OFF | ○ | — |
| 1 | 0010010 | TRACK-OFFSET ADJUST START | | — |
| 1 | 0010011 | TRACK-OFFSET ADJUST OFF | ○ | — |
| 1 | 0010100 | LASER ON | | — |
| 1 | 0010101 | LASER OFF : F-SERVO ON | | — |
| 1 | 0010110 | LASER OFF : F-SERVO OFF | ○ | — |
| 1 | 0010111 | SPINDLE 8CM | | — |
| 1 | 0011000 | SPINDLE 12 CM | ○ | — |
| 1 | 0011001 | SPINDLE OFF | | — |
| 1 | 0011010 | SLED ON | ○ | — |
| 1 | 0011011 | SLED OFF | | — |
| 1 | 0011100 | E/F BALANCE START | Nonadjusted | — |
| 1 | 0011101 | TRACK-SERVO OFF | ○ | — |
| 1 | 0011110 | TRACK-SERVO ON | | — |

Timing chart



LA9220M

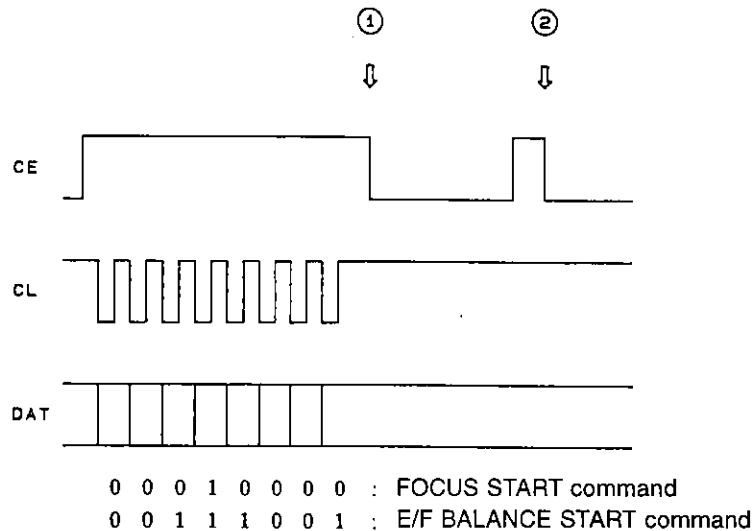
Notes Concerning Microprocessor Program Creation (Supplementary)

1. Commands .

After sending the FOCUS START command and the E/F BALANCE START command, send 11111110 (FEH) in order to clear the internal registers of the IC. MSB LSB

Reason: Although the above commands are executed at point ① in the timing chart below, the same commands will be executed again at point ② if there is subsequent input to CE as shown below.

Timing chart



A04303

- When sending the TRACK-OFFSET ADJUST START command or the FOCUS-OFFSET ADJUST START command after either the V_{CC} ON (POWER ON RESET), RESET command or a corresponding OFFSET ADJUST OFF command, waiting time is necessary as listed below. (Only when a 4.2 MHz clock is input.)

TRACK-OFFSET ADJUST START: 4 ms or more

FOCUS-OFFSET ADJUST START: 30 ms or more

3. E/F balance adjustment

E/F balance adjustments should be made in a bit region of the disc, not a mirrored region.

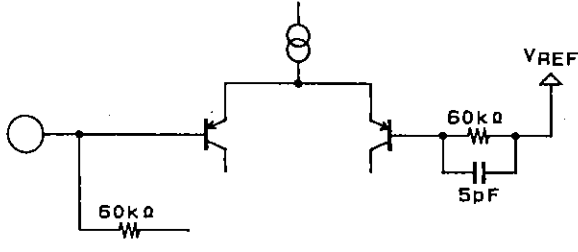
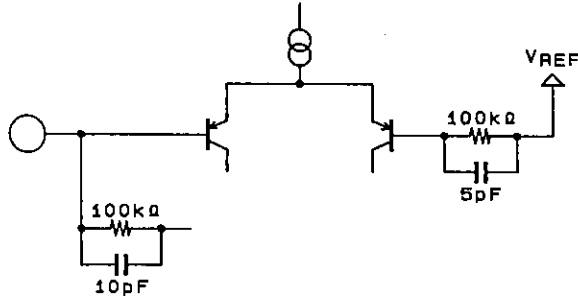
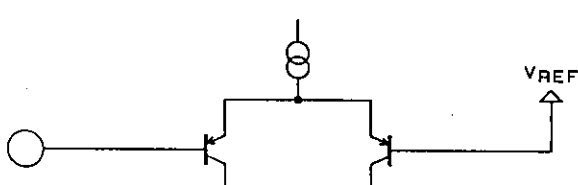
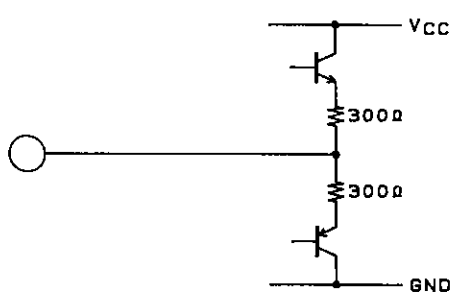
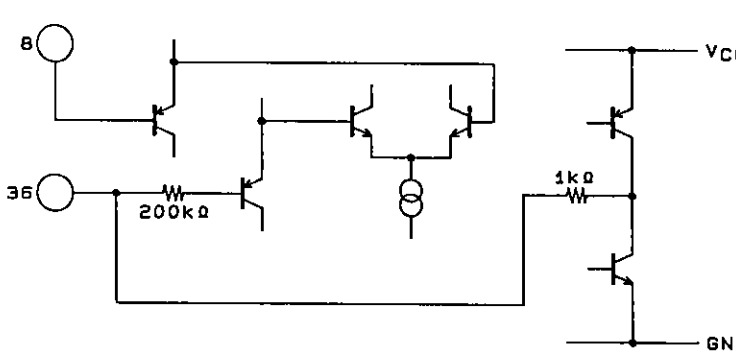
(This is because the E/F balance adjustment entails about 100 to 200 track kicks.)

Pattern Design Notes

To prevent signal jump-in from CV⁺ (pin 40) to RFSM (pin 41), a shielding line is necessary in between.

LA9220M

Pin Internal Equivalent Circuit

| Pin No., (): Pin Name | Internal Equivalent Circuit |
|---|---|
| Pin 1 (FIN2) Pin 2 (FIN1) |  <p style="text-align: right;">A04508</p> |
| Pin 3 (E) Pin 4 (F) |  <p style="text-align: right;">A04509</p> |
| Pin 5 (TB) Pin 6 (TE ⁻) Pin 17 (FD ⁻) Pin 21 (FE ⁻) Pin 26 (SP ⁻) Pin 28 (SLEQ) Pin 44 (SLI) Pin 46 (VC ⁻) |  <p style="text-align: right;">A04510</p> |
| Pin 16 (FD) Pin 27 (SPD) Pin 43 (SLC) |  <p style="text-align: right;">A04511</p> |
| Pin 8 (TESI) Pin 36 (TES) |  <p style="text-align: right;">A04512</p> |

Continued on next page.

LA9220M

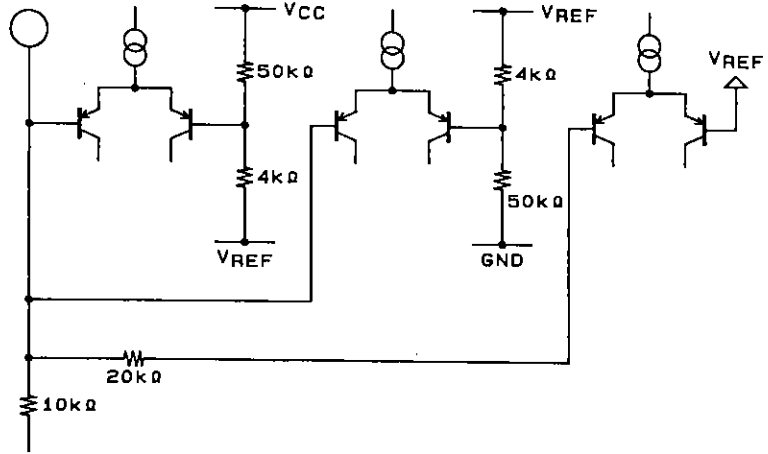
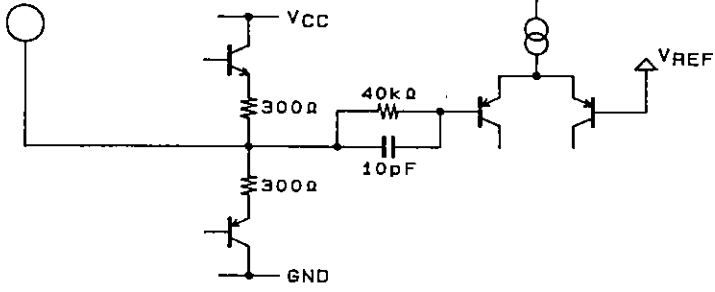
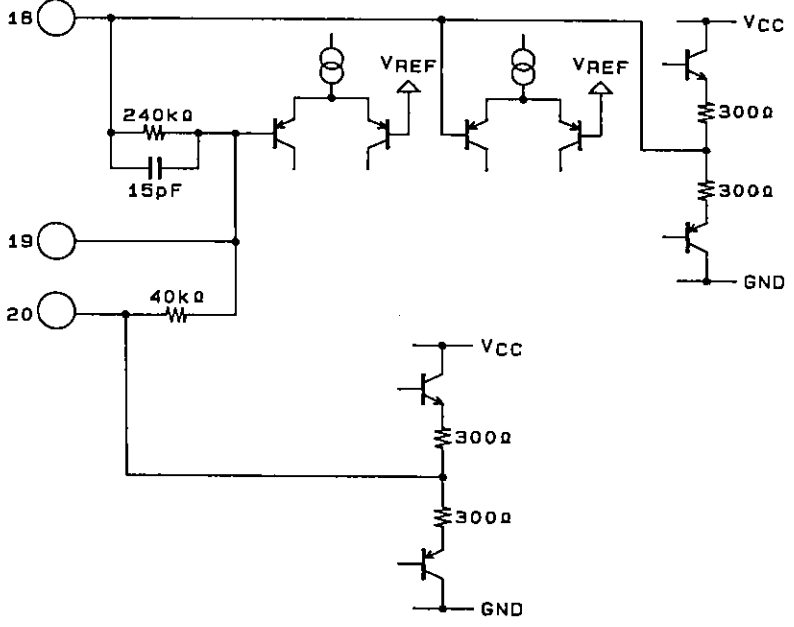
Continued from preceding page.

| Pin No., (): Pin Name | Internal Equivalent Circuit |
|-----------------------------|--|
| Pin 9 (SCI) Pin 34 (TGL) | <p style="text-align: right;">A04513</p> |
| Pin 7 (TE) Pin 10 (TH) | <p style="text-align: right;">A04514</p> |
| Pin 11 (TA) Pin 12 (TD-) | <p style="text-align: right;">A04515</p> |
| Pin 13 (TD) | <p style="text-align: right;">A04516</p> |

Continued on next page.

LA9220M

Continued from preceding page.

| Pin No., (): Pin Name | Internal Equivalent Circuit |
|---|---|
| Pin 14 (JP) |  <p style="text-align: right; margin-top: 10px;">A04517</p> |
| Pin 15 (TO) |  <p style="text-align: right; margin-top: 10px;">A04518</p> |
| Pin 18 (FA) Pin 19 (FA ⁻) Pin 20 (FE) |  <p style="text-align: right; margin-top: 10px;">A04519</p> |

Continued on next page.

LA9220M

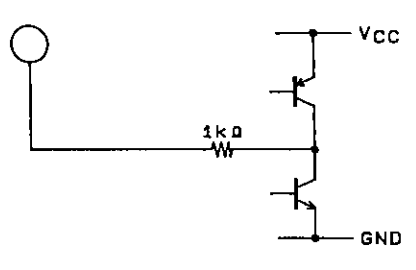
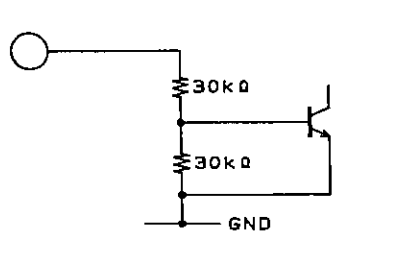
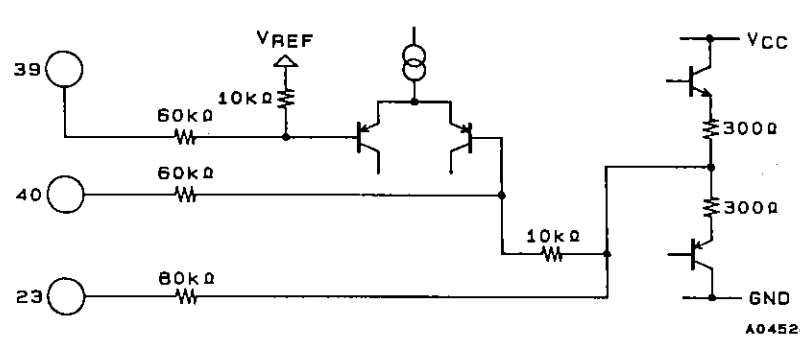
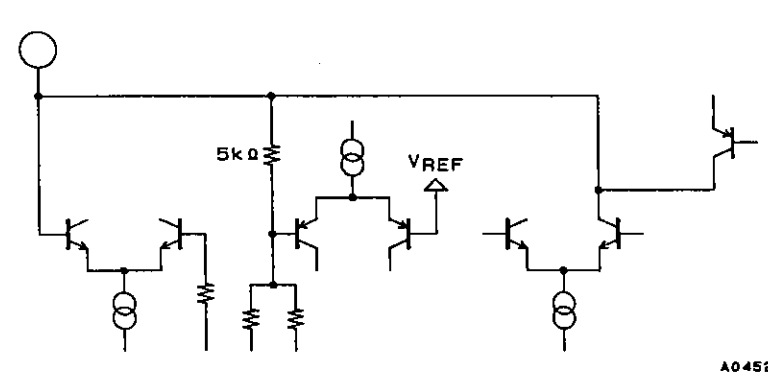
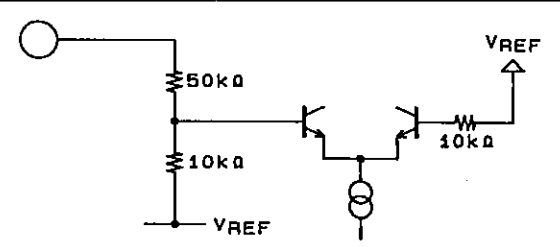
Continued from preceding page.

| Pin No., (): Pin Name | Internal Equivalent Circuit |
|--|--|
| Pin 24 (SPI) Pin 25 (SPG) | <p style="text-align: right;">A04520</p> |
| Pin 29 (SLD) Pin 30 (SL ⁻) Pin 31 (SL ⁺) | <p style="text-align: right;">A04521</p> |
| Pin 32 (JP ⁻) Pin 33 (JP ⁺) | <p style="text-align: right;">A04522</p> |
| Pin 35 (TOFF) | <p style="text-align: right;">A04523</p> |

Continued on next page.

LA9220M

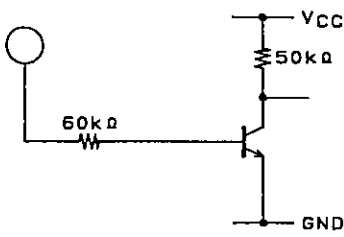
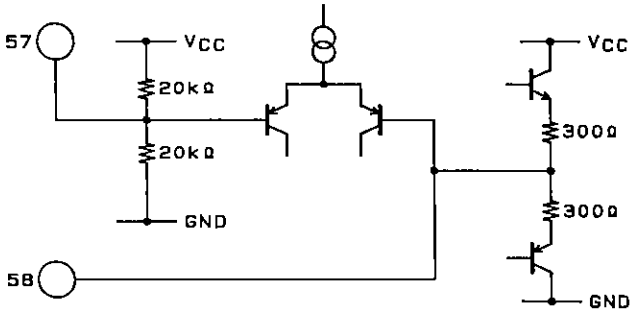
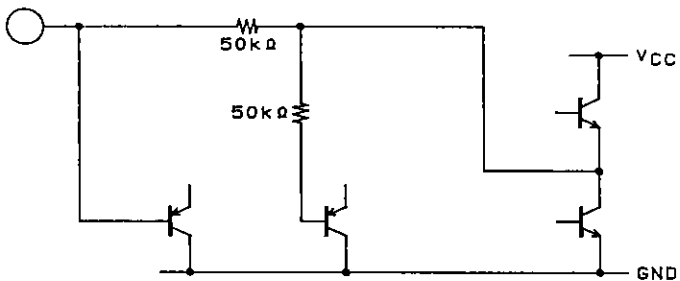
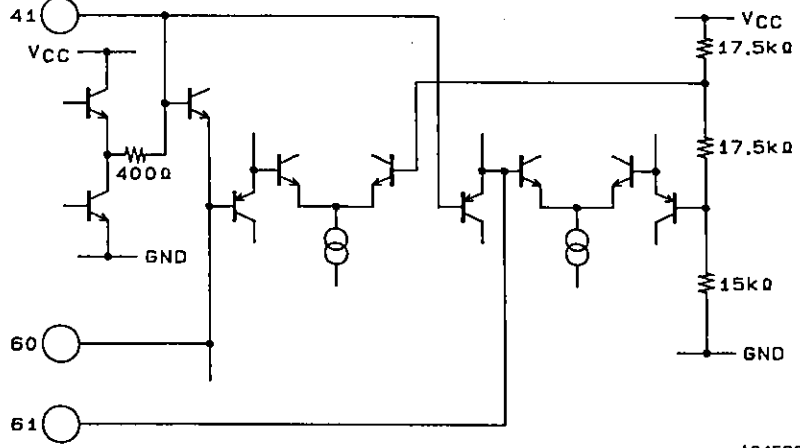
Continued from preceding page.

| Pin No., (): Pin Name | Internal Equivalent Circuit |
|---|---|
| Pin 37 (HFL) Pin 49 (DEF) Pin 54 (DRF) |  <p style="text-align: right;">A04524</p> |
| Pin 38 (SLOF) |  <p style="text-align: right;">A04525</p> |
| Pin 39 (CV ⁻) Pin 40 (CV ⁺) Pin 23 (SP) |  <p style="text-align: right;">A04526</p> |
| Pin 42 (RF ⁻) |  <p style="text-align: right;">A04527</p> |
| Pin 50 (CLK) |  <p style="text-align: right;">A04557</p> |

Continued on next page.

LA9220M

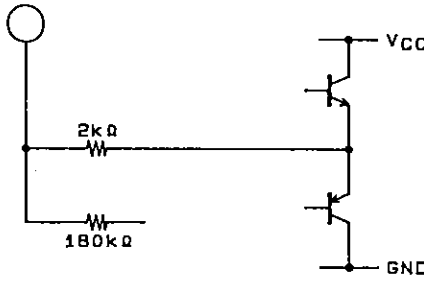
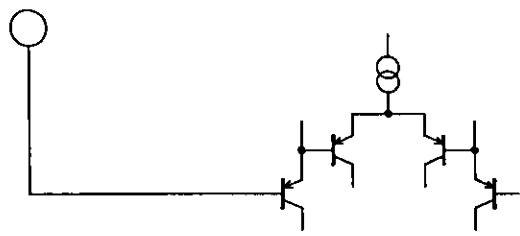
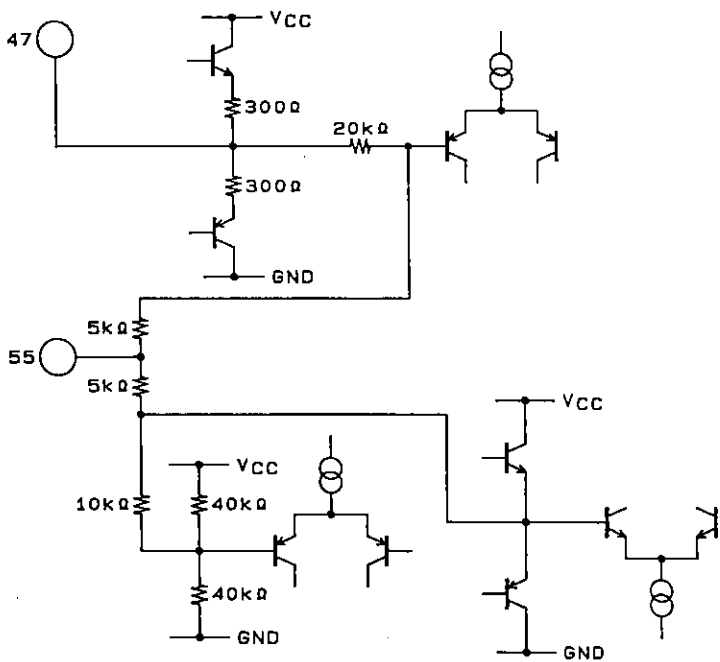
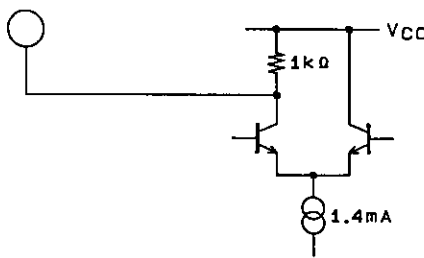
Continued from preceding page.

| Pin No., (): Pin Name | Internal Equivalent Circuit |
|---|---|
| Pin 51 (CL) Pin 52 (DAT) Pin 53 (CE) |  <p style="text-align: right; margin-top: 10px;">A04529</p> |
| Pin 57 (REFI) Pin 58 (VR) |  <p style="text-align: right; margin-top: 10px;">A04530</p> |
| Pin 59 (LF2) |  <p style="text-align: right; margin-top: 10px;">A04531</p> |
| Pin 41 (RFSM) Pin 60 (PH1) Pin 61 (BH1) |  <p style="text-align: right; margin-top: 10px;">A04532</p> |

Continued on next page.

LA9220M

Continued from preceding page.

| Pin No., (): Pin Name | Internal Equivalent Circuit |
|------------------------------|---|
| Pin 62 (LDD) |  <p style="text-align: right;">A04533</p> |
| Pin 63 (LDS) |  <p style="text-align: right;">A04534</p> |
| Pin 47 (VCOC) Pin 55 (LF) |  <p style="text-align: right;">A04535</p> |
| Pin 48 (VCO) |  <p style="text-align: right;">A04536</p> |

LA9220M

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.