Ordering number : ENN7543

Monolithic digital IC

LB11690, 11690H

Pre-Driver IC for Brushless Motor Drive in Electric Bicycles

Overview

The LB11690 and LB11690H are three-phase bipolar PWM drive pre-driver ICs that allow the output circuits to be implemented using only n-channel FETs. These ICs can implement, at low cost, high-efficiency drive circuits in applications that use motors that require high drive currents. These ICs include a built-in Hall sensor signal F/V conversion circuit and can provide a voltage that is proportional to motor speed for use, for example, in speedometers for electric bicycles. These ICs also support use in applications that holds the speed controlled at a constant rate as the load varies.

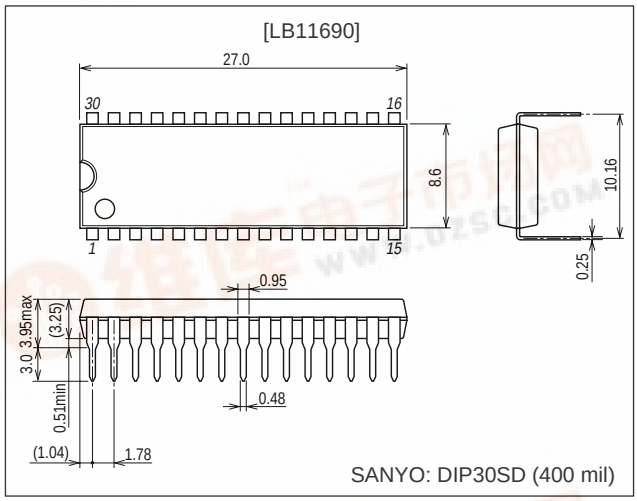
Functions and Features

- Three-phase bipolar PWM drive (high and low side n-channel FET drive)
- Maximum supply voltage: 45 V
- Gate drive voltage: about 10 V (high and low side n-channel FETs)
- Hall sensor signal F/V conversion circuit (one-shot multivibrator output)
- Synthesized three-phase Hall sensor signal output
- Built-in current limiter and undervoltage protection circuits

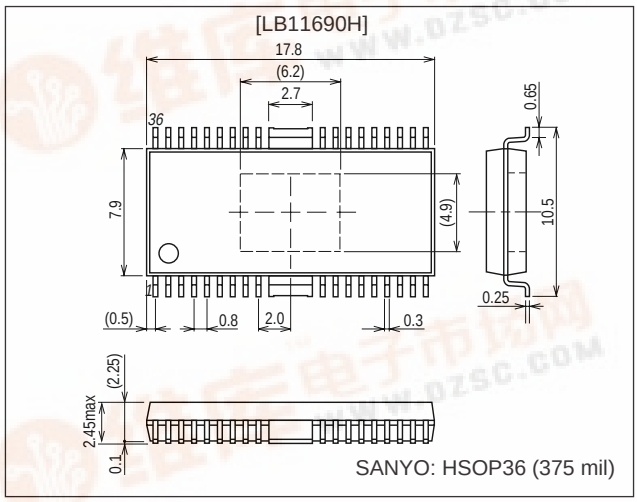
Package Dimensions

unit: mm

3196A-DIP30SD



3235A-HSOP36



Specifications

Absolute Maximum Ratings at Ta = 25°C (Note: Ratings for the LB11690H are preliminary.)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC} max	V_{CC} pin	45	V
Supply voltage 2	VB max	VB pin	60	V
Output current 1-1	I_O max1-1	UL, VL, and WL pins, sink current	40	mA
Output current 1-2	I_O max1-2	UL, VL, and WL pins, source current	30	mA
Output current 2	I_O max2	UH, VH, and WH pins	20	mA
RF pin applied voltage	VRF max		4	V
LVS pin applied voltage	VLVS max		60	V
IN pin applied voltage	V_{IN} max	IN1, IN2, and IN3 pins	V5 + 0.3	V
RES pin applied voltage	VRES max		V5 + 0.3	V
TOC pin applied voltage	VTOC max		V5 + 0.3	V
EI^+ pin applied voltage	VEI^+ max		V5 + 0.3	V
EI^- pin applied voltage	VEI^- max		V5 + 0.3	V
RC pin applied voltage	VRC max		V5 + 0.3	V
FV pin applied voltage	VFV max		V5 + 0.3	V
HP pin applied voltage	VHP max		45	V
Allowable power dissipation	Pd max1	Independent IC (LB11690 and LB11690H)	0.9	W
	Pd max2	Mounted on designated PCB: 114.3 × 76.1 × 1.6 mm, glass epoxy (LB11690H)	2.1	W
Operating temperature	Topr		–20 to +100	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_{CC}	V_{CC} pin	15 to 42	V
Supply voltage range 2	VB	VB pin	V_{CC} + 13	V
Output current 1-1	I_{OUT}1-1	UL, VL, and WL pins, sink current	30	mA
Output current 1-2	I_{OUT}1-2	UL, VL, and WL pins, source current	–25	mA
Output current 2-1	I_{OUT}2-1	UH, VH, and WH pins, sink current	15	mA
Output current 2-2	I_{OUT}2-2	UH, VH, and WH pins, source current	–15	mA
12 V constant voltage output current	I_{12REG}		–30	mA
5 V constant voltage output current	I_{5REG}		–30	mA
HP pin applied voltage	V_{HP}		0 to 42	V
HP pin output current	I_{HP}		0 to 5	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 36 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}			15	20	mA
[5 V Constant Voltage Output (V5 pin)]						
Output voltage	V_{5REG}	I_O = –5 mA	4.7	5.0	5.3	V
Line regulation	$\Delta V_{5REG}1$	V_{CC} = 15 to 42 V		40	100	mV
Load regulation	$\Delta V_{5REG}2$	I_O = –5 to –30 mA		10	30	mV
Temperature coefficient	$\Delta V_{5REG}3$	Design target value*		0		mV/°C

Note :*Design target values and are not tested.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[12 V Constant Voltage Output (V12 pin)]						
Output voltage	V_{12REG}	I_O = – 5 mA	11.2	12.0	12.8	V
Line regulation	$\Delta V_{12REG}1$	V_{CC} = 15 to 42 V		120	240	mV
Load regulation	$\Delta V_{12REG}2$	I_O = –5 to –30 mA		10	30	mV
Temperature coefficient	$\Delta V_{12REG}3$	Design target value*		0		mV/°C
[Output Block] Conditions: U_{OUT} = V_{OUT} = W_{OUT} = 18 V, when 48 V is applied to VB						
Output high level voltage 1	$V_{OH}1$	UL, VL, and WL pins, I_{OH} = –10 mA	V12 – 1.2	V12 – 0.8		V
Output low level voltage 1	$V_{OL}1$	UL, VL, and WL pins, I_{OL} = 10 mA		0.8	1.2	V
Output high level voltage 2	$V_{OH}2$	UH, VH, and WH pins, I_{OH} = –5 mA	46.8	47.2		V
Output low level voltage 2	$V_{OL}2$	UH, VH, and WH pins, I_{OL} = 5 mA		18.2	18.6	V
[Charge Pump Output (VB pin)]						
Output voltage	VB_{OUT}		46.0	48.0	50.5	V
[CP1 Pin]						
Output high level voltage	V_{OH} (CP1)	ICP1 = –2 mA	V_{CC} – 1.9	V_{CC} – 1.4		V
Output low level voltage	V_{OL} (CP1)	ICP1 = 2 mA		1.5	2.0	V
[Integrating Amplifier]						
Input offset voltage	VIO (CONT)		–10		+10	mV
Input bias current	IB (CONT)		–1		+1	µA
Common-mode input voltage range	VICM		0		V5 – 1.7	V
Output high level voltage	V_{OH} (CONT)	ITOC = –0.2 mA	V5 – 1.1	V5 – 0.8		V
Output low level voltage	V_{OL} (CONT)	ITOC = 0.2 mA		0.8	1.1	V
Open-loop gain		f (CONT) = 1 kHz	45	51		dB
[PWM Oscillator (PWM pin)]						
Output high level voltage	V_{OH} (PWM)		2.75	3.0	3.25	V
Output low level voltage	V_{OL} (PWM)		1.0	1.2	1.3	V
External capacitor charge current	ICHG	VPWM = 2.1 V	–35	–25	–19	µA
Oscillator frequency	f (PWM)	C = 270 pF	31	39	48	kHz
Amplitude	V (PWM)		1.6	1.8	2.1	Vp-p
[TOC Pin]						
Input voltage 1	VTOC1	Output duty: 100%	2.72	3.0	3.30	V
Input voltage 2	VTOC2	Output duty: 0%	0.99	1.2	1.34	V
Input voltage 1L	VTOC1L	Design target value*, 100% when V5 = 4.7 V	2.72	2.80	2.90	V
Input voltage 2L	VTOC2L	Design target value*, 0% when V5 = 4.7 V	0.99	1.08	1.17	V
Input voltage 1H	VTOC1H	Design target value*, 100% when V5 = 5.3 V	3.08	3.20	3.30	V
Input voltage 2H	VTOC2H	Design target value*, 0% when V5 = 5.3 V	1.11	1.22	1.34	V
[Current Limiter Circuit (RF pin)]						
Limit voltage	VRF		85	100	115	V

Note :*Design target values and are not tested.

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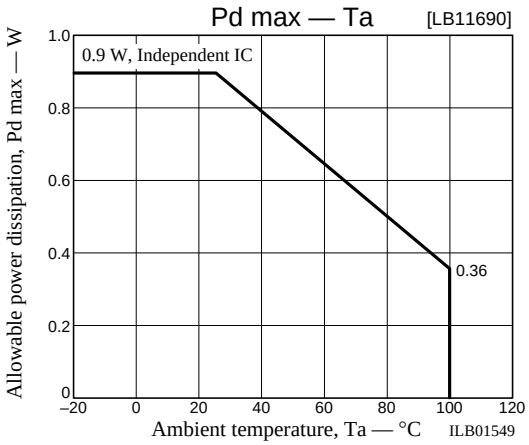
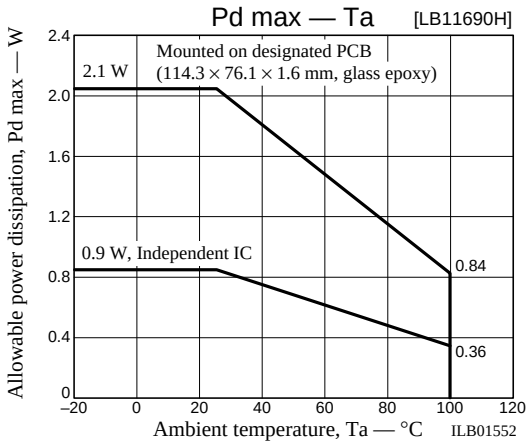
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Undervoltage Protection Circuit (LVS pin)]						
Operating voltage	VSDL		3.6	3.8	4.0	V
Release voltage	VSDH		4.1	4.3	4.5	V
Hysteresis	ΔVSD		0.35	0.5	0.65	V
[Reset Circuit (RES pin)]						
Reset operating voltage	VRESL		1.17	1.27	1.37	V
Reset release voltage	VRESH		1.37	1.5	1.63	V
Hysteresis	ΔVRES		0.2	0.23	0.26	V
[HP Pin]						
Output saturation voltage	VHPL	I_O = 3 mA		0.15	0.5	V
Output leakage current	IHP leak	VHP = 42 V			10	μA
[RC Pin]						
Output high level voltage	V_{OH} (RC)		3.12	3.4	3.68	V
Output low level voltage	V_{OL} (RC)		0.73	0.8	0.87	V
Clamp voltage	VCLP (RC)			1.5		V
[FV Pin]						
Charge current	ICHG1	VFV = 2.5 V	–420	–300	–230	μA
Discharge current	ICHG2	VFV = 1 V	1.3	2.5	5.0	mA
[IN1, IN2, and IN3 Pins]						
Input high level voltage	V_{IH} (IN)		4.0		V5	V
Input low level voltage	V_{IL} (IN)		0		2.5	V
Input open voltage	V_{IO} (IN)		V5 – 0.5		V5	V
Hysteresis	VIS (IN)		0.55	0.9	1.25	V
Input high level current	I_{IH} (IN)	V_{IN} = V5	–10	0	+10	μA
Input low level current	I_{IL} (IN)	V_{IN} = 0 V		–500		μA



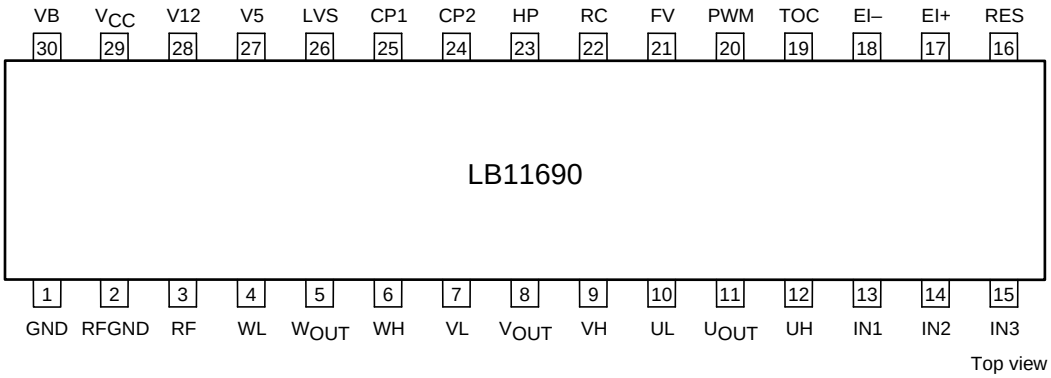


Three-Phase Logic Truth Table

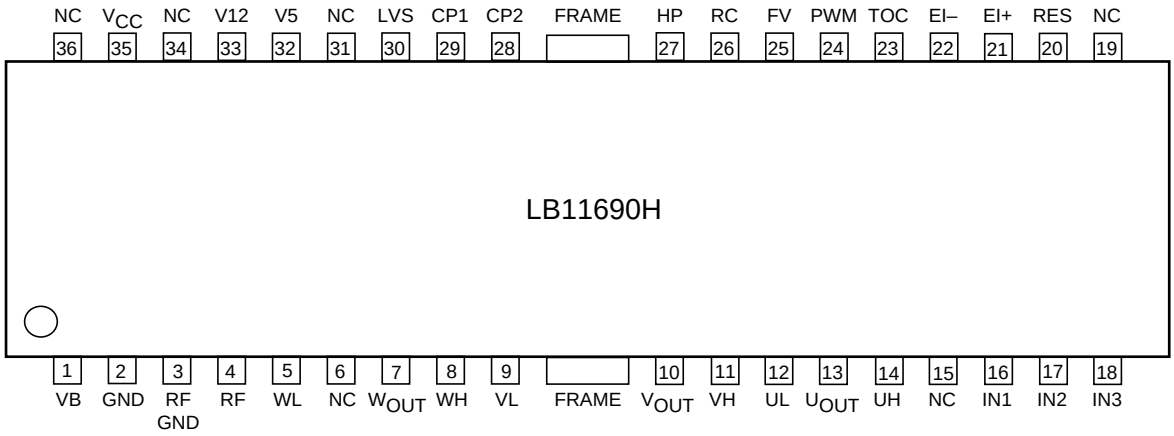
	IN1	IN2	IN3	High side gate	Low side gate	HP
1	H	L	H	VH	UL	H
2	H	L	L	WH	UL	L
3	H	H	L	WH	VL	H
4	L	H	L	UH	VL	L
5	L	H	H	UH	WL	H
6	L	L	H	VH	WL	L

- In the state where the high side gate is VH and the low side gate is VL, the high side FET connected to the VH pin will be on and the low side FET connected to the UL pin will also be on.
- Since the HP output is an open collector output, the high output level is the open state.

Pin Assignments



Top view

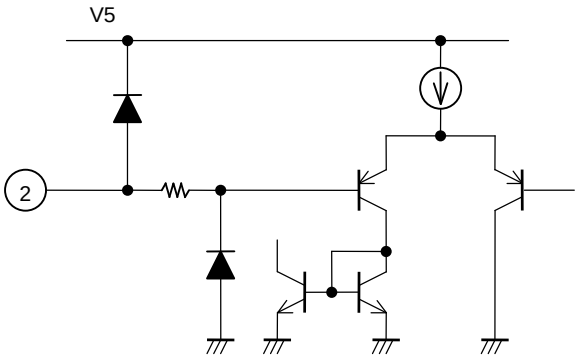
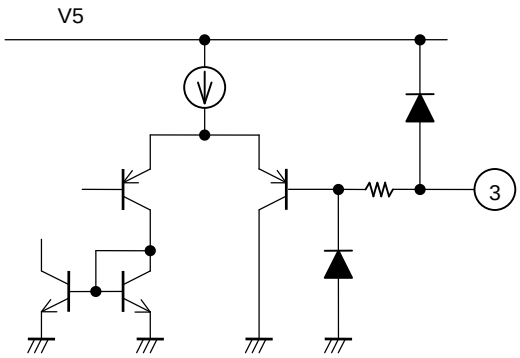
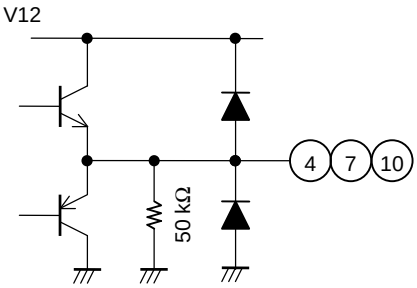
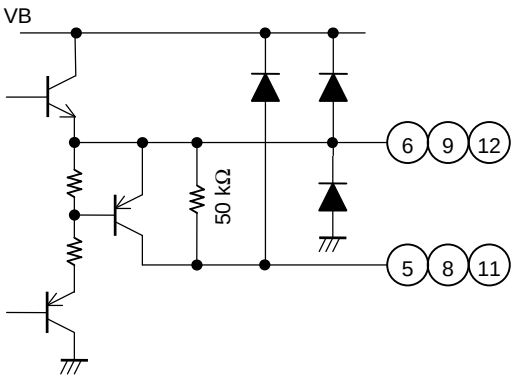


Top view

Pin Functions *: Items in parentheses refer to the LB11690H.

Pin name	Pin No.	Pin description
GND	1 (2)	Ground
RFGND	2 (3)	Ground sensing pin. Connect the ground side of the low-resistance resistor RF connected to the RF pin to this pin.
RF	3 (4)	Output current detection pin. Connect the low-resistance resistor RF between this pin and ground. The output current will be limited to a value determined by the equation I_{OUT} = 0.1/RF. (Current limiter circuit)
WL VL UL	4 (5) 7 (9) 10 (12)	Low side n-channel power FET gate drive output
W_{OUT} V_{OUT} U_{OUT}	5 (7) 8 (10) 11 (13)	High side n-channel power FET source voltage detection
WH VH UH	6 (8) 9 (11) 12 (14)	High side n-channel power FET gate drive output
IN1 IN2 IN3	13 (16) 14 (17) 15 (18)	Hall sensor signal inputs. Insert capacitors between these pins and ground for stabilization.
RES	16 (20)	Reset input. Insert a resistor between this pin and the V5 pin, and a capacitor between this pin and ground.
EI^+	17 (21)	Integrating amplifier noninverting input
EI^-	18 (22)	Integrating amplifier inverting input
TOC	19 (23)	PWM waveform comparison (integrating amplifier output)
PWM	20 (24)	PWM oscillator frequency setting. Insert a capacitor between this pin and ground.
FV	21 (25)	Hall sensor signal one-shot multi-pulse output
RC	22 (26)	Hall sensor signal one-shot multi-pulse amplitude setting. Insert a resistor between this pin and the V5 pin, and a capacitor between this pin and ground.
HP	23 (27)	Hall sensor signal three-phase synthesized output (open collector output)
CP2 CP1	24 (28) 25 (29)	Charge pump capacitor connections. Connect a capacitor between pins CP1 and CP2.
LVS	26 (30)	Undervoltage protection voltage detection. To detect a voltage of 5 V or over, connect a zener diode in series to set the detection voltage.
V5	27 (32)	5 V power supply (control circuit power supply). Insert a capacitor between this pin and ground.
V12	28 (33)	12 V power supply (UL, VL, and WL output block power supply). Insert a capacitor between this pin and ground.
V_{CC}	29 (35)	Power supply. Insert a capacitor between this pin and ground for power supply stabilization.
VB	30 (1)	Charge pump output (UH, VH, and WH output block power supply). Insert a capacitor between this pin and VCC.
(FRAME)	—	The FRAME pin is connected to the IC lower surface metal frame. Both should be left electrically open during operation.
(NC)	(6) (15) (19) (31) (34) (36)	These pins are not connected to the IC internally in the package, and thus may be used for wiring connections.

Pin Functions *: Items in parentheses refer to the LB11690H.

Pin No.	Pin Name	Pin description	Equivalent circuit
1 (2)	GND	Ground	Ground
2 (3)	RF GND	Connect the ground side of the external resistor Rf to this pin.	
3 (4)	RF	Output current detection Connect the low-resistance resistor RF between this pin and ground. The maximum output current is determined by the equation I_{OUT} = 0.1/RF.	
4 (5) 7 (9) 10 (12)	WL VL UL	Outputs (Low side n-channel power FET gate drive outputs) The duty is controlled.	
5 (7) 8 (10) 11 (13)	W_{OUT} V_{OUT} U_{OUT}	Voltage detection (High side n-channel power FET source voltage detection)	
6 (8) 9 (11) 12 (14)	WH VH UH	Outputs (High side n-channel power FET gate drive outputs)	

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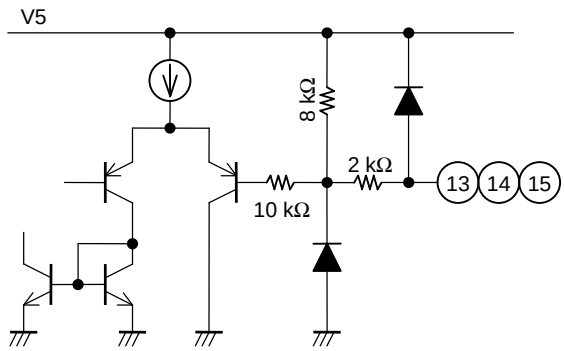
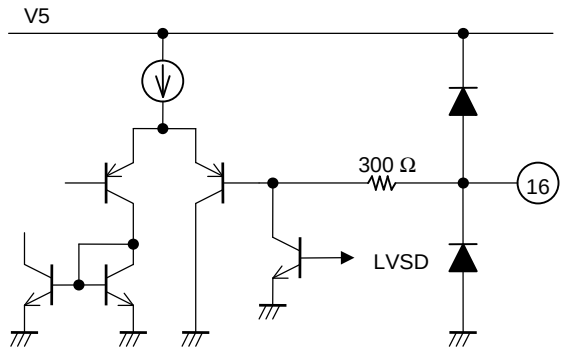
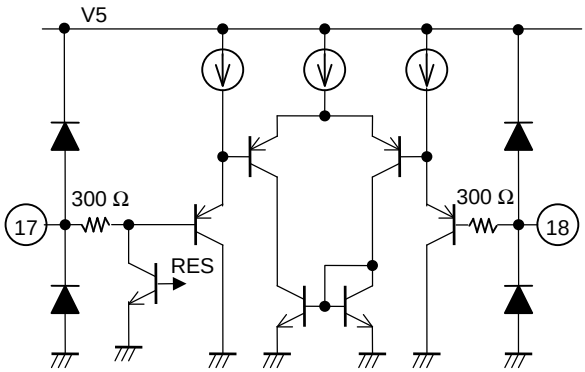
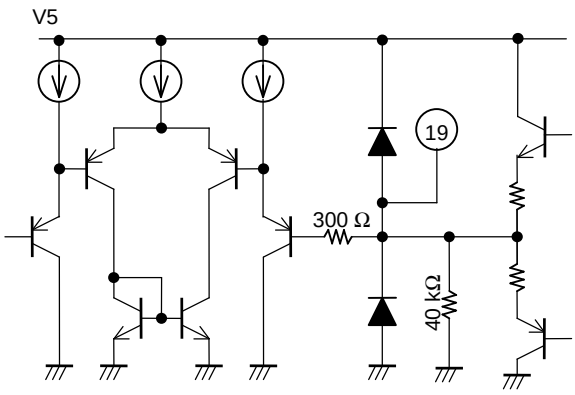
Pin No.	Pin Name	Pin description	Equivalent circuit
13 (16) 14 (17) 15 (18)	IN1 IN2 IN3	Hall sensor signal inputs When open, these pins go to the high level. Insert capacitors between these pins and ground for stabilization.	
16 (20)	RES	Reset	
17 (21)	EI^+	Integrating amplifier noninverting input	
18 (22)	EI^-	Integrating amplifier inverting input	
19 (23)	TOC	Integrating amplifier output (PWM waveform comparison)	

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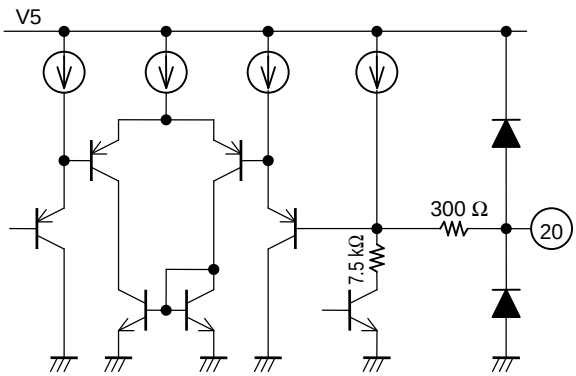
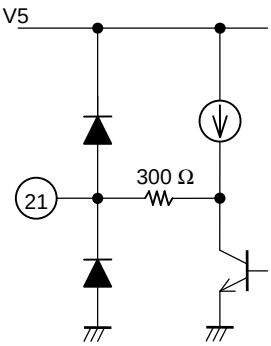
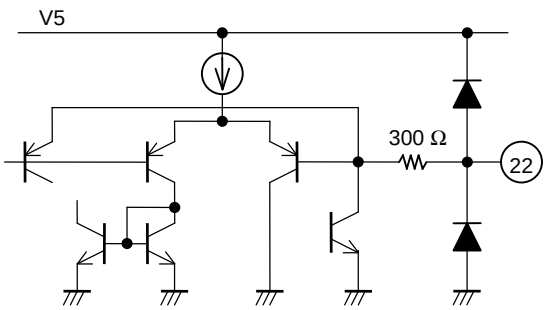
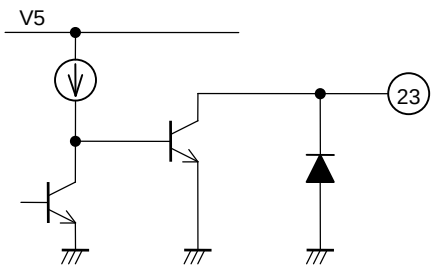
Pin No.	Pin Name	Pin description	Equivalent circuit
20 (24)	PWM	PWM oscillator frequency setting Insert a capacitor between this pin and ground.	
21 (25)	FV	Hall sensor signal one-shot multi-pulse output	
22 (26)	RC	Hall sensor signal one-shot multi-pulse amplitude setting Insert a resistor between this pin and the V5 pin, and a capacitor between this pin and ground.	
23 (27)	HP	Hall sensor signal three-phase synthesized output (Open collector output)	

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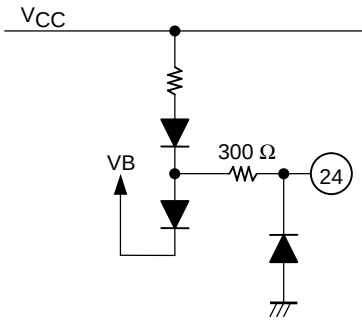
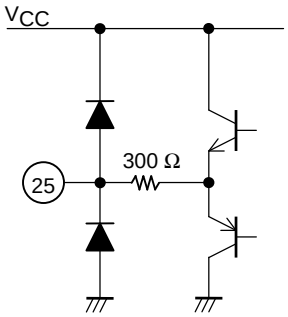
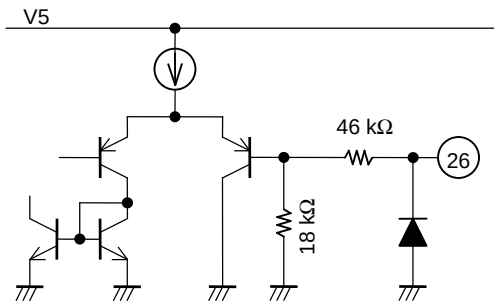
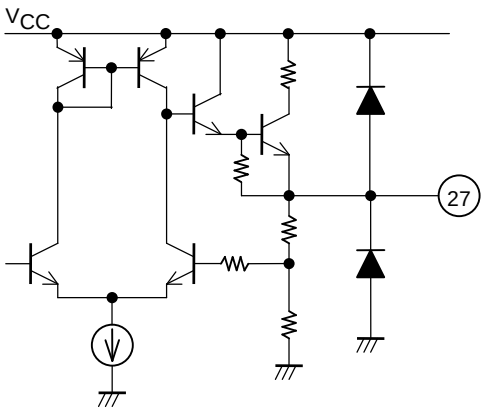
Pin No.	Pin Name	Pin description	Equivalent circuit
24 (28)	CP2	Charge pump capacitor connections Connect a capacitor between pins CP1 and CP2.	
25 (29)	CP1		
26 (30)	LVS	Undervoltage protection voltage detection. To detect a voltage of 5 V or over, connect a zener diode in series to set the detection voltage.	
27 (32)	V5	Stabilized power supply output (5 V output) Insert a capacitor (about 0.1 µF) between this pin and ground for power supply stabilization.	

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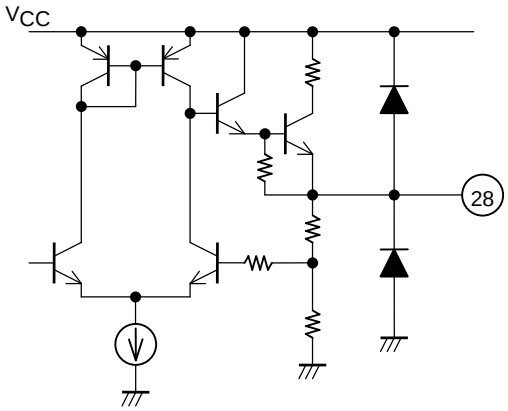
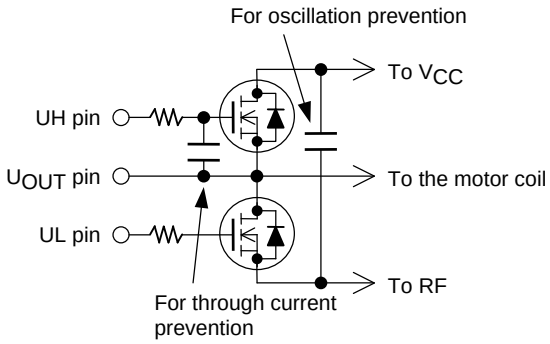
Pin No.	Pin Name	Pin description	Equivalent circuit
28 (33)	V12	Stabilized power supply output (12 V output) Insert a capacitor (about 0.1 µF) between this pin and ground for power supply stabilization.	
29 (35)	V_{CC}	Power supply Insert a capacitor between this pin and ground for power supply stabilization.	
30 (1)	VB	Charge pump output (UH, VH, and WH output block power supply) Insert a capacitor between this pin and V_{CC}.	
	(FRAME)	The FRAME pin is connected to the IC lower surface metal frame internally. Both should be left electrically open during operation.	
(6) (15) (19) (31) (34) (36)	(NC)	These pins are not connected to the IC internally in the package, and thus may be used for wiring connections.	

LB11690/LB11690H Function Description

1. Output Drive Circuit

This IC was designed assuming that n-channel FETs would be used in both the low and high side output circuits. Direct PWM drive was adopted as the drive method to minimize power loss in the outputs. The output transistors are always saturated when on, and the motor drive power is adjusted by changing the output on duty. The output PWM switching is performed on the low side output circuits connected to the UL, VL, and WL pins. Since the reverse recovery time for the diodes built into the high side (the non-PWM side) output FETs can become a problem, the devices used must be selected carefully. (If diodes with a short reverse recovery time are not used, through currents may flow at the instant the PWM side transistors turn on.)

Capacitors (about 0.1 µF) must be inserted close to the output FETs for each of the three phases to prevent high-frequency oscillator due to the PCB pattern.



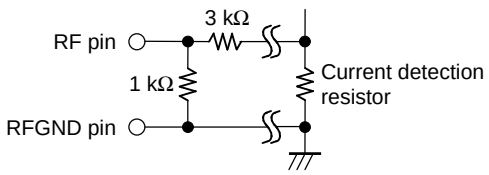
If the FET switching speed is too fast and leads to problems, adjust the speed by inserting a series resistor in the gate line. If the low side (PWM side) FET on speed is too fast, through currents may flow. However if too large a resistance is inserted in the gate line, the gate waveform may become less sharp. When the PWM on duty is low, the gate voltage may be insufficient. This can lead to excessive heating or even destruction of the low side FET. Even if a resistor is not inserted, a similar phenomenon may occur if the FET gate capacitance is relatively large. In such cases, the lowest duty used must be limited, taking the ASO of the switching device used into consideration.

Depending on the FET devices used, through currents may flow when the PWN on duty is low. One workaround for this problem is to insert capacitors between the gate and source of the high side FETs. However, if the capacitor values are too high, switching may become too slow, resulting in excessive heating in the high side FETs.

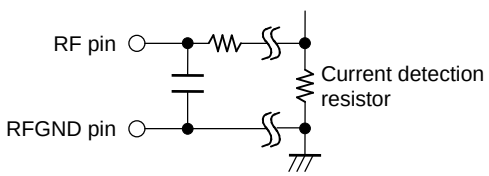
2. Current Limiter Circuit

The current limiter circuit limits the (peak) current at a current determined by the equation I = VRF/Rf (where VRF is 0.1 V (typical) and Rf is the value of the current detection resistor). The current limiter operates by reducing the output on duty, thus reducing the output current. This circuit can be operated at a precise current limit value by connecting both ends of the current detection resistor as close as possible to the RF and RFGND pins.

If a current detection resistor with an extremely small value is used, the PCB pattern must be designed so that the wiring resistance components for each phase are as close to identical as possible. If there are differences in the wiring resistance components between the phases, the current limit value will change each time the phase changes. This can lead to motor vibration and motor noise.



While the reference voltage is set to 0.1 V to minimize power loss in the current detection resistor, it may be desirable to use a larger current detection resistor value in some applications. In such cases, a resistor divided voltage must be input to the RF pin. If the resistor ratio shown in the figure is used, a current detection resistor about 4 times larger can be used.



The current limiter circuit includes a built-in filter circuit so that the current limiter circuit does not operate incorrectly due to detecting the output diode reverse recovery current due to PWM operation. In most applications, the built-in filter circuit will function without problem. If problems due occur (if the diode reverse recovery current flows for more than 1 µs), add an external filter circuit such as a low-pass RC filter. However, be careful not to insert excessive delay, as that will delay detection by the current limiter circuit.

3. PWM Oscillator Circuit

The PWM frequency is determined by the capacitor C (rated in F) connected to the PWM pin.

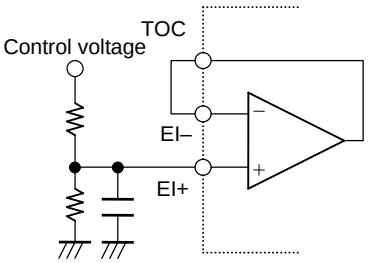
$$f_{PWM} \approx 1/(93000 \times C)$$

When a 270 pF capacitor is used, the frequency will be about 39 kHz. If the PWM frequency is too low, the motor will generate audible noise at the switching frequency, and if it is too high, the power loss will increase. A frequency in the range 20 to 50 kHz is desirable. Connect the ground side of this capacitor to a point as close as possible to the IC ground pin to minimize the influence of output noise.

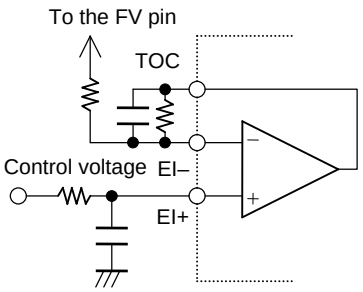
4. Control Methods

The output duty is determined by comparing the PWM oscillator waveform to the TOC pin voltage. When the TOC pin voltage is about 1.2 V or lower, the duty will be 0%, and when that voltage is 3.0 V or higher, the duty will be 100%.

Normally, the integrating amplifier is used as a full feedback amplifier (with the EI^- pin and the TOC pin connected directly), and the control voltage is input to the EI^+ pin. (Here, the output duty increases as the EI^+ voltage increases.) When the EI^+ pin is set to the reset operating state by the RES pin, the EI pin voltage is lowered to a level close to the ground level by an IC internal transistor. (This is to discharge the capacitor.) Therefore, do not connect a low-impedance power supply directly to this pin, but rather input the voltage through a resistor. Also, a pull-down resistor must be inserted between the EI^+ pin and ground so that the motor does not operate when the control voltage is in the open state. If there is noise on the control voltage or if it is desirable to suppress rapid fluctuations in the control voltage, a noise rejection capacitor must be inserted between the EI^+ pin and ground. The operating voltage range can be expanded by inputting the control voltage to the EI^+ pin through a resistor voltage divider as shown in the figure.



A speed control circuit using the FV pin can be implemented as shown in the figure to control the motor so that a constant speed is maintained to a certain degree despite variations in the load. A resistor of 25 kΩ or larger must be used between the FV and EI^+ pin. The feedback capacitor must be selected so that the TOC pin voltage is adequately stable at low speeds.



5. Charge Pump Circuit

The charge pump steps up the supply voltage to generate the high side FET gate voltage. The capacitor CP connected between the CP1 and CP2 pins is used for step up, and charge is stored on the capacitor CB connected between the VB and V_{CC} pins. The capacitances of CP and CB must have the following relationship.

$$CB \geq CP \times 4$$

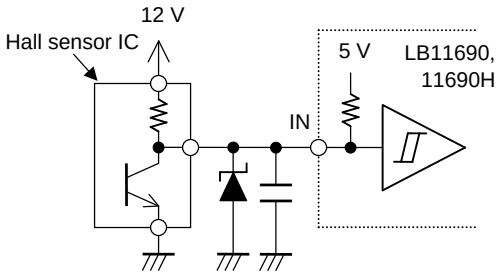
The CP capacitor is charged and discharged based on the PWM frequency. While increasing the capacitance of the capacitor C increases current capacity of the VB power supply, if the capacitance is too large, the charge and discharge operation may be inadequate. Note that the larger the capacitance of the capacitor VB, the more stable the VB voltage will be. However, if that capacitance is too large, the time before the VB voltage is generated when power is first applied will increase. While testing and evaluation is required to set the values of the capacitors CP and CB, use the following table as a reference for the initial values.

When the V_{CC} supply voltage is under 20 V, the VB power supply current capacity falls rapidly causing the VB voltage to fall. Care is required in application design to assure that this does not become a problem.

V_{CC} voltage	24 V	36 V
CP	0.1 µF	6800 pF
CB	1 µF	0.47 µF

6. Hall Sensor Input Signals

The outputs of the Hall sensor IC are connected to this IC's Hall sensor inputs. Since the IC includes internal pull-up resistors (about 10 kΩ) to the 5 V regulator, normally, there is no need for external pull-up resistors. If a Hall sensor IC with built-in pull-up resistors is used, no problems will occur as long as the Hall sensor IC uses a 5 V power supply. However, pull-down resistors and voltage clamping zener diodes must be added to assure that voltages over 5 V are not applied to this IC if the Hall sensor IC uses a 12 V power supply.



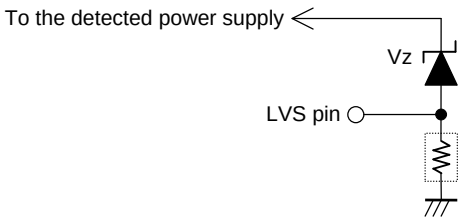
The inputs are comparator inputs with a hysteresis of about 0.9 V. If noise becomes a problem, noise rejection capacitors must be inserted between the inputs and ground.

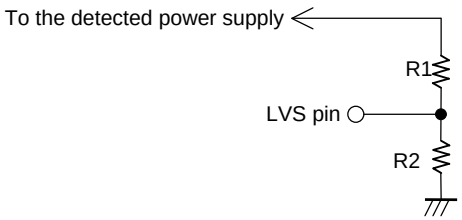
If all three of the Hall input signals go to the same input state, all the outputs, both the high side and low side, will go to the off state.

7. Undervoltage Protection Circuit

The undervoltage protection circuit detects the voltage applied to the LVS pin and if that voltage falls under the operating voltage (3.8 V typical), the drive outputs are all set to the off state. This circuit has hysteresis to prevent the circuit from repeatedly turning the outputs on and off when the supply voltage is close to the protection operating voltage. Therefore, the output will not recover unless the supply voltage rises to about 0.5 V above the circuit's operating voltage. Also, the RES pin voltage goes to the low level in the protection operating state.

The protection operating voltage is set to be the detection level for a 5 V system. The detection level can be increased by inserting a zener diode in the LVS pin to level shift the detection level. (The detection voltage will then be the zener voltage (Vz) plus 3.8 V (typical).) The LVS pin sink current during detection is about 62 µA. If it is necessary to stabilize the zener diode voltage increase and to minimize variations in the zener voltage, insert a resistor between the LVS pin and ground to increase the zener current. It is also possible to increase the detection voltage without using a zener diode by using a resistor voltage divider.





If the circuit in the figure is used, the detection and release voltages will be as follows.

Detection voltage ≈ ((3.8 ÷ R2) + 62 µA) × (R1 + R2)

Release voltage ≈ ((4.3 ÷ R2) + 70 µA) × (R1 + R2)

If R1 is 13 kΩ and R2 is 2.2 kΩ, the detection voltage will be about 27 V and the release voltage will be about 31 V. Note that errors in the detection voltage due to temperature and sample-to-sample variations increase as the value of the resistor R2 increases.

If this protection circuit is not used, the LVS pin must not be left open (the outputs are turned off when this pin is open). Rather, a voltage at a level at which the circuit does not operate must be applied.

8. RES Circuit

When power is first applied, the application must apply an initial reset to the RES pin to assure stable operation. The initial reset performs the following operations.

- All the drive outputs are turned off.
- The EI^+ pin voltage is forced to the low level.
- The FV pin voltage is forced to the low level.

Normally, a resistor and a capacitor are inserted between the RES pin and the V5 pin and the RES pin and ground, respectively, to set the reset time. A resistor with a value of 2.7 kΩ or higher must be used. The time constant must be set to a value such that R × C ≥ 1 ms (if a 10 kΩ resistor is used, the capacitor must be 0.1 µF or larger). However, in cases where it is necessary to completely discharge the capacitors on the EI^+ and FV pins, the reset time must be set to cover those discharge times. It is also desirable to set the reset time to be longer than the time required to stabilize the VB voltage after power is first applied.

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The IC remains in the reset state as the RES pin voltage goes from 0 V to about 1.5 V. Since the reset circuit has a hysteresis of about 0.23 V, the IC will not return to the reset state unless the RES pin voltage falls to under 1.27 V.
In addition to the initial reset, the RES pin can also be used to apply a reset when the control voltage is low as shown in figure 1. This circuit sets all the drive outputs to the off state when the control voltage reaches about 0.67 V (1.27 V - V_{BE}). Here, the reset release voltage is about 0.9 V (0.67 V + 0.23 V).
In the state when 0% duty (1.2 V or lower) is set up with just the control voltage, the circuit will function as a brake if the motor is operated in the reverse direction. Thus the circuit shown here can be useful if braking is not required during reverse rotation. If the control voltage cannot be lowered below 1 V, a circuit such as that shown in figure 3 can be used.
Applications that use a thermistor to detect the temperature and prevent thermal destruction of the FETs can also be considered. The FETs can be protected by adjusting the value of the external resistor connected as shown in figure 2.
Figure 4 shows how to combine this application circuit with the application circuit shown in figure 3.

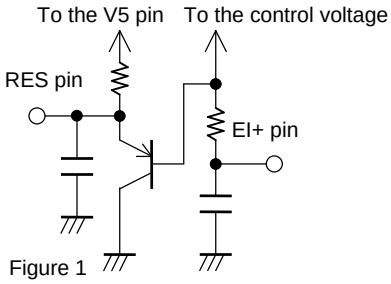


Figure 1

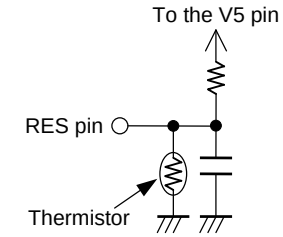


Figure 2

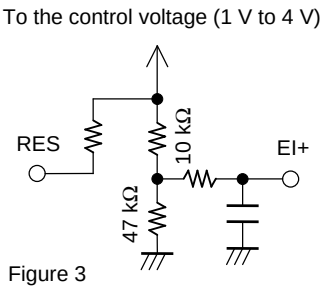


Figure 3

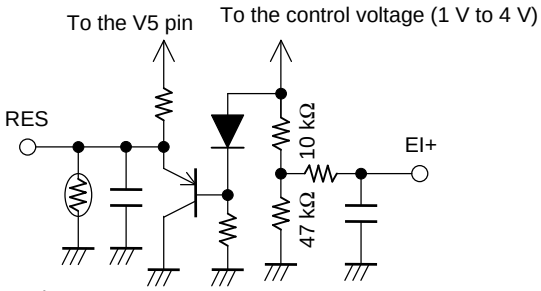


Figure 4

9. RC and FV Circuits

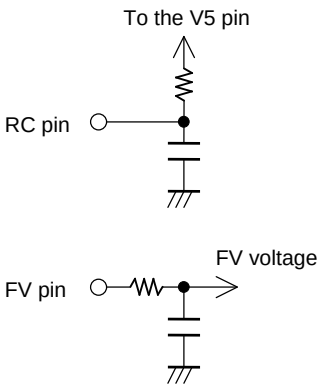
The RC pin sets the pulse width (the high-level period) of the signal generated at the FV pin at each edge (both rising and falling edges) of the HP signal (the three-phase synthesized Hall signal). The pulse width is set by connecting a resistor between the RC pin and the V5 pin and a capacitor between the RC pin and ground. The pulse width, TRC, can be calculated with the following formula.

$$TRC\ (seconds) \approx 1.1 \times R \times C$$

The FV pin is normally smoothed with an RC circuit such as that shown in the figure. A resistor with a value of 25 kΩ or higher must be used. Choose a capacitance such that the FV voltage is smoothed adequately at low motor speeds. Normally, TRS is set to meet the following condition when the HP signal frequency at the highest motor speed is fHP (Hz).

$$TRC\ (seconds) \leq 1 \div (2 \times f_{HP})$$

Here, the FV voltage will vary from 0 to about 5 V according to the motor speed. The FV voltage can be used for speed feedback or speedometer display by using an analog meter or level meter IC.
If the FV output is not used, the RC pin must be connected to ground and the FV pin must be left open.



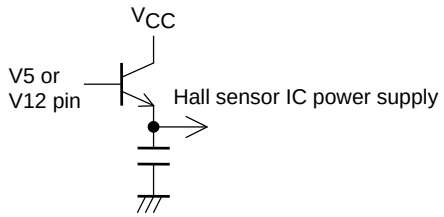
10. Power Supply Stabilization

Since this IC uses a switching based drive technique, it can easily cause voltage fluctuations in the power supply lines. This means that capacitors fully adequate to stabilize the supply voltage must be inserted between the V_{CC} pin and ground.
If diodes are inserted in the power supply lines to prevent damage when the power supply is connected with the polarity reversed, voltage fluctuations in the power supply lines can occur even more easily. In such applications, even larger capacitors are required.

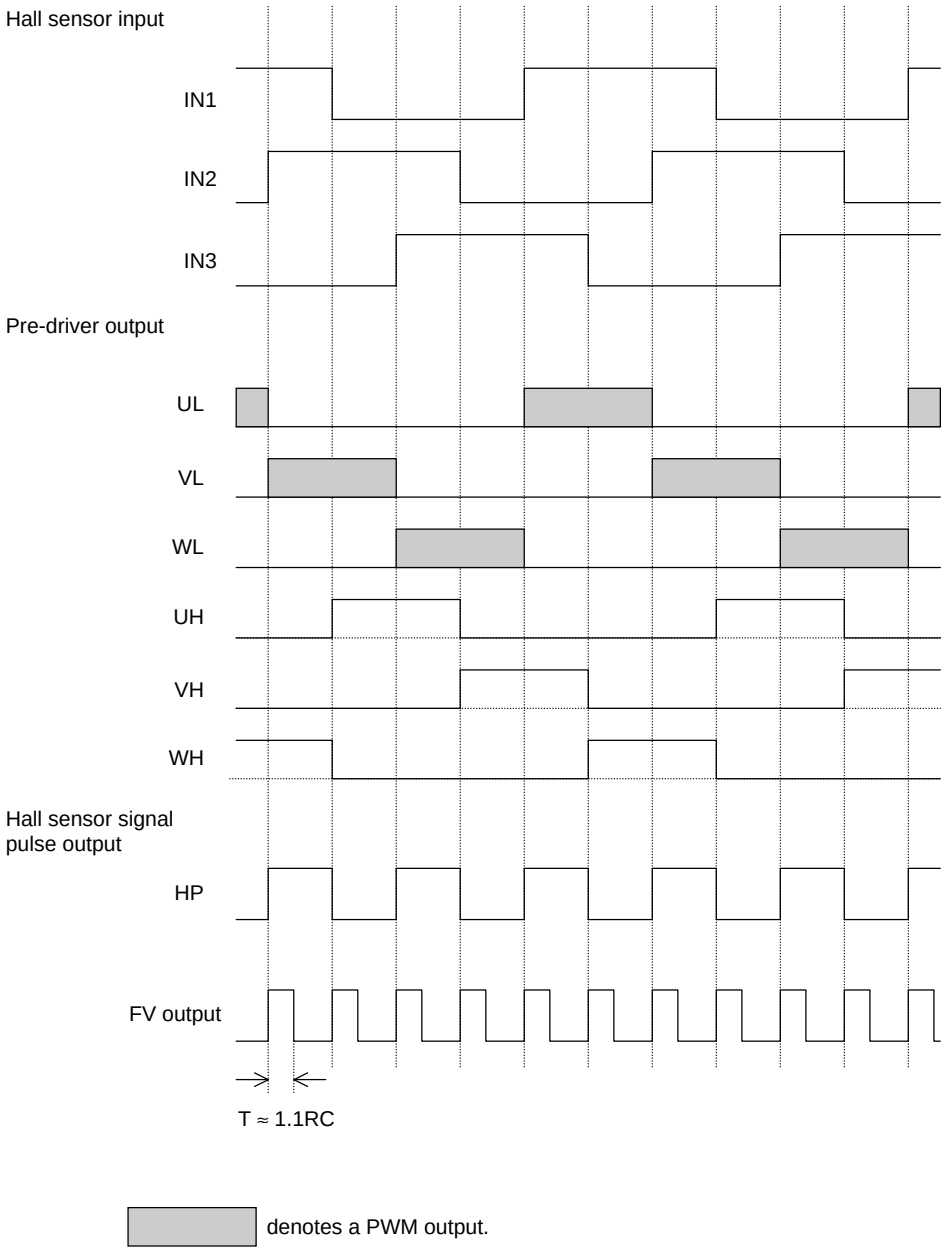
11. Regulator Output Voltage Stabilization

Capacitors of 0.1 µF or larger must be inserted between the V5 (5 V control circuit power supply) and V12 (12 V low side drive output circuit power supply) pins and ground. The ground sides of these capacitors must be connected to points as close as possible to an IC ground pin.

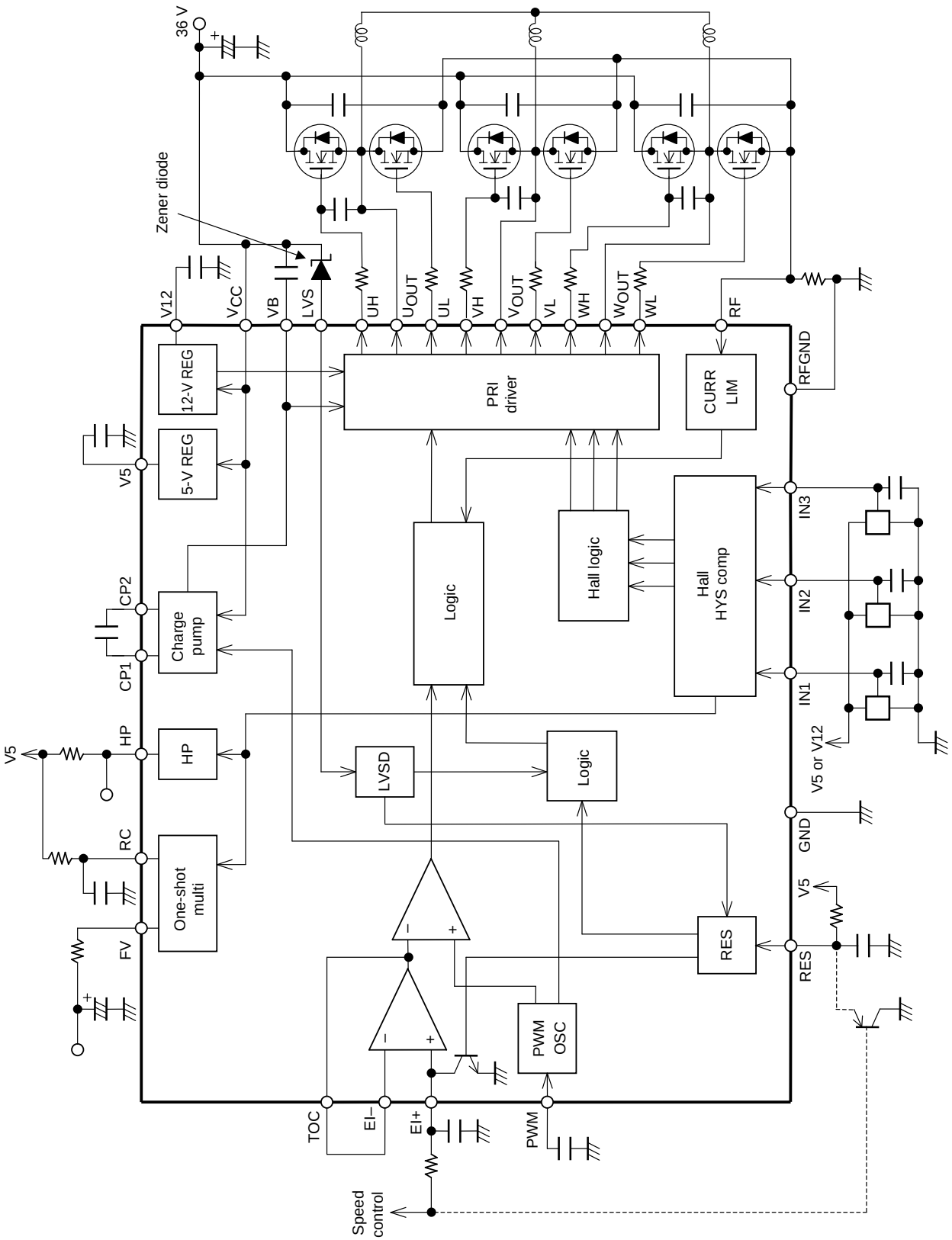
While each of these outputs can provide currents of up to 30 mA to external circuits, care is required since this can increase IC heating. If this IC is used as the power supply for the Hall sensor IC and other circuits and heating becomes a problem, use an external transistor as shown in the figure so that this heating load is born by that transistor.



Hall Sensor Input to Drive Output Timings



Sample Application Circuit



Sample Application Circuit (Closed Loop Speed Control)