

TISP61060D, TISP61060P DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

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SEPTEMBER 1995 - REVISED SEPTEMBER 1997

PROGRAMMABLE SLIC OVERVOLTAGE PROTECTION

- **Dual Voltage-Programmable Protectors**
 - Third Generation Design using Vertical Power Technology
 - Wide -5 V to -85 V Programming Range
 - High 150 mA min. Holding Current
- **Reduced V_{BAT} Supply Current**
 - Triggering Current is Typically 50x Lower
 - Negative Value Power Induction Current Removes Need for Extra Protection Diode
- **Rated for LSSGR & FCC Surges**

STANDARD	WAVE SHAPE	I_{TSP} A
LSSGR	10/1000 μ s	30
FCC Part 68	10/160 μ s	45
LSSGR	2/10 μ s	50

- **Surface Mount and Through-Hole Options**
 - TISP61060P for Plastic DIP
 - TISP61060D for Small-Outline
 - TISP61060DR for Taped and Reeled Small-Outline
- **Functional Replacements for**

PART NUMBERS	FUNCTIONAL REPLACEMENT
TCM1030P, TCM1060P, LB1201AB	TISP61060P
TCM1030D, TCM1060D, LB1201AS	TISP61060D
TCM1030DR, TCM1060DR	TISP61060DR

description

The TISP61060 is a dual forward-conducting buffered p-gate overvoltage protector. It is designed to protect monolithic SLICs (Subscriber Line Interface Circuits), against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISP61060 limits voltages that exceed the SLIC supply rail voltage.

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -10 V to -70 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. As the protection voltage will track the negative supply voltage, the overvoltage stress on the SLIC is minimised. (see Applications Information).

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition. As the current subsides the high holding current of the crowbar prevents d.c. latchup.

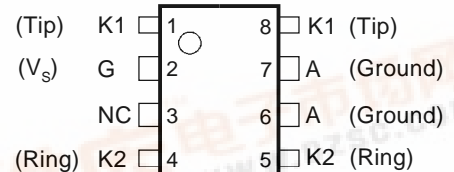
'61060D PACKAGE
(TOP VIEW)



MD6XAO

NC - No internal connection
Terminal typical application names shown in parenthesis

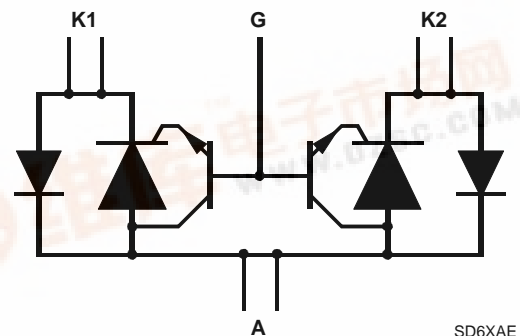
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(TOP VIEW)



MD6XAP

NC - No internal connection
Terminal typical application names shown in parenthesis

device symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, V_{GG} , applied to the G terminal.

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These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction.

absolute maximum ratings

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, $I_G = 0$, $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$	V_{DRM}	-100	V
Repetitive peak gate-cathode voltage, $V_{KA} = 0$, $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$	V_{GKRM}	-85	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)	I_{TSP}	30 45 50	A
10/1000 μs			
10/160 μs			
2/10 μs			
Non-repetitive peak on-state current (see Notes 1 and 2)	I_{TSM}	6 1	Arms
60 Hz sine-wave, 25 ms			
60 Hz sine-wave, 2 s			
Continuous on-state current (see Note 2)	I_{TM}	0.3	A
Continuous forward current (see Note 2)	I_{FM}	0.3	A
Operating free-air temperature range	T_A	-40 to +85	$^\circ\text{C}$
Storage temperature range	T_{stg}	-40 to +150	$^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 s	T_L	260	$^\circ\text{C}$

NOTES: 1. Initially the protector must be in thermal equilibrium with $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$. The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above 85°C , derate linearly to zero at 150°C lead temperature.

recommended operating conditions

	MIN	TYP	MAX	UNIT
C_G Gate decoupling capacitor		100		nF

electrical characteristics, $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_D Off-state current	$V_D = -85\text{ V}$, $V_{GK} = 0\text{ V}$			5	μA
				50	μA
$V_{(BO)}$ Breakover voltage	$dv/dt = -250\text{ V/ms}$, Source Resistance = $300\ \Omega$, $V_{GG} = -50\text{ V}$			-53	V
	$dv/dt = -250\text{ V/ms}$, Source Resistance = $300\ \Omega$, $V_{GG} = -65\text{ V}$			-68	
	$I_T = 12.5\text{ A}$, 10/1000 μs , Source Resistance = $80\ \Omega$, $V_{GG} = -50\text{ V}$			-55	
I_S Switching current	$dv/dt = -250\text{ V/ms}$, Source Resistance = $300\ \Omega$, $V_{GG} = -50\text{ V}$	-100			mA
V_T On-state voltage	$I_T = 1\text{ A}$			3	V
	$I_T = 10\text{ A}$			4	
	$I_T = 16\text{ A}$			5	
	$I_T = 30\text{ A}$			7	
V_F Forward voltage	$I_F = 1\text{ A}$			2	V
	$I_F = 10\text{ A}$			4	
	$I_F = 16\text{ A}$			5	
	$I_F = 30\text{ A}$			5	
I_H Holding current	$I_T = -1\text{ A}$, $di/dt = +1\text{ A/ms}$, $V_{GG} = -50\text{ V}$	-150			mA

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electrical characteristics, $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GAS} Gate reverse current	$V_{GG} = -85\text{ V}$, K and A terminals connected	$T_J = 25^{\circ}\text{C}$		5	μA
		$T_J = 85^{\circ}\text{C}$		50	μA
I_{GT} Gate trigger current	$I_T = -1\text{ A}$, $t_{p(g)} \geq 20\text{ }\mu\text{s}$, $V_{GG} = -50\text{ V}$			15	mA
dv/dt Critical rate of rise of off-state voltage	$V_{GG} = -50\text{ V}$, (see Note 3)	-1000			V/ μs
C_O Anode-cathode off-state capacitance	$f = 1\text{ MHz}$, $V_d = 0.1\text{ V}$, $I_G = 0$, (see Note 4)	$V_D = 0\text{ V}$		85	pF
		$V_D = -50\text{ V}$		10	pF

NOTES: 3. Linear rate of rise, maximum voltage limited to 80% V_{GG} .

4. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

thermal characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction to free air thermal resistance	$P_{tot} = 0.8\text{ W}$, $T_A = 25^{\circ}\text{C}$ 5 cm ² , FR4 PCB	D Package		170	$^{\circ}\text{C/W}$
		P Package		125	

PARAMETER MEASUREMENT INFORMATION

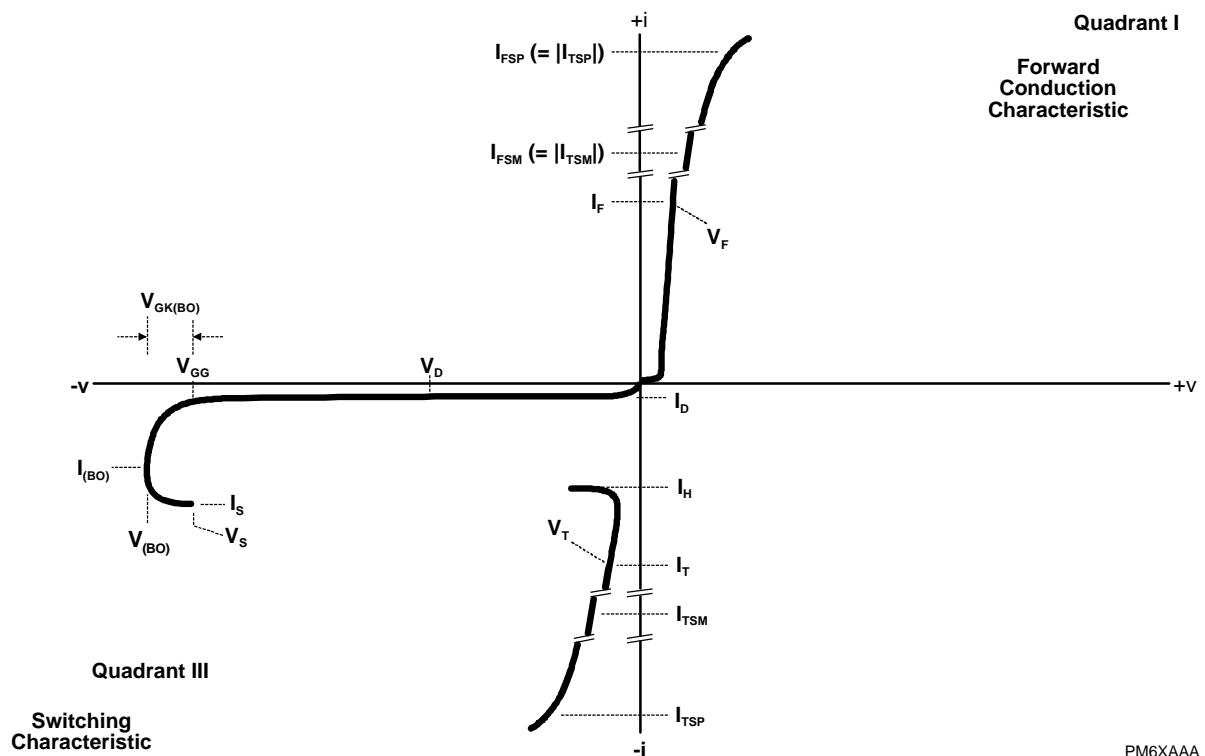


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC

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DEVICE PARAMETERS

general

Thyristor based overvoltage protectors, for telecommunications equipment, became popular in the late 1970s. These were fixed voltage breakover triggered devices, likened to solid state gas discharge tubes. As these were new forms of thyristor, the existing thyristor terminology did not cover their special characteristics. This resulted in the invention of new terms based on the application usage and device characteristic. Initially, there was a wide diversity of terms to describe the same thing, but today the number of terms have reduced and stabilised.

Programmable, (gated), overvoltage protectors are relatively new and require additional parameters to specify their operation. Similarly to the fixed voltage protectors, the introduction of these devices has resulted in a wide diversity of terms to describe the same thing. To help promote an understanding of the terms and their alternatives, this section has a list of alternative terms and the parameter definitions used for this data sheet. In general, the Texas Instruments approach is to use terms related to the device internal structure, rather than its application usage as a single device may have many applications each using a different terminology for circuit connection.

alternative symbol cross-reference guide

This guide is intended to help the translation of alternative symbols to those used in this data sheet. As in some cases the alternative symbols have no substance in international standards and are not fully defined by the originators, users must confirm symbol equivalence. No liability will be assumed from the use of this guide.

CROSS-REFERENCE FOR TISP61060 AND TCM1030/60

TISP61060 PARAMETER	DATA SHEET SYMBOL	ALTERNATIVE SYMBOL	ALTERNATIVE PARAMETER
RATINGS & CHARACTERISTICS		TCM1060, TCM1030	
Non-repetitive peak on-state pulse current	I_{TSP}	-	Non-repetitive peak surge current
Non-repetitive peak on-state current	I_{TSM}	-	Non-repetitive peak surge current, 10 ms
Non-repetitive peak on-state current	I_{TSM}	-	Continuous 60-Hz sinewave, 2 s
Forward voltage	V_F	V_{CF}	Forward clamping voltage
Forward current	I_F	I_{FM}	Peak forward current
On-state voltage	V_T	V_C	Reverse clamping voltage
On-state current	I_T	I_{TM}	Peak reverse current
Switching current	I_S	I_{trip}	Trip current
Breakover voltage	$V_{(BO)}$	V_{trip}	Trip voltage
Gate reverse current (with A and K terminals connected)	I_{GAS}	I_D	Stand-by current, TIP & RING at GND
Off-state current	I_D	I_D	Stand-by current, TIP & RING at V_S
Off-state voltage	V_D	V_S	Supply voltage
Gate-cathode breakover voltage	$V_{GK(BO)}$	V_{OS}	Transient overshoot voltage
Gate voltage, (V_{GG} is gate supply voltage referenced to the A terminal)	V_G	V_S	Supply voltage
Off-state capacitance	C_O	C_{off}	Off-state capacitance
TERMINALS		TCM1060, TCM1030	
Cathode 1	K1	Tip	Tip
Cathode 2	K2	Ring	Ring
Anode	A	GND	Ground
Gate	G	V_S	Supply voltage

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CROSS-REFERENCE FOR TISP61060 AND LB1201AB

TISP61060 PARAMETER	DATA SHEET SYMBOL	ALTERNATIVE SYMBOL	ALTERNATIVE PARAMETER
RATINGS & CHARACTERISTICS		LB1201AB	
Non-repetitive peak on-state pulse current	I_{TSP}	I_P	Pulse current
Non-repetitive peak on-state current	I_{TSM}	I_P	RMS pulse current, 60 Hz
On-state voltage	V_T	V_{ON}	On-state voltage
Switching current	I_S	I_t	Trip current
Breakover voltage	$V_{(BO)}$	V_T	Trip voltage
Maximum continuous on-state current	I_{TM}	I_C	On-state current
Maximum continuous forward current	I_{FM}	I_C	On-state current
Gate voltage, (V_{GG} is gate supply voltage referenced to the A terminal)	V_G	V_S	Supply voltage
Off-state capacitance	C_O	C_{OFF}	Off-state capacitance
TERMINALS		LB1201AB	
Cathode 1	K1	Tip	Tip
Cathode 2	K2	Ring	Ring
Anode	A	GND	Ground
Gate	G	V_S	Supply voltage

APPLICATIONS INFORMATION

electrical characteristics

The electrical characteristics of a thyristor overvoltage protector are strongly dependent on junction temperature, T_J . Hence a characteristic value will depend on the junction temperature at the instant of measurement. The values given in this data sheet were measured on commercial testers, which generally minimise the temperature rise caused by testing.

gated protector evolution and characteristics

This section covers three topics. Firstly, it is explained why gated protectors are needed. Second, the performance of the original IC (integrated circuit) based version is described. Third, the performance improvements given by the TISP61060 are detailed.

purpose of gated protectors

Fixed voltage thyristor overvoltage protectors have been used since the early 1980s to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. As the SLIC was usually powered from a fixed voltage negative supply rail, the limiting voltage of the protector could also be a fixed value. The TISP1072F3 is a typical example of a fixed voltage SLIC protector.

SLICs have become more sophisticated. To minimise power consumption, some designs automatically adjust the supply voltage, V_{BAT} , to a value that is just sufficient to drive the required line current. For short lines the supply voltage would be set low, but for long lines, a higher supply voltage would be generated to drive sufficient line current. The optimum protection for this type of SLIC would be given by a protection voltage which tracks the SLIC supply voltage. This can be achieved by connecting the protection thyristor gate to the SLIC supply, Figure 2. This gated (programmable) protection arrangement minimises the voltage stress on the SLIC, no matter what value of supply voltage.

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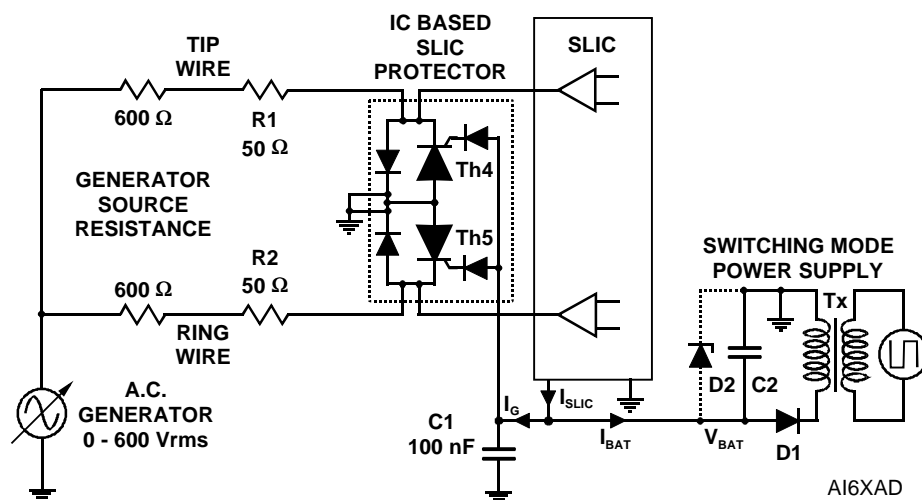


Figure 2. SIMPLIFIED IC BASED SLIC PROTECTOR CIRCUIT

ic based protectors

In 1986, an IC based gated protector was proposed (A 90 V Switching Regulator and Lightning Protection Chip Set, Robert K. Chen, Thomas H. Lerch, Johnathan S. Radovsky, D. Alan Spires, IEEE Solid-State Circuits Conference, February 20, 1986, pp 178/9 and pp 340/1). Commercially, this resulted in the AT&T Microelectronics LB1201AB device and the higher current Texas Instruments Inc. TCM1060 device

This implementation consisted of four diodes and two high holding current thyristors. Positive overvoltages on the line wires are clipped to ground by forward conduction of the wire to ground diodes. Negative overvoltages are initially clipped close to the SLIC negative supply rail, V_{BAT} , by conduction of the thyristor cathode-gate and gate series diode. This means that the protection voltage level for slow wave forms will be about 1.5 V lower than the SLIC supply voltage. If sufficient current is available from the overvoltage, then the thyristor will switch into a low voltage on-state condition. When the thyristor crowbars, the two series gate diodes prevent the SLIC supply from being shorted to ground via the thyristor gate. As the overvoltage subsides the high holding current of the crowbar prevents d.c. latchup (see Figure 1).

impulse protection performance

The impulse protection voltage will be the sum of the gate supply (V_{BAT}) and the impulse peak gate-cathode voltage ($V_{GK(BO)}$). Capacitor C1 provides the pulse of gate current that occurs during fast rising impulses. The protection voltage will be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse (e.g. 2/10), the gate current (I_G) is the same as the cathode current (I_K). Rates of 70 A/ μ s can cause inductive voltages of 0.7 V in 2.5 cm of printed wiring track. To minimise this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimised. Inductive voltages in the protector cathode wiring can increase the protection voltage. These voltages can be minimised by routing the SLIC connection through the protector as shown in Figure 2.

a.c. protection performance

Figure 2 shows a typical a.c. power cross test circuit. A variable voltage a.c. source is applied to the line card via 600 Ω series resistors. On the line card there are further series resistors R1 and R2. These resistors provide over-current protection by fusing or going high resistance under high current a.c. conditions.

Figure 3 shows the gate and cathode a.c. power line cross voltage and current wave forms of the IC based protector. Positive voltages are clipped at about +1 V by diode conduction. Negative voltages are clipped to about -52 V as the SLIC supply voltage was -50 V. Sufficient current (200 mA) was available to cause the

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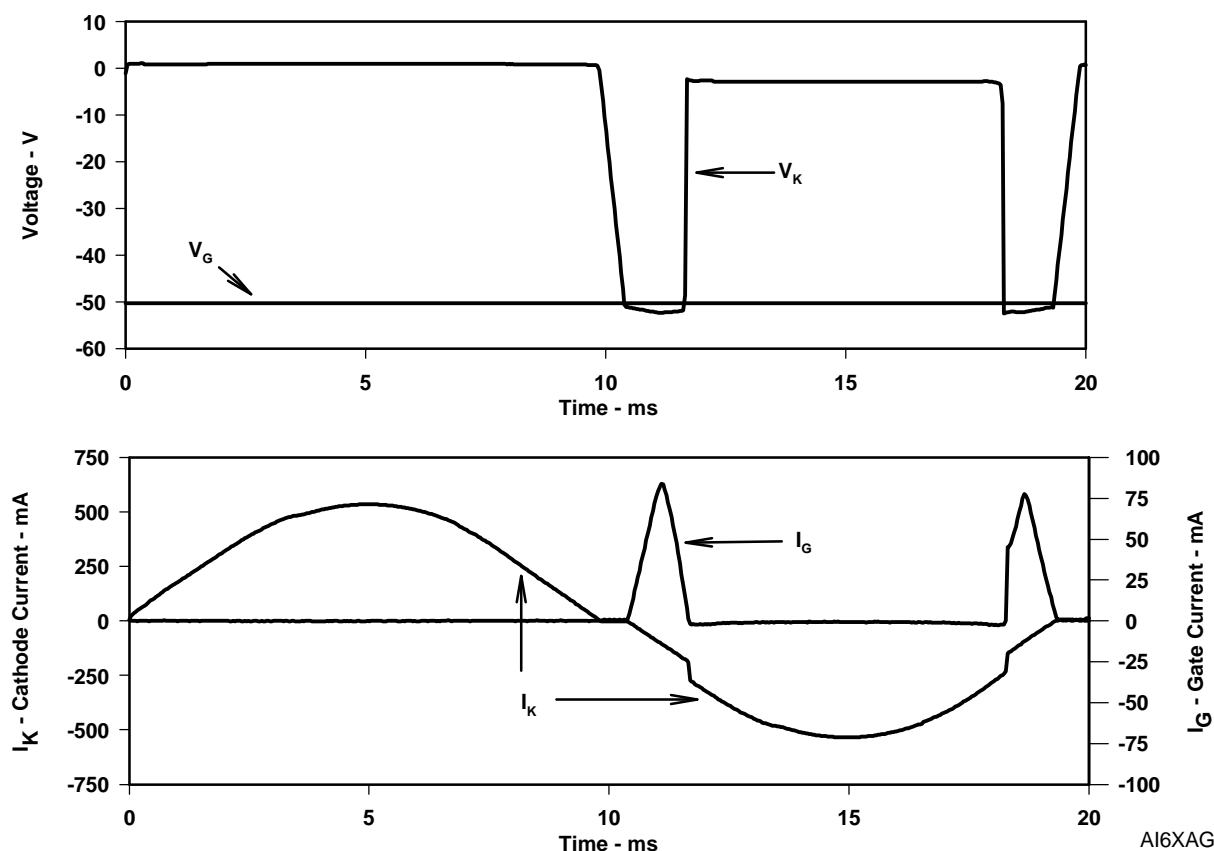


Figure 3. IC PROTECTOR POWER CROSS WAVE FORMS

thyristor to switch into the low-voltage on-state condition. At the end of the negative half cycle, the thyristor switches off when the current falls below the holding current value (300 mA). Switch-off and re-clipping at -52 V causes a second pulse of gate current. The wire current drawn by the protector is quasi-sinusoidal

During the positive a.c. voltage period (diode clipping) there is no gate current. During the negative a.c. voltage period there are two triangular pulses of gate current, which peak at about 80 mA. This is current which flows into the gate terminal as indicated by the I_G current arrow in Figure 2. This direction of current charges the V_{BAT} supply. This would not be a problem if the V_{BAT} supply was a rechargeable battery. However, often the supply is generated from a switching mode power supply or the SLIC supply feed has a series diode which blocks reverse (charging) current flow to the battery. In these cases the supply can only sink current in the direction shown by the I_{BAT} arrow in Figure 2. Unless the SLIC current, I_{SLIC} , is equal or greater than I_G the value of V_{BAT} will increase, possibly to a level which causes destruction of the SLIC.

The maximum average value of I_G occurs when the thyristor only clips the voltage and the peak cathode current is just beginning to approach the switching (I_S) value, see Figure 4. The average current is maximised under high source impedance conditions (e.g. 600 Ω). In the case of the LB1201AB, it is recommended that the supply should be able to absorb 700 mA of "wrong way" current. If the supply cannot absorb the current then a shunt breakdown diode is recommended to provide a path for the gate current to ground (D2 in Figure 2). High power diodes are expensive, so diode D2 is usually low power, purposely selected to fail under this a.c. condition and protect the SLIC.

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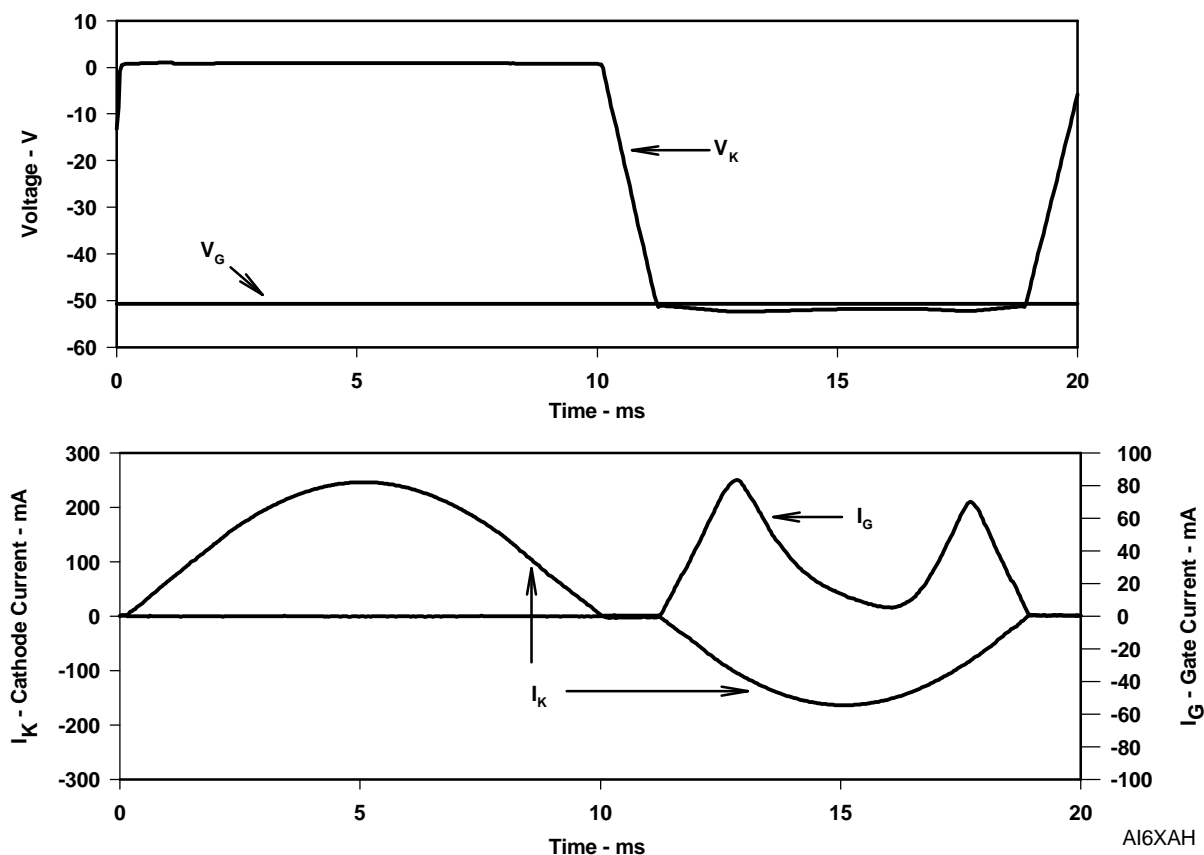


Figure 4. IC PROTECTOR HIGH IMPEDANCE POWER CROSS CLIPPING WAVE FORMS

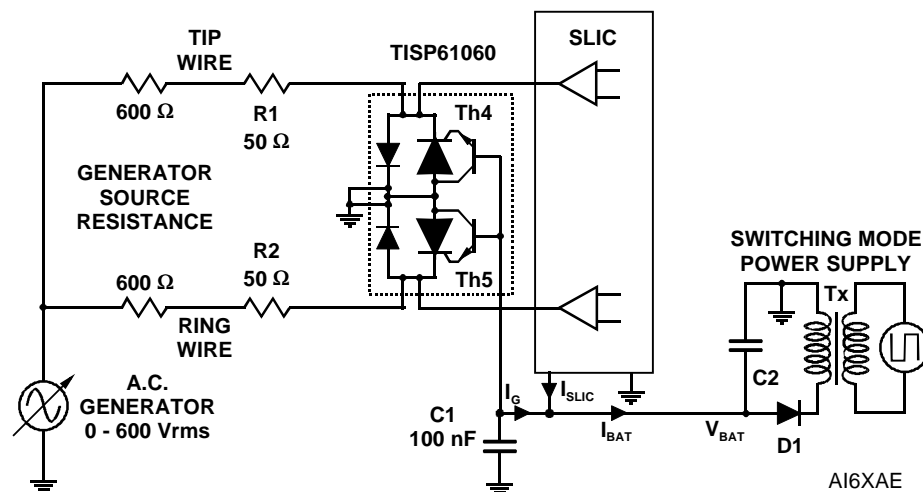


Figure 5. TISP61060 BUFFERED GATE PROTECTOR

TISP61060 buffered gate protector

The TISP61060 improves on the original IC based design in three ways, Figure 5. Firstly, the thin lateral IC structure has been changed to a vertical power device structure for increased area efficiency and greater

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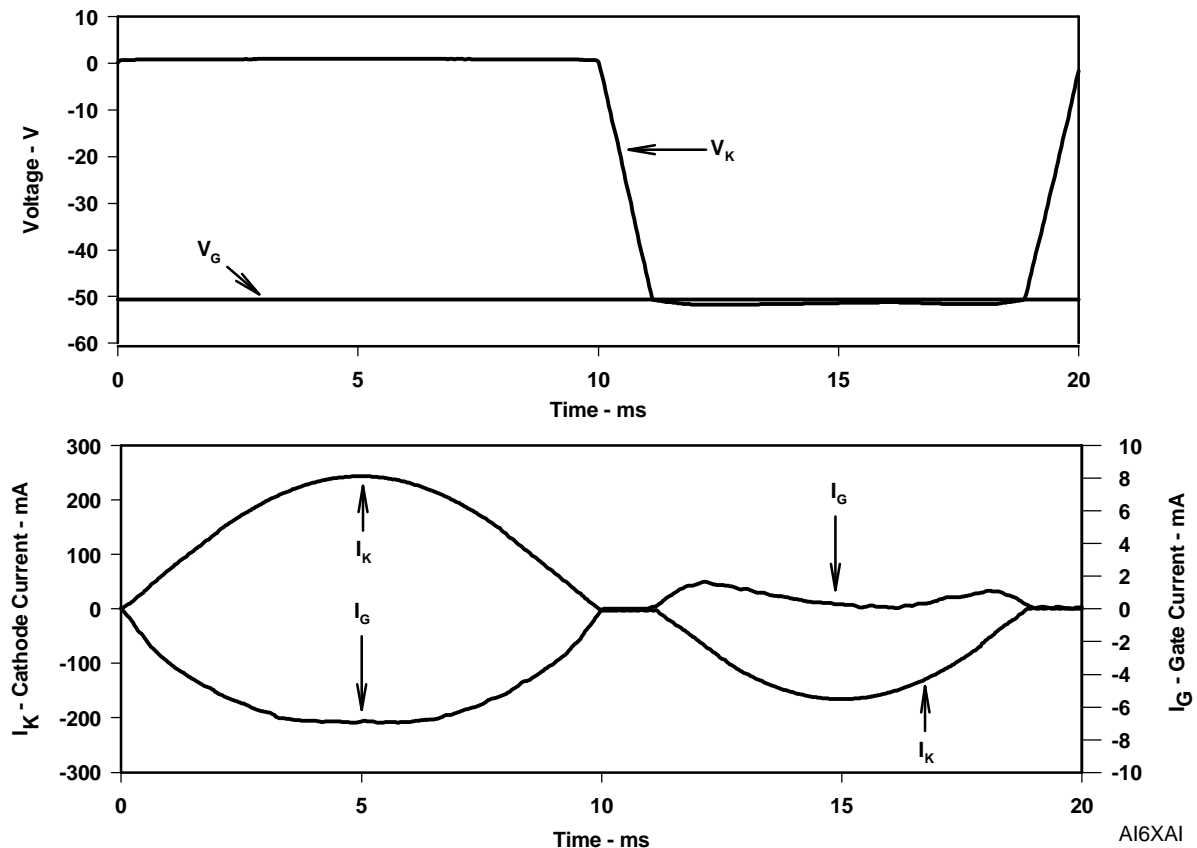


Figure 6. TISP61060 HIGH IMPEDANCE POWER CROSS CLIPPING WAVE FORMS

energy capability. Second, the series gate diodes have been changed to transistor buffers. The maximum current injected into the gate supply is then reduced by the transistors gain factor (H_{FE}). Third, some current from the positive voltage diode conduction has been diverted to the gate terminal which subtracts from the normal gate current. In most cases, this allows any previously used SLIC supply rail shunt protection diode to be removed. Although the SLIC supply is taken to a terminal that is internally connected to transistor bases, the terminal is still designated as the gate terminal, G.

Figure 6 shows the high impedance a.c. waveforms for the TISP61060. As the TISP61060 replaces the IC based protector's gate diode with a transistor, the peak gate current is reduced by over 50 times. In addition there is a compensating negative gate current flow during diode conduction. The TISP61060 has the maximum value of peak gate current specified and so allows for designer to design for limit conditions. Most IC protectors do not specify this parameter. Figure 7 shows the improvement due to the TISP61060. These plots show the full cycle average gate current against rms a.c. voltage. The IC based protector has a substantial positive gate current which will always charge the SLIC supply, possibly causing an overvoltage. The TISP61060 has a negative gate current and so cannot overvoltage the SLIC.

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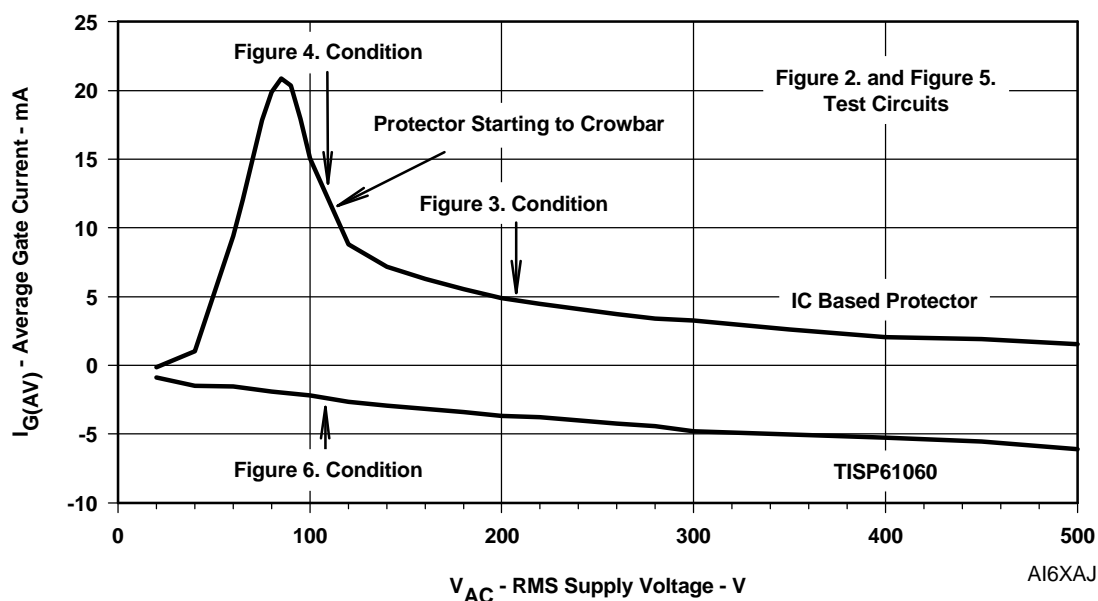


Figure 7. AVERAGE GATE CURRENT VS A.C. SUPPLY VOLTAGE IN FIGURES 2 AND 5

circuit component values

The TISP61060 is a functional replacement for three devices, the LB1201, TCM1030 and TCM1060. These devices have a minimum value of series limiting resistor (R1 and R2 in Figure 2) which will ensure that the impulse surge current will not exceed the device rated value. This is summarised in the table below.

DEVICE		10/1000 1 kV, 10 Ω	10/160 1.5 kV, 7.5 Ω	2/10 2.5 kV, 5 Ω	RECOMMENDED MIN. SERIES RESISTANCE Ω
LB1201	I_{TSP} A	12.5	18.5	23	100
	MIN. SERIES RESISTANCE Ω	70	73.6	104	
TCM1030	I_{TSP} A	16	25	35	100
	MIN. SERIES RESISTANCE Ω	52.5	52.5	66.4	
TCM1060	I_{TSP} A	30	45	50	50
	MIN. SERIES RESISTANCE Ω	23.3	25.8	45	
TISP61060	I_{TSP} A	30	45	50	50
	MIN. SERIES RESISTANCE Ω	23.3	25.8	45	

This table shows that the TISP61060 has impulse ratings which are higher or equal to those of the other three devices. Similarly, the TISP61060 has a.c. ratings which are higher or equal to those of the other three devices. A series over-current protector should be included in the wire feed to prevent exceeding the

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TISP61060 a.c. ratings. As covered earlier, the gate decoupling capacitor should be 100 nF and should be mounted as close to the protector as possible.

application circuit

Figure 8 shows a typical TISP61060 SLIC card protection circuit. The incoming line wires, R and T, connect to the relay matrix via the series over-current protection. Fusible resistors, fuses and positive temperature coefficient (PTC) resistors can be used for over-current protection. Resistors will reduce the prospective current from the surge generator for both the TISP61060 and the ring/test protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration maybe ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-wire protection voltage is twice the wire to ground value.

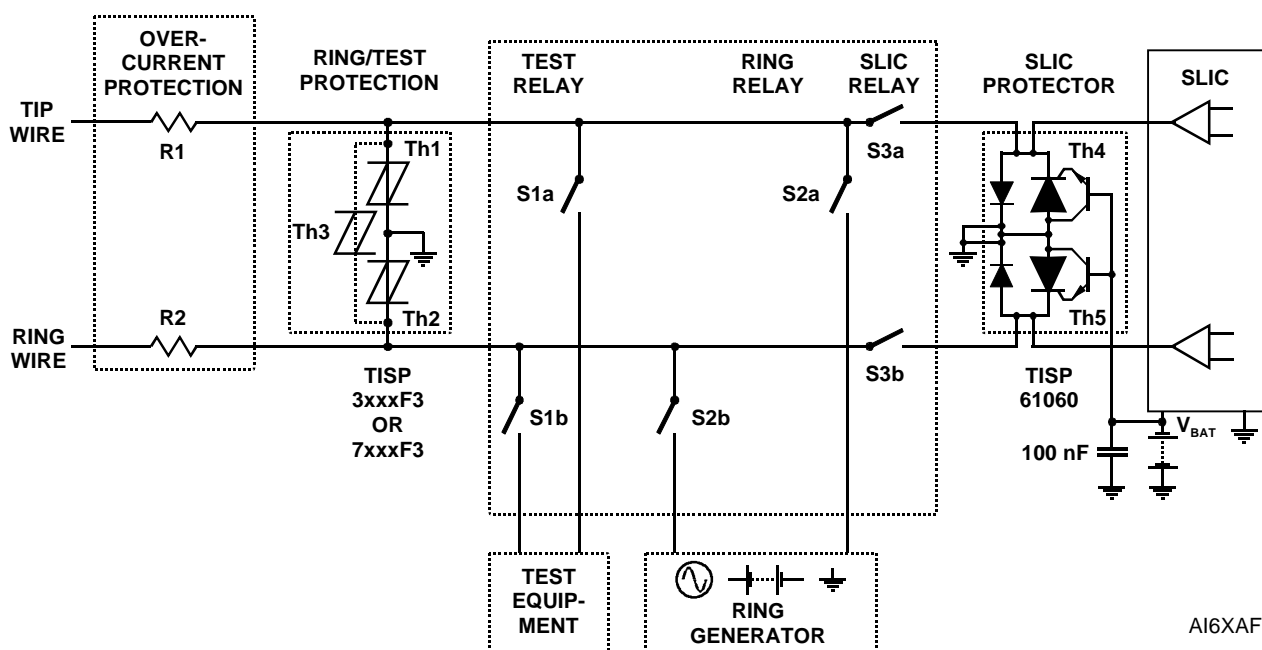


Figure 8. TYPICAL APPLICATION CIRCUIT

Relay contacts 3a and 3b connect the line wires to the SLIC via the TISP61060 protector. The protector gate reference voltage comes from the SLIC negative supply (V_{BAT}). A 100 nF gate capacitor sources the high gate current pulses caused by fast rising impulses.

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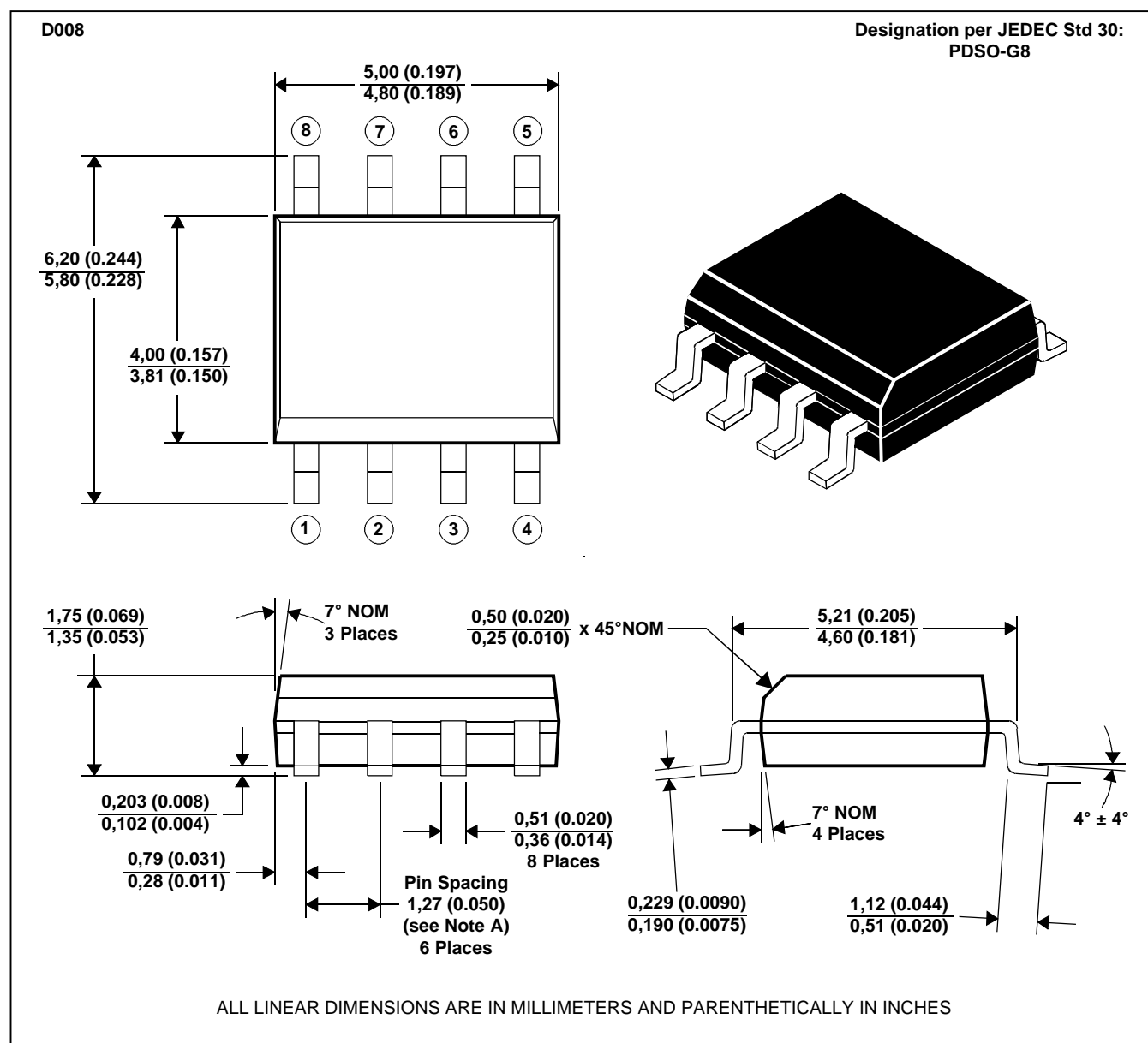
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MECHANICAL DATA

D008

plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

MDXXAA

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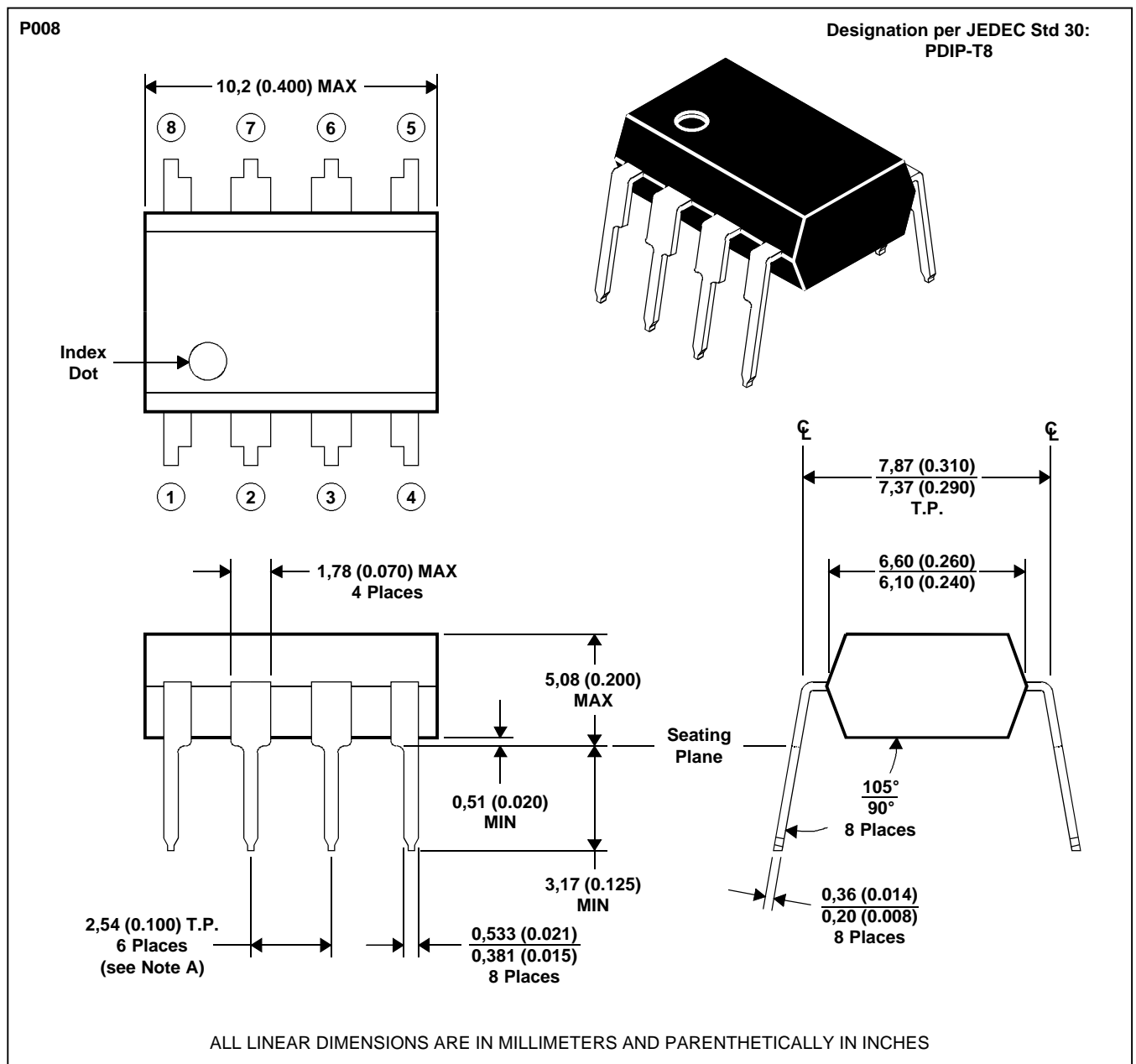
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MECHANICAL DATA

P008

plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position

MDXXABA

TISP61060D, TISP61060P
DUAL FORWARD-CONDUCTING P-GATE THYRISTORS
PROGRAMMABLE OVERVOLTAGE PROTECTORS

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