Monolithic Digital IC

SANYO

No.3323

LB1619M

3-Phase Brushless Motor Driver

Applications

The LB1619M is a 3-phase brushless motor driver IC ideally suited for use in VTR capstan motor driver, drum motor driver applications.

Features

· 120° voltage linear type

Supply Voltage

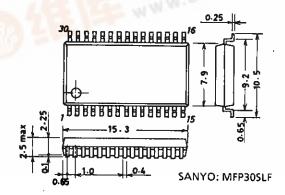
- · Speed control based on motor voltage control
- · Soft switching type eliminating noises caused by current switching and making the values of external capacitors smaller (comparable to those of chip capacitors)
- · On-chip torque ripple compensation circuit
- · On-chip thermal shutdown circuit

Absolute Maximum Ratings at	$Ta = 25^{\circ}C$		unit
Maximum Supply Voltage	V _{CC} max	16	v
Maximum Supply Voltage	V _S max	V_{CC}	V
Output Current	IO	1.5	Α
Hall Supply Current	I_{H}	20	mA
Allowable Power Dissipation	Pd max	1.0	W
Operating Temperature	Topr	-20 to +75	°C
Storage Temperature	Tstg	-55 to +125	°C
Allowable Operating Condition	Dron		C.C.C
Allowable Operating Conditio		unit	

 V_{CC}

(Design Notes) It should be noted that dielectric breakdown is liable to occur between pin 11 and other pins.

Package Dimensions 3073A-M30IC (unit: mm)

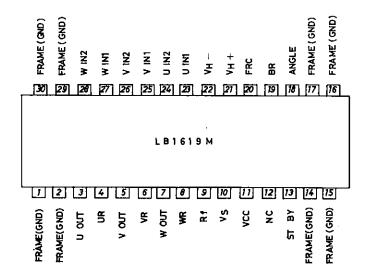


6 to 16

Electrical Characteristics at Ta = 25°C, V _{CC} = 12V, V _S = 3V min typ max							
Supply Current 1	I_{CC}	$V_{BR} = 5V$		18	23	mA	
Supply Current 2	I_S	$V_{BR} = 5V$		5.0	7.0	mA	
Supply Standby Current	I_{CCOQ}	$V_{STBY} = 0V$			180	μΑ	
Output Saturation Voltage	Vo (sat)	$I_{OUT} = 1.0A$, sink + source	•		2.3	V	
Output Transistor	$V_{O(sus)}$	$I_{OUT} = 20 \text{mA} \%$	16			V	
Breakdown Voltage							
Output Standby Voltage	v_{oq}	$V_{BR} = 5V$	1.43	1.53	1.63	V	
Hall Amp Input Offset Voltage	V_{HOFFse}	t *	-5		+5	mV	
Hall Amp Common-Mode	V_{HCOM}		1.4		2.8	V	
Input Voltage Range							
Hall Input-Output Voltage Gain	$G_{ m VHO}$	Under specified circuit conditions	31.5	34.5	37.5	dB	
Brake Pin 'H'-Level Voltage			2.0			V	
Brake Pin 'L'-Level Voltage					0.8	V	
Brake Pin Input Current					100	μA	
Brake Pin Leak Current					-30	μA	
FRC Pin 'H'-Level Voltage			2.8			v	
FRC Pin 'L'-Level Voltage					1.2	V	
FRC Pin Input Current					100	μА	
FRC Pin Leak Current					-30	μA	
Hall Supply Voltage	V_{H}	$I_{H} = 10 \text{mAV}_{H}^{(+)} - V_{H}^{(-)}$	0.8	1.0	1.5	V	
Upper Residual Voltage	V_{XH}	$I_{OUT} = 100 \text{mA}$	0.40	0.6	0.75	V	
Lower Residual Voltage	V_{XL}	$I_{OUT} = 100 mA$	0.5	0.6	0.7	V	
Residual Voltage Inflection Point	ţ			2.0		V	
Overlap Amount		$V_{\rm CC}$ =12 V , $V_{\rm S}$ =3.5 V	60	70	80	%	
Operating Temperature of		※	150	180	210	°C	
Thermal Shutdown Circuit							
Hysteresis of Thermal		*		15		$^{\circ}\mathrm{C}$	
Shutdown Circuit							
Standby Operating Voltage					0.1	V	
Standby Bias Current		Pin GND			10	μΑ	
V _S OFF-State IC Flow-out∕in Cur	rent	Number of revolutions: 1260rp	m		0.8	Α	

Note) × : Values shown are design targets only. No measurements have been taken. Overlap amount : Value measured at the time of shipment

Pin Assignment



Note: All FRAME pins are connected to GND.

Truth Table

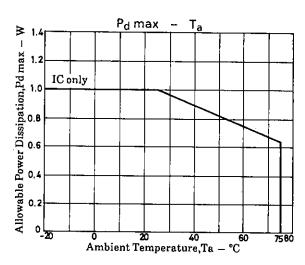
				Τ.	Input		Forward/Reverse	
	Source		Sink		v	w	Control	
1	W phase	→	V phase] ,,			L	
	V phase	→	W phase	H	Н	L	н	
	W phase				L ·			
2	U phase	→	W phase	H	L	L	Н	
	V phase	· →	W phase		Ľ	н	L	
3	W phase	>	V phase	l r			Н	
	U phase	→	V phase		н	L	L	
4	V phase	→	U phase	L			Н	
_	V phase	→	U phase	<u> </u>	L.	н	L	
5	U phase	→	V phase	H			Н	
6	U phase	→	W phase	Ι,	Н	Н	L	
	W phase	→	U phase	L			Н	

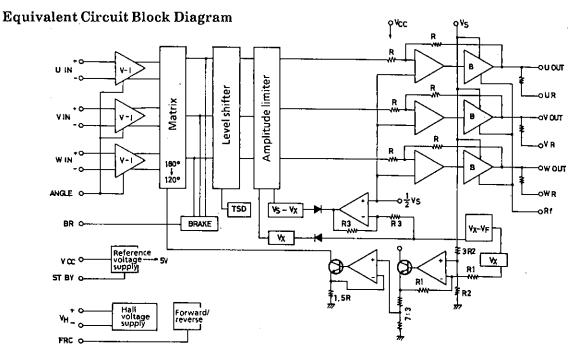
Input:

- H: High level. One of the inputs should have a potential at least 0.2V higher than the other.
- 0.2V higher than the other.
 L: Low level. One of the inputs should have a potential at least 0.2V lower than the other.

Forward/reverse control:

H:2.8 to 5V L: 0 to 1.2V





Pin Description

Unit (resistance: Ω)

	cription			Unit (resistance: 12)
Pin No.	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Function
1,2 14,15 16,17 29,30	FRAME (GND)		·	GND for other than output
3 5 7	U _{out} V _{out} W _{out}		0V _S 3 3 √ 3 √ 7	Output pins
4 6 8	U _R V _R W _R		RI 6	Output pins with resistor of 2Ω
9	R_{f}			GND for output transistor
10	V _S	<v<sub>CC2</v<sub>		Power supply pin for fixing the output amplitude. Must be lower than $V_{\rm CC}2$ voltage.
11	v_{cc}			Power supply pin for power amp circuit other than motor driver transistor.
13	ST, BY	L: 0.1V max H: 2.0V min	100x 100x 100x 100x 100x 100x 100x 100x	When this pin is grounded, all the circuitry stops operating. In this case, the supply current is approximately 100µA. In the normal operation mode, this pin is left open or made to be at a potential of more than 2V.
18	ANGLE		vcc www.	The hall input-output gain (slope of motor waveform) can be changed by changing the resistance connected across this pin and GND. $\rightleftharpoons 10 \mathrm{k}\Omega$
19	BR	H: 2.0V min L: 0.8V max	5V 100k 100k 100k 100k 100k 100k 100k 100	Pin for stopping the motor L level: Motor drive (Less than 0.8V) H level: Motor stop (More than 2.0V)

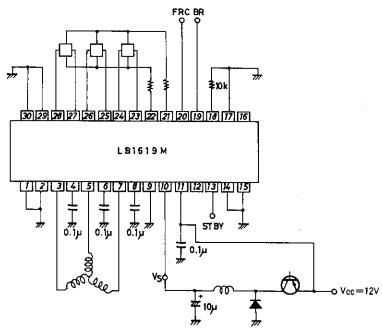
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Unit (resistance: Ω)

Pin No.	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Function
20	FRC	H:2.8V min L: 1.2V max	100k 100k 100k 100k 100k 100k 100k 100k	Pin for forward/reverse control of motor L level: Forward (Less than 1.2V) H level: Reverse (More than 2.8V)
21 22	V _H + V _H -		20k 9k \$ 7	Pin for supplying the hall bias current A voltage of approximately 1V is developed across (V _H +) and (V _H -).
23 24 25 26 27 28	U _{IN} 1 U _{IN} 2 V _{IN} 1 V _{IN} 2 W _{IN} 1 W _{IN} 2	1.4V min 2.8V max	200 200 200 200 200 200 200 200 200 200	U phase hall element input pin Logic "H": $U_{IN}1>U_{IN}2$ V phase hall element input pin Logic "H": $V_{IN}1>V_{IN}2$ W phase hall element input pin Logic "H": $W_{IN}1>W_{IN}2$

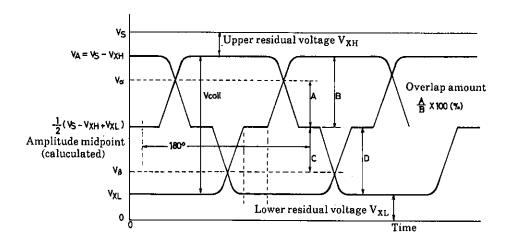
Note) Pin 12 (NC pin) must be left open.

Sample Application Circuit



Unit (resistance: Ω , capacitance: F)

Output Voltage Waveform



Upper overlap =
$$(2V_a - V_A - V_{XL}) / (V_A - V_{XL}) \times 100[\%]$$

Lower overlap = $(V_A + V_{XL} - 2V_B) / (V_A - V_{XL}) \times 100[\%]$

1. Upper overlap

DC voltage of upper amplitude: $V_S - V_{XH} = V_A$

DC voltage of lower amplitude: VXL

Let the DC voltage at the intersection of two phases of the upper waveform be $V\alpha$:

From the drawing shown above

At upper overlap amount = $A/B \times 100[\%]$

$$A = Va - 1/2 (V_S - V_{XH} + V_{XL}) = Va - 1/2 (V_A + V_{XL})$$

$$B = (V_S - V_{XH}) - 1/2 (V_S - V_{XH} + V_{XL}) = 1/2 (V_A + V_{XL})$$

※ Upper overlap

$$=(2V\alpha - V_A - V_{XL})/(V_A - V_{XL}) \times 100[\%]$$

2. Lower overlap

DC voltage of upper amplitude: $V_S - V_{XH} = V_A$

DC voltage of lower amplitude: VXL

Let the DC voltage at the intersection of two phases of the upper waveform be $V\beta$:

From the drawing shown above

At lower overlap amount = C/D × 100[%]

$$C = 1/2 (V_S - V_{XH} + V_{XL}) - V\beta = 1/2 (V_A + V_{XL}) - V\beta$$

$$D = 1/2 (V_S - V_{XH} + V_{XL}) - V_{XL} = 1/2 (V_A - V_{XL})$$

* Lower overlap

$$=(V_A + V_{XL} - 2V\beta)/(V_A - V_{XL}) \times 100[\%]$$

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