Ordering number : EN4264A

Monolithic Digital IC

LB1824

Power Brushless Motor Driver for OA Equipment

Overview

The LB1824 produces the direct PWM drive output appropriate for the brushless motors used in office data processing (OA) equipment, and integrates on a single chip the speed control circuits, FG amplifier, and other circuits required to form the drive circuit.

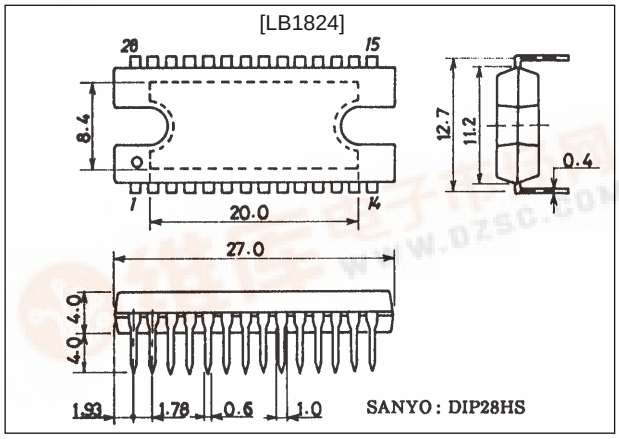
Features

- Breakdown voltage: 30 V, output current: 2.5 A
- Direct PWM drive output
- Crystal oscillator circuit
- Speed discriminator plus PLL speed control system
- Forward/reverse switching circuit
- Start/stop switching circuit
- Current control circuit
- Overheating protection circuit
- Built-in FG amplifier
- Lock detection output

Package Dimensions

unit: mm

3147A-DIP28HS



Specifications

Absolute Maximum Ratings at Ta = 25°C

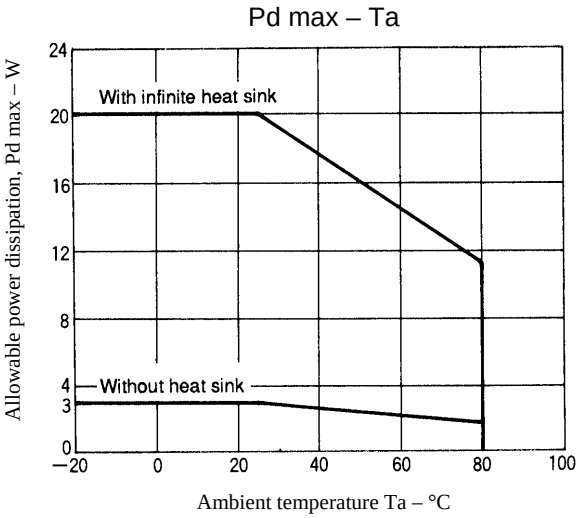
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		30	V
	V_M max		30	V
Output current	I_O max	T ≤ 100 ms	2.5	A
Allowable power dissipation	Pd max1	The IC independently	3	W
	Pd max2	With an arbitrary large heat sink	20	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

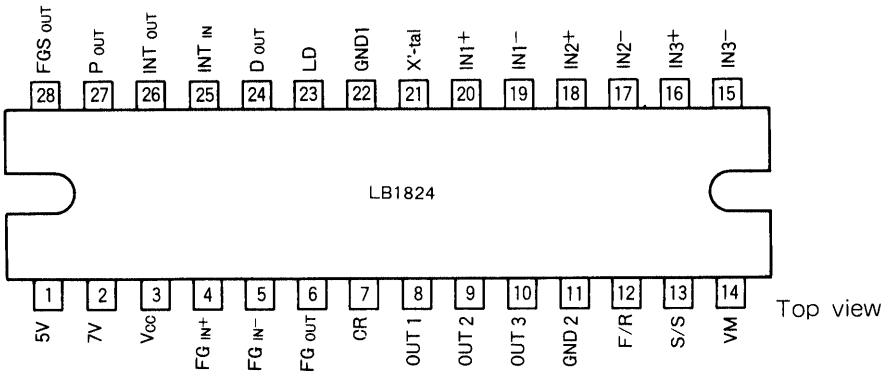
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		9.5 to 28	V
Supply voltage range	V_M		9 to 28	V
FG Schmitt output, applied voltage	V_{FGS}		0 to 8	V
Fixed voltage output current	I_{O1}	7 V output	0 to –20	mA
	I_{O2}	5 V output	0 to –20	mA
	I_{O3}	4 V output	0 to –15	mA
FG Schmitt output, output current	I_{FGS}		0 to 5	mA
Lock detection output current	I_{LD}		0 to 20	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = V_M = 24 V

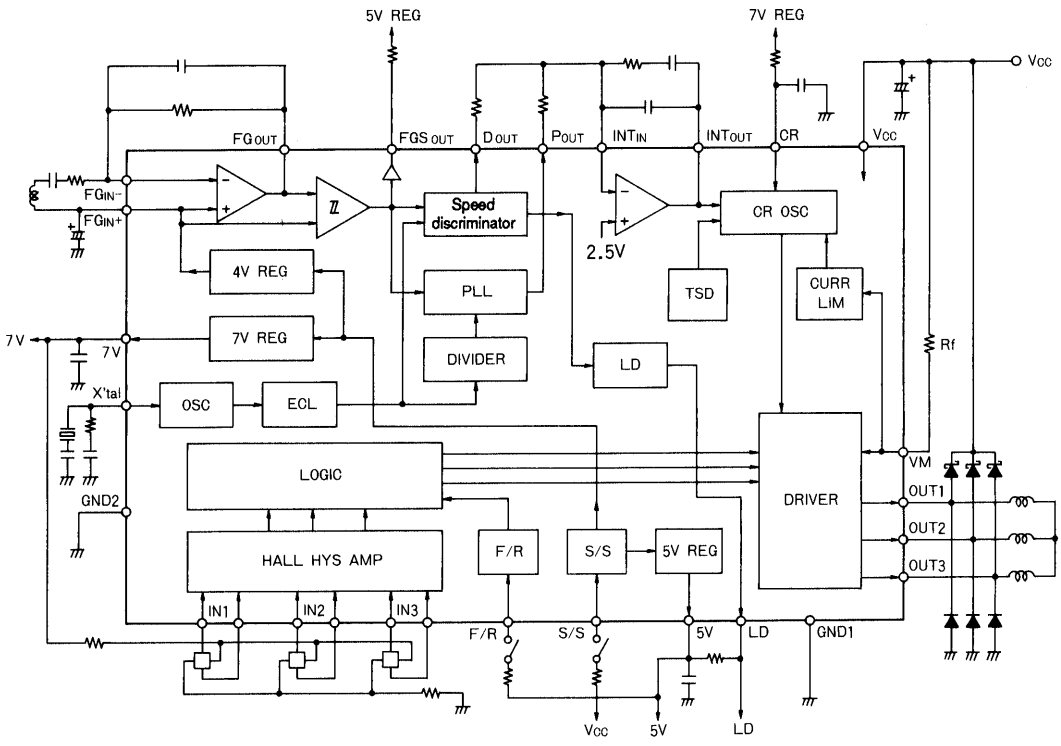
Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Current drain		I_{CC1}			34	50	mA
		I_{CC2}	When stopped		8	11	mA
Output saturation voltage		V_{Osat1}	I_O = 1A		2.0	3.0	V
		V_{Osat2}	I_O = 2A		2.7	4.2	V
Output leakage current		I_{Oleak}				100	µA
7 V fixed voltage output	Output voltage	V_H	I_O = –10 mA	6.65	7.0	7.35	V
	Voltage variation	ΔV_{H1}	V_{CC} = 9.5 to 28 V		50	200	mV
	Load variation	ΔV_{H2}	I_O = –5 to –20 mA		40	200	mV
5 V fixed voltage output	Output voltage	V_X	I_O = –5 mA	4.45	4.80	5.15	V
	Voltage variation	ΔV_{X1}	V_{CC} = 9.5 to 28 V		50	200	mV
	Load variation	ΔV_{X2}	I_O = –5 to –20 mA		5	200	mV
4 V fixed voltage output	Output voltage	V_{FG}	I_O = –5 mA	3.65	4.0	4.35	V
	Voltage variation	ΔV_{FG1}	V_{CC} = 9.5 to 28 V		40	200	mV
	Load variation	ΔV_{FG2}	I_O = –5 to –15 mA		110	200	mV
Hall amplifier	Input bias current	I_{HB}		–4	–1		µA
	Common mode input voltage range	V_{ICM}		1.5		5.1	V
	Hall input sensitivity			60			mVp-p
	Hysteresis	ΔV_{IN}		8	14	24	mV
	Input voltage low → high	V_{SLH}			7		mV
	Input voltage high → low	V_{SHL}			–7		mV
Oscillator	Output high level voltage	$V_{OH(CR)}$		2.8	3.1	3.4	V
	Output low level voltage	$V_{OL(CR)}$		0.8	1.1	1.4	V
	Oscillator frequency	$f_{(CR)}$	R = 56 kΩ, C = 1000 pF		15		kHz
	Amplitude	$V_{(CR)}$			2.0		Vp-p
Current control operation	Limiter	V_{CC} –V_M		0.4	0.5	0.6	V
Thermal shutdown operation	Thermal shutdown operating temperature	TSD	Design target	150	180		°C
	Hysteresis	ΔTSD			50		°C
FG amplifier	Input offset voltage	$V_{IO(FG)}$		–10		+10	mV
	Input bias current	$I_{B(FG)}$		–1		+1	µA
	Output high level voltage	$V_{OH(FG)}$	I_{FG} = –2 mA	5.5	6		V
	Output low level voltage	$V_{OL(FG)}$	I_{FG} = 2 mA		1	1.5	V
	FG input sensitivity		100x gain	3			mV
	Next stage Schmitt width			100	180	250	mV
	Operating frequency range					2	kHz
	Open loop gain		$f_{(FG)}$ = 2 kHz	45	51		dB
FGS output	Output saturation voltage	$V_{O(FGS)}$	$I_{O(FGS)}$ = 2 mA		0.1	0.5	V
	Output leakage current	$I_{L(FGS)}$	V_O = 5 V			10	µA
Speed discriminator	Output high level voltage	$V_{OH(D)}$		4.0	4.3		V
	Output low level voltage	$I_{OL(D)}$			0.8	1.1	V
	Number of counts				512		
PLL output	Output high level voltage	$V_{OH(P)}$		3.2	3.5	3.8	V
	Output low level voltage	$V_{OL(P)}$		1.2	1.5	1.8	V
Lock detection	Output low level voltage	$V_{OL(LD)}$	I_{LD} = 10 mA		0.15	0.5	V
	Locking range				±6.25		%
Integrator	Input bias current	$I_{B(INT)}$		–0.4		+0.4	µA
	Output high level voltage	$V_{OH(INT)}$		3.7	4.3		V
	Output low level voltage	$V_{OL(INT)}$			0.8	1.2	V
	Open loop gain			60			dB
	Gain-bandwidth product				1.6		MHz
	Reference voltage			–5%	V_X/2	5%	V
Crystal oscillator	Operating frequency range	f_{OSC}		1		10	MHz
Start/stop pin	Input high level voltage	$V_{IH(S/S)}$		4.0			V
	Input low level voltage	$V_{IL(S/S)}$				1.5	V
	Pull-down resistance	$R_{D(S/S)}$		30	50	70	kΩ
Forward/reverse pin	Input high level voltage	$V_{IH(F/R)}$		4.0			V
	Input low level voltage	$V_{IL(F/R)}$				1.5	V
	Hysteresis	ΔV_{IN}			0.5		V
	Pull-down resistance	$R_{D(F/R)}$		30	50	70	kΩ



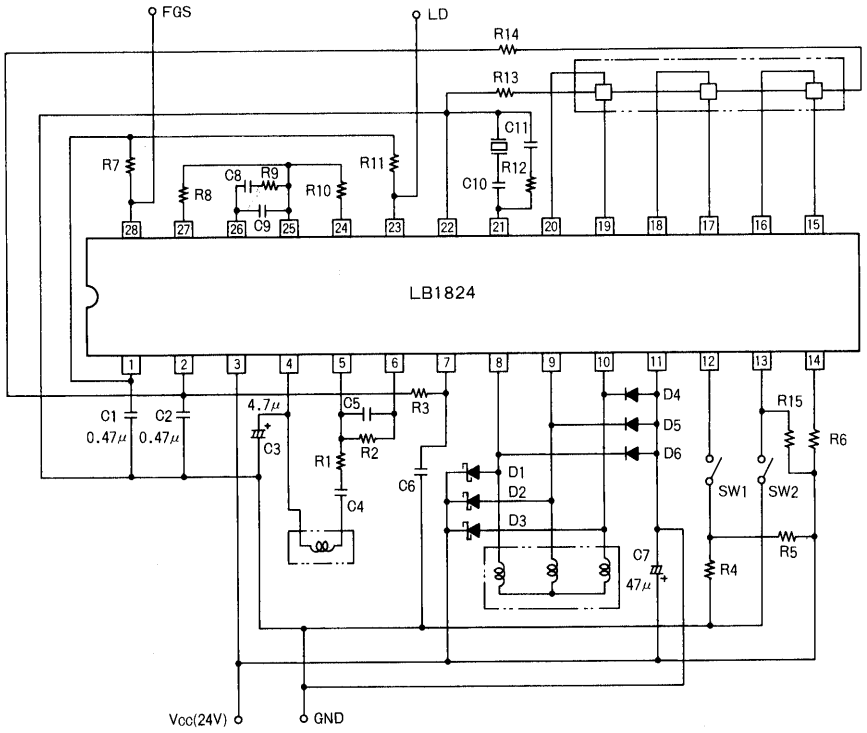
Pin Assignment



Equivalent Circuit Block Diagram

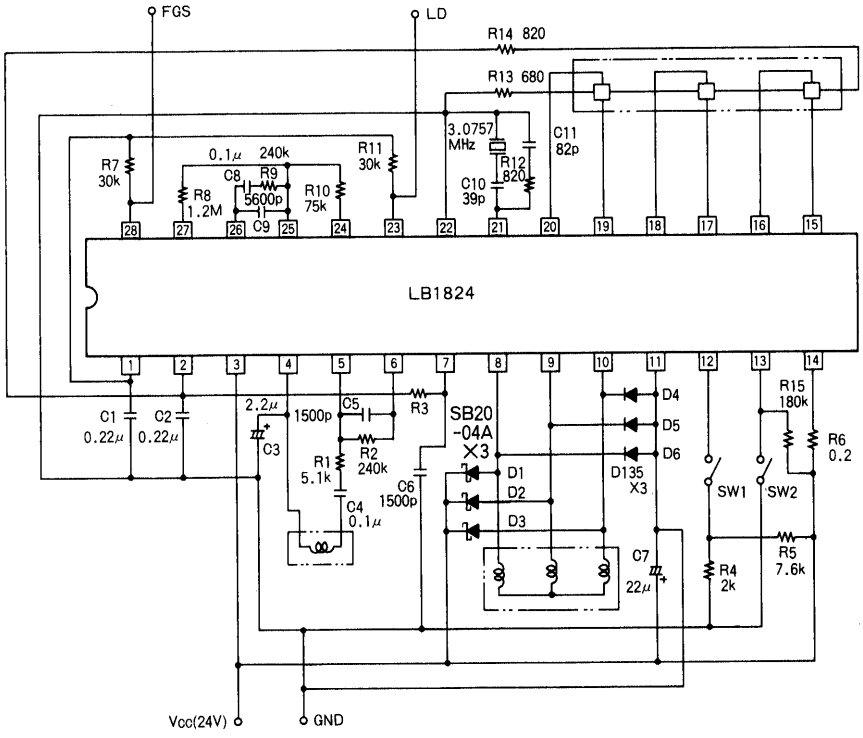


Sample Application Circuit



Unit (capacitance: F)

AC Test Circuit Diagram



Unit (resistance: Ω, capacitance: F)

Logic Table

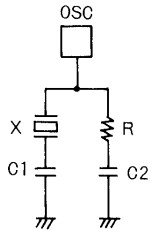
Parameter	Source → Sink	F/R = Low			F/R = High		
		IN1	IN2	IN3	IN1	IN2	IN3
1	OUT3 → OUT2	H	H	L	L	L	H
2	OUT3 → OUT1	H	L	L	L	H	H
3	OUT2 → OUT3	L	L	H	H	H	L
4	OUT1 → OUT2	L	H	L	H	L	H
5	OUT2 → OUT1	H	L	H	L	H	L
6	OUT1 → OUT3	L	H	H	H	L	L

Note: 'H' for an input indicates the state where IN+ > IN–.
H: High
L: Low

The formula below gives the relationship between the crystal oscillator frequency (f_{OSC}) and the FG frequency (f_{FG}).

f_{FG} (servo) = f_{OSC}/(the ECL divider factor (16) × the number of counts)
= f_{OSC}/8192

(External crystal oscillator circuit)



External Constants (reference values)

X'tal (MHz)	C1 (pF)	C2 (pF)	R (kΩ)
3 to 4	39	82	0.82
4 to 5	39	82	1.0
5 to 7	39	47	1.5
7 to 10	39	27	2.0

Note that the crystal used should have a ratio between the fundamental wave f_O impedance and $3f_O$ impedance of 1:5 or greater.

Pin Functions

Pin name	Pin No.	Function
IN1+, IN1– IN2+, IN2– IN3+, IN3–	20, 19 18, 17 16, 15	OUT1 Hall input pin OUT2 Hall input pin OUT3 Hall input pin
OUT1	8	Output pin 1
OUT2	9	Output pin 2
OUT3	10	Output pin 3
V_{CC}	3	Pin for the power supply applied to all blocks other than the output block
V_M	14	Output block power supply pin. Also used for output current detection: connecting a resistor (R_f) between this pin and V_{CC} allows the output current to be detected as a voltage.
GND1	22	Ground for all blocks other than the output block
GND2	11	Output block ground
CR	7	Pin for setting the PWM oscillator frequency
INT IN	25	Integrator input pin
INT OUT	26	Integrator output pin (speed control pin)
D OUT	24	Speed discriminator output pin: overspeed → high
P OUT	27	PLL output pin
LD	23	Lock detection pin. Open collector output. Goes low when the motor speed is within the lock range (±6.25%).
FG IN+ FG IN–	4 5	FG pulse input pin (4 V power supply pin)
FG OUT	6	FG amplifier output pin
FGS OUT	28	FG amplifier output pin (post-schmitt). Open collector output.
X'tal	21	Crystal oscillator pin. Connect the crystal oscillator to this pin.
5 V	1	5 V power supply pin
7 V	2	7 V power supply pin
S/S	13	Start/stop control pin Start → low, stop → high
F/R	12	Forward/reverse control pin Forward → low, reverse → high

LB1824 Functional Description (including external components)

1. Speed control circuit

The LB1824 uses a combination of a speed discriminator circuit and a PLL circuit for speed control. The speed discriminator circuit outputs an error signal once every two FG periods using a charge pump method. The PLL circuit outputs a phase error signal once every FG period also using a charge pump method. As compared with earlier speed control methods that used only a speed discriminator circuit, the combination of both a PLL circuit as well as a speed discriminator circuit employed in the LB1824 results in improved suppression of speed variations in cases where motors with large load variations are used. Since the FG servo frequency determined as shown in the formula below, the motor speed is set by the FG pulse count and the crystal oscillator frequency.

$f_{FG}(servo) = f_{OSC}/8192$
f_{OSC} = crystal oscillator frequency

2. Direct PWM drive

The LB1824 adopts a direct PWM drive method in order to reduce the power loss at the output. The output transistor is always saturated when on, and it adjusts the motor drive power by varying the duty that the output is on. Since the output switching is performed by the lower side transistor, Schottky diodes (D1, D2 and D3) must be attached between OUT and V_{CC}. (This is because if diodes with a short reverse recovery time are not used, through current will flow at the instant that the lower side transistor turns on.) Normal forward current diodes can be used for the diodes between OUT and GND.

3. Current control circuit

The current control circuit performs its control operation with a current determined by $I = 0.5/R_f$. (This limits the peak current.) The control operation functions to reduce the on duty and thus suppress the current. No phase compensation capacitor is required.

4. Speed locking range

The speed locking range is within ±6.25% of the set speed, and when the motor speed enters the locking range the LD pin goes low (open collector output). When the motor speed is outside the locking range, the motor drive output on duty is changed according to the speed error, thus implementing the control required to return the motor speed to within the locking range.

5. PWM frequency

The PWM frequency is determined by the resistor R3 and the capacitor C6 that are attached to the CR pin.

- When R3 is connected to the 4 V fixed voltage power supply:
  $f_{PWM} \approx 1/(1.2 \times C \times R)$
- When R3 is connected to the 7 V fixed voltage power supply:
  $f_{PWM} \approx 1/(0.5 \times C \times R)$

Do not use a resistor of less than 30 kΩ for R3. A PWM frequency of about 15 kHz is desirable. If the PWM frequency is too low, the motor could oscillate at the PWM frequency during motor constraint and become noisy since the oscillation will be in the audible frequency range. On the other hand, if the PWM frequency is too high, the output transistor switching time loss will increase.

6. Ground leading

GND1 (pin 22): ground for blocks other than the output block
GND2 (pin 11): output block ground

Connect D4, D5 and D6 to GND2. All other external components should be connected to GND1. The GND1 and GND2 leads should be grounded at a single point at the connector. Since GND2 carries a large current, its lead should be as short as possible.

7. Output parasitic effect

   Parasitism occurs when the voltage on an output pin falls more than –0.7 V below GND1 and GND2. (The –0.7 V figure is reduced by the temperature characteristics.) Also, do not let the voltage on the output pins exceed V_{CC} by more than 1 V. When parasitism occurs, first speed control will be lost intermittently, and then, if it becomes larger, the output transistors can be damaged. D1, D2 and D3 are used to prevent through currents, and Schottky diodes with a low V_f should be used. Therefore the potential difference between the output pin and V_{CC} will not be a serious issue. Although normal forward current diodes can be used for D4, D5 and D6, care must be taken to keep the ground leads short, as mentioned in item 6 above, to avoid parasitism.

8. External interface pins

   - LD pin
     Output type: open collector
     Breakdown voltage: a maximum current voltage of 30 V
     Saturation voltage variance reference value (at I_{LD} = 10 mA)
     0.10 V to 0.15 V

   - FGS pin
     Output type: open collector
     Breakdown voltage: a maximum current voltage of 30 V
     Saturation voltage variance reference value (at I_{FGS} = 2 mA)
     0.12 V to 0.18 V
     FGS is the FG amplifier output converted to pulses by a hysteresis comparator (for high speed monitoring).

   - Start/stop pin
     Input type: PNP transistor base with a 50 kΩ pull-down resistor to ground
     Threshold level (typical): about 2.6 V
     Turns off the 4, 5 and 7 V fixed voltage power supplies in steps.

   - F/R pin
     Input type: PNP transistor base with a 50 kΩ pull-down resistor to ground
     Threshold level (typical): about 2.2 V (high → low), about 2.7 V (low → high)
     With a hysteresis of about 0.5 V.
     F/R switching must be performed when stopped.Continued from preceding page.

9. Fixed voltage power supply temperature characteristics

   - 4 V power supply: about –0.5 mV/°C (typical)
   - 5 V power supply: about –0.6 mV/°C (typical)
   - 7 V power supply: about –2.5 mV/°C (typical)

10. FG amplifier

    The FG amplifier gain is set by R1 and R2 to be a gain of G = R2/R1. C4 and C5 determine the FG amplifier's frequency characteristics. (R1 and C4 form a high pass filter, and R2 and C5 form a low pass filter.) Since a Schmitt comparator is connected following the FG amplifier, the FG amplifier's output must be set to be over 250 mVp-p by R1, R2, C4 and C5. (It is desirable that the FG output be between 1 to 3 Vp-p during normal motor rotation.)

11. External capacitors

    - C3
      C3 is required for FGIN+ pin fixed voltage power supply stabilization and for IC internal logic initial reset pulse generation. Although a low capacitance is acceptable for the power supply stabilization function, a relatively large capacitance (about 4.7 µF) is required for reset pulse generation. The reset pulse is generated when the FGIN+ pin goes from 0 V to about 1.3 V. If the reset does not occur, it is possible that LD could go on briefly at start time. If this phenomenon is not a problem, a value of 0.1 µF can be used for C3. After C3 has been charged to 4 V, when V_{CC} is turned off (or in stop mode) the charge on C3 is dissipated through an IC internal load resistance of about 10 kΩ that is connected to ground.

- C1 and C2
  C1 and C2 are required for fixed voltage power supply stabilization. Since this IC adopts a direct PWM method and a large current is switched at the output, noise is generated extremely easily. Accordingly, adequate stabilization is required on the power supplies so that noise does not cause incorrect circuit operation.
  The connections between C1, C2 and C3 and ground should be kept as short as possible. Special care should be exercised with respect to C1, since its characteristics are easily influenced by grounding problems.

12. External resistors

- R4 and R5
  R4 and R5 are used to apply a high level to the F/R pin. Since there is a pull-down resistance of about 50 kΩ on the F/R input pin it goes low when open. A high level input to the F/R pin should be at least 4.0 V and not more than 6.3 V.
- R15
  R15 is used to apply a high level to the S/S pin. Since there is a pull-down resistance of about 50 kΩ on the S/S input it goes low when open. (In the start state a high level input to the S/S pin should be at least 4.0 V and not more than 6.3 V.) As is the case with the F/R pin, the resistance is divided into 2 resistors, and while this scheme is resistant to noise (since the input impedance can be lowered), if noise is not a problem the high level can be set by connecting a single resistor such as R15. (A value of 180 kΩ is recommended.)

  If the initial rise in V_{CC} is slow (under about 10 V/ms) the motor may turn to some extent (in stop mode) when V_{CC} is first applied. This is because the S/S input voltage is resistor divided, and when V_{CC} is under 12 V, the input voltage will be under 2.6 V (the start input level). If the rise slope cannot be increased and this phenomenon is a problem, it can be handled by connecting a capacitor between V_{CC} and S/S.

13. Through currents due to the direct PWM method

  In the direct PWM method through currents flow in the outputs due to the switching, e.g., when used in a discrete structure or in LB1822 applications. This is due to the output transistor's delay and parasitic capacitance. Previously, an external capacitor was used to handle this kind of situation. However, the LB1824 provides internal circuit measures to handle this problem, and no measures based on external components are required. Although an overshoot with a duration of under 10 ns will appear on the RF voltage waveform during switching, this will not be a problem.

14. Oscillator

  A crystal oscillator is normally used with the LB1824. If the speed control conditions are not critical, a ceramic oscillator could be used. To avoid problems always consult the oscillator's manufacturer concerning the oscillator itself and the external resistances and capacitances used.

15. IC internal power dissipation calculation example (calculation for a V_{CC} of 24 V and typical ratings)

- Power dissipation due to the power supply current (I_{CC})
  At start time:
  $P1 = V_{CC} \times I_{CC1} = 24 \times 34\ m = 0.82\ W$
  At stop time:
  $P2 = V_{CC} \times I_{CC2} = 24 \times 8\ m = 0.19\ W$
- Power dissipation when a –10 mA load current is taken from the 7 V fixed voltage output
  $P3 = (V_{CC} - 7) \times 10\ m = 17 \times 10\ m = 0.17\ W$
- Power dissipation due to the output drive current (for an output on duty of 100%)
  $P4 = \{(V_{CC} - 1)^2/8\ k\} + \{(V_{CC} - 2)^2/10\ k\}$
  $= (23^2/8\ k) + (22^2/10\ k) = 0.12\ W$
- Power dissipation in the output transistor (For I_O = 2 A and an output on duty of 100%)
  $P5 = V_{Osat2} \times I_O = 2.7 \times 2 = 5.4\ W$

  Therefore the IC overall power dissipation is:
  At stop time:

P = P2 = 0.19 W
At start time:
P = P1 + P3 + P4 + P5 = 6.51 W
(for an output on duty of 100%)

16. Techniques for measuring the IC temperature increase

- Measurement with a thermocouple

When using a thermocouple to measure the IC temperature, the thermocouple should be attached to a fin. While this measurement technique is simple, it is subject to large measurement errors if the IC is not in a stable heat generation state.

- Measurement using the characteristics of an IC internal diode

We recommend using the parasitic diode between INT.IN and GND internal to the IC. (According to our data, I_D = 1 mA with about 1.8 mV/°C) Remove the external resistor when making the measurements.

17. Servo constants

When calculating the servo constants, they will be heavily dependent on the motor actually used. Since experience is generally required, these constants should be determined by the motor manufacturer. We can provide the IC characteristics data required for the servo constants calculations as well as frequency characteristics simulation data for the filter constants set by the motor manufacturer.

If the resistor connected between DOUT and INT.IN (R10) is too small, C8 and C9 are too large, and R10 is too large, speed errors will be likely to occur due to the speed discriminator cutoff current and the integrator input current. Therefore, a 10 to 100 kΩ resistor should be used. If the resistor connected between POUT and INT.IN (R8) is too small, the PLL system influence will become too large and the in-phase pull-in to locking will get worse. Therefore, do not make this value too small. (We recommend 1 MΩ when R10 is 75 kΩ.) First set the constants just for the speed discriminator system (R9, R10, C8 and C9) and then set the R8 value for the PLL system.