

Overview

The LB1871 and LB1871M are three-phase brushless motor driver ICs that are optimal for LBP and LBF polygon mirror motor drive. The LB1871 and LB1871M are versions of the LB1870 and LB1870M in which the value of the divisor has been changed.

Functions and Features

- Single-chip implementation of all circuits required for LBP polygon mirror motor drive (speed control and driver circuits)
- Low motor drive noise level due to the current linear drive scheme implemented by these ICs. Also, small capacitors suffice for motor output oscillation suppression, with certain motors not requiring these capacitors at all.
- Extremely high rotational precision provided by PLL speed control.
- Built-in phase lock detector output
- Four motor speed modes set by switching the clock divider provided under internal clock/crystal oscillator operation. This supports 240, 300, 400 and 480 dpi.
- Use of an external clock allows arbitrary motor speeds.
- Built-in FG and integrating amplifiers
- Full set of built-in protection circuits, including current limiter, undervoltage protection, and thermal protection circuits.

Specifications

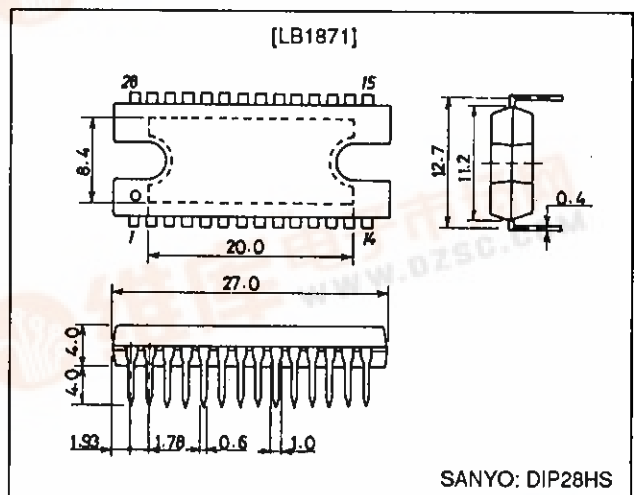
Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|---------------------------------|--------------|-------------------------------------|-------------|------------------|
| Maximum supply voltage | V_{CC} max | | 30 | V |
| Maximum output current | I_O max | $T < 0.1$ s | 1.0 | A |
| Allowable power dissipation (1) | Pd max1-1 | Independent IC (DIP28HS) | 3.0 | W |
| | Pd max1-2 | Independent IC (MFP36SLF) | 0.95 | W |
| Allowable power dissipation (2) | Pd max2 | With an arbitrarily large heat sink | 20 | W |
| Operating temperature | T_{opr} | | -20 to +80 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

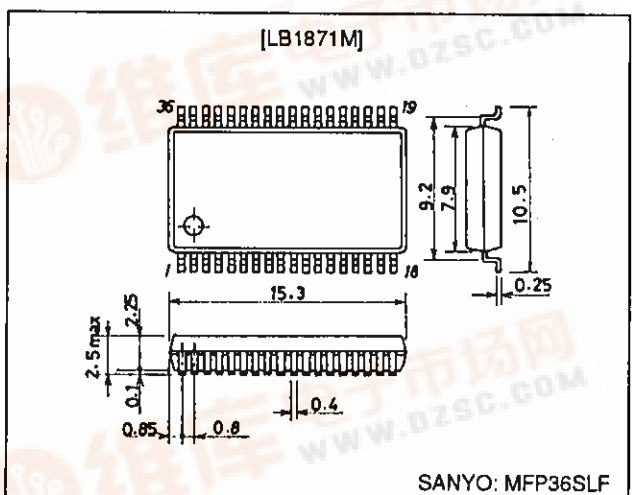
Package Dimensions

unit: mm

3147A-DIP28HS



3129-MFP36SLF



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Allowable Operating Conditions at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------------|-----------|------------|----------|------|
| Supply voltage range | V_{CC} | | 20 to 28 | V |
| 6.3 V fixed voltage output current | I_{REG} | | 0 to -15 | mA |
| LD pin voltage | V_{LD} | | 0 to +28 | V |
| FGS pin voltage | V_{FGS} | | 0 to +28 | V |
| LD pin output current | I_{LD} | | 0 to +10 | mA |
| FGS pin output current | I_{FGS} | | 0 to +5 | mA |

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 24\text{ V}$

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|-------------------|--|-----------------|-----------------|----------------|----------------------|
| Current drain | I_{CC} | Stop mode | | 22 | 32 | mA |
| [Output saturation voltage]: $V_{AGC} = 3.5\text{ V}$ | | | | | | |
| Source (1) | V_{sat1-1} | $I_O = 0.6\text{ A}$, $R_f = 0\ \Omega$ | | 1.8 | 2.5 | V |
| Source (2) | V_{sat1-2} | $I_O = 0.3\text{ A}$, $R_f = 0\ \Omega$ | | 1.6 | 2.3 | V |
| Sink (1) | V_{sat2-1} | $I_O = 0.6\text{ A}$, $R_f = 0\ \Omega$ | | 0.5 | 1.0 | V |
| Sink (2) | V_{sat2-2} | $I_O = 0.3\text{ A}$, $R_f = 0\ \Omega$ | | 0.25 | 0.7 | V |
| Output leakage current | I_O (LEAK) | $V_{CC} = 28\text{ V}$ | | | 100 | μA |
| [6.3 V fixed voltage output] | | | | | | |
| Output voltage | V_{REG} | | 5.8 | 6.3 | 6.8 | V |
| Voltage variation | ΔV_{REG1} | $V_{CC} = 20\text{ to }28\text{ V}$ | | | 200 | mV |
| Load variation | ΔV_{REG2} | $I_O = 0\text{ to }-10\text{ mA}$ | | | 200 | mV |
| Temperature coefficient | ΔV_{REG3} | Design target value | | 0 | | mV/ $^\circ\text{C}$ |
| Short circuit current | ISV_{REG} | Design target value | | 70 | | mA |
| [Hall input block] | | | | | | |
| Input bias current | I_B (HA) | | | 2 | 10 | μA |
| Differential input range | V_{HIN} | Sine wave input | 50 | | 350 | mVp-p |
| Common-mode input range | V_{ICM} | Differential input: 50 mVp-p | 3.5 | | $V_{CC} - 3.5$ | V |
| Input offset voltage | V_{IOH} | Design target value | -20 | | +20 | mV |
| [Undervoltage protection] | | | | | | |
| Operating voltage | V_{SD} | | 8.4 | 8.8 | 9.2 | V |
| Hysteresis | ΔV_{SD} | | 0.2 | 0.4 | 0.6 | V |
| [Thermal protection] | | | | | | |
| Thermal shutdown operating temperature | TSD | Design target value (junction temperature) | 150 | 180 | | $^\circ\text{C}$ |
| Hysteresis | ΔTSD | Design target value (junction temperature) | | 40 | | $^\circ\text{C}$ |
| [Current limiter operation] | | | | | | |
| Limiter | V_{RF} | | 0.52 | 0.58 | 0.63 | V |
| [FG amplifier] | | | | | | |
| Input offset voltage | V_{IO} (FG) | Design target value | -10 | | +10 | mV |
| Input bias current | I_B (FG) | | -1 | | +1 | μA |
| DC bias level | V_B (FG) | | -5% | $1/2 V_{REG}$ | +5% | V |
| Output high level voltage | V_{OH} (FG) | No external load | $V_{REG} - 1.3$ | $V_{REG} - 0.8$ | | V |
| Output low level voltage | V_{OL} (FG) | No external load | | 0.8 | 1.2 | V |
| [FG Schmitt block] | | | | | | |
| Input hysteresis (high to low) | V_{SHL} | | | 0 | | mV |
| Input hysteresis (low to high) | V_{SLH} | | | 150 | | mV |
| Hysteresis | V_{FGL} | | 100 | | 200 | mV |
| Input operating level | V_{FGSIL} | | 400 | | | mVp-p |
| Output saturation voltage | V_{FGS} (sat) | $I_{FGS} = 4\text{ mA}$ | | 0.2 | 0.4 | V |
| Output leakage current | I_{FGS} (LEAK) | $V_{CC} = 28\text{ V}$ | | | 10 | μA |

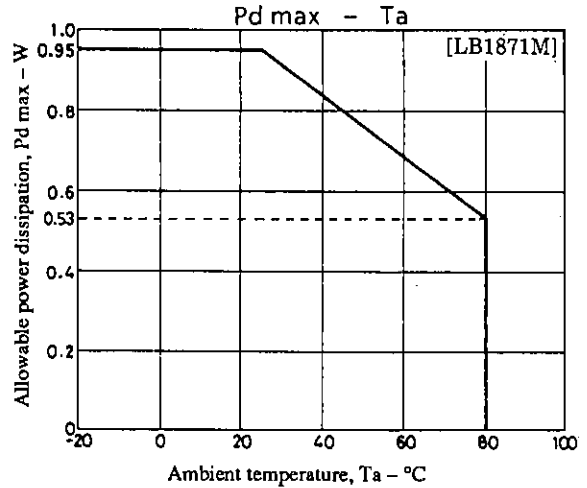
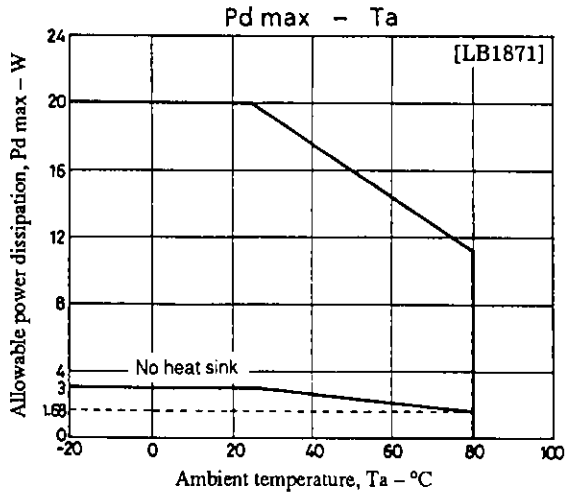
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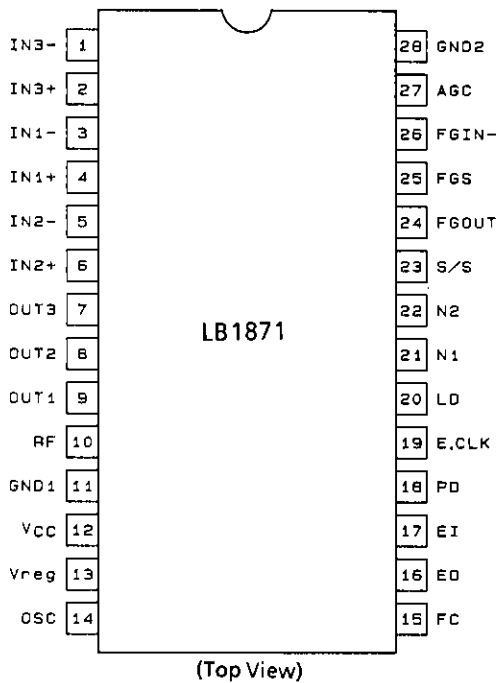
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| Parameter | Symbol | Conditions | min | typ | max | Unit |
|------------------------------|-----------------|------------------------------|-----------------|---------------|-----------|---------|
| [Error amplifier] | | | | | | |
| Input offset voltage | V_{IO} (ER) | Design target value | -10 | | +10 | mV |
| Input bias current | I_B (ER) | | -1 | | +1 | μ A |
| DC bias level | V_B (ER) | | -5% | $1/2 V_{REG}$ | +5% | V |
| Output high level voltage | V_{OH} (ER) | No external load | $V_{REG} - 1.0$ | | | V |
| Output low level voltage | V_{OL} (ER) | No external load | | | 1.0 | V |
| [Phase comparator output] | | | | | | |
| Output high level voltage | V_{POH} | No external load | $V_{REG} - 0.4$ | | | V |
| Output low level voltage | V_{PDL} | No external load | | | 0.4 | V |
| Output source current | I_{PD}^+ | $V_{PD} = V_{REG}/2$ | | | -0.6 | mA |
| Output sink current | I_{PD}^- | $V_{PD} = V_{REG}/2$ | 1.5 | | | mA |
| [Lock detector output] | | | | | | |
| Output saturation voltage | V_{LD} (sat) | $I_{LD} = 5$ mA | | 0.1 | 0.4 | V |
| Output leakage current | I_{LD} (LEAK) | $V_{CC} = 28$ V | | | 10 | μ A |
| [Drive block] | | | | | | |
| Dead zone | V_{DZ} | | 50 | 100 | 300 | mV |
| Output idling voltage | V_{ID} | | | | 6 | mV |
| Forward gain | G_{DF}^+ | | 0.4 | 0.5 | 0.6 | |
| Reverse gain | G_{DF}^- | | -0.6 | -0.5 | -0.4 | |
| Accelerate command voltage | V_{STA} | | 5.0 | 5.6 | | V |
| Decelerate command voltage | V_{STO} | | | 0.8 | 1.5 | V |
| Forward limiter voltage | V_L^+ | $R_I = 22 \Omega$ | | 0.58 | | V |
| Reverse limiter voltage | V_L^- | $R_I = 22 \Omega$ | | 0.58 | | V |
| [Reference signal block] | | | | | | |
| Crystal oscillator frequency | f_{OSC} | Crystal oscillator mode | 1 | | 8 | MHz |
| Low level pin voltage | V_{OSCL} | $I_{OSC} = -0.5$ mA | | 4.4 | | V |
| High level pin voltage | I_{OSCH} | $V_{OSC} = V_{OSCL} + 0.3$ V | | 0.5 | | mA |
| [External clock input block] | | | | | | |
| External input frequency | f_{CLK} | External clock mode | 500 | | 7000 | Hz |
| Input high level voltage | V_{IH} (CLK) | | 3.5 | | V_{REG} | V |
| Input low level voltage | V_{IL} (CLK) | | 0 | | +1.5 | V |
| Input open voltage | V_{IO} (CLK) | | 3.5 | 4.0 | 4.7 | V |
| Hysteresis | V_{IS} (CLK) | | 0.27 | 0.4 | 0.53 | V |
| Input high level current | I_{IH} (CLK) | V (CLK) = V_{REG} | | 155 | 200 | μ A |
| Input low level current | I_{IL} (CLK) | V (CLK) = 0 V | -400 | -300 | | μ A |
| [N1 pin] | | | | | | |
| Input high level voltage | V_{IH} (N1) | | 3.5 | | V_{REG} | V |
| Input low level voltage | V_{IL} (N1) | | 0 | | +1.5 | V |
| Input open voltage | V_{IO} (N1) | | 3.5 | 4.0 | 4.7 | V |
| Input high level current | I_{IH} (N1) | V (N1) = V_{REG} | | 155 | 200 | μ A |
| Input low level current | I_{IL} (N1) | V (N1) = 0 V | -400 | -300 | | μ A |
| [N2 pin] | | | | | | |
| Input high level voltage | V_{IH} (N2) | | 4.0 | | V_{REG} | V |
| Input middle level voltage | V_{IM} (N2) | | 2.0 | | 3.0 | V |
| Input low level voltage | V_{IL} (N2) | | 0 | | +1.0 | V |
| Input open voltage | V_{IO} (N2) | | 3.5 | 4.0 | 4.7 | V |
| Input high level current | I_{IH} (N2) | V (N2) = V_{REG} | | 155 | 200 | μ A |
| Input low level current | I_{IL} (N2) | V (N2) = 0 V | -400 | -300 | | μ A |
| [S/S pin] | | | | | | |
| Input high level voltage | V_{IH} (S/S) | | 3.5 | | V_{REG} | V |
| Input low level voltage | V_{IL} (S/S) | | 0 | | +1.5 | V |
| Input open voltage | V_{IO} (S/S) | | 3.5 | 4.0 | 4.7 | V |
| Hysteresis | V_{IS} (S/S) | | 0.27 | 0.4 | 0.53 | V |
| Input high level current | I_{IH} (S/S) | V (S/S) = V_{REG} | | 155 | 200 | μ A |
| Input low level current | I_{IL} (S/S) | V (S/S) = 0 V | -400 | -300 | | μ A |

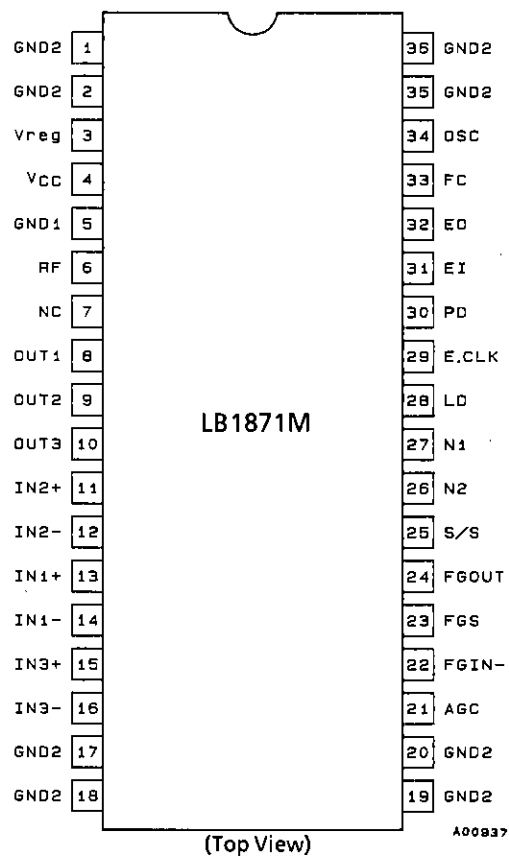
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Pin Assignment



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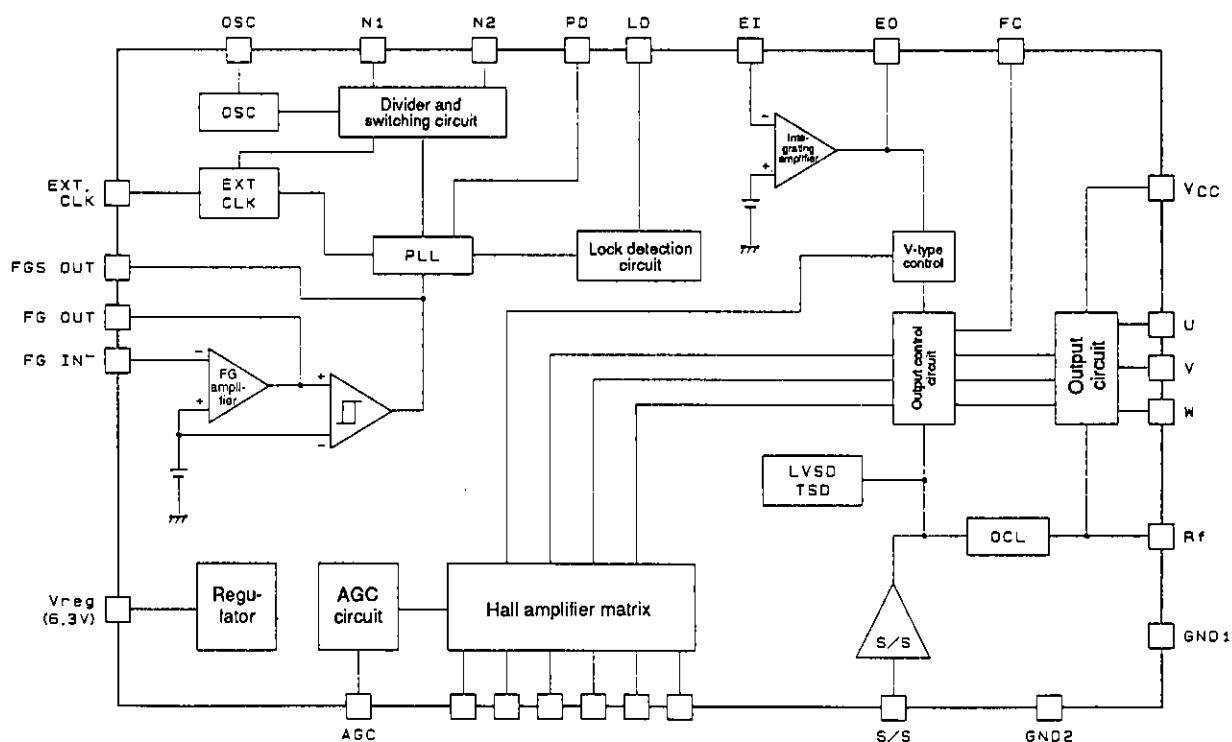
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Pin Functions

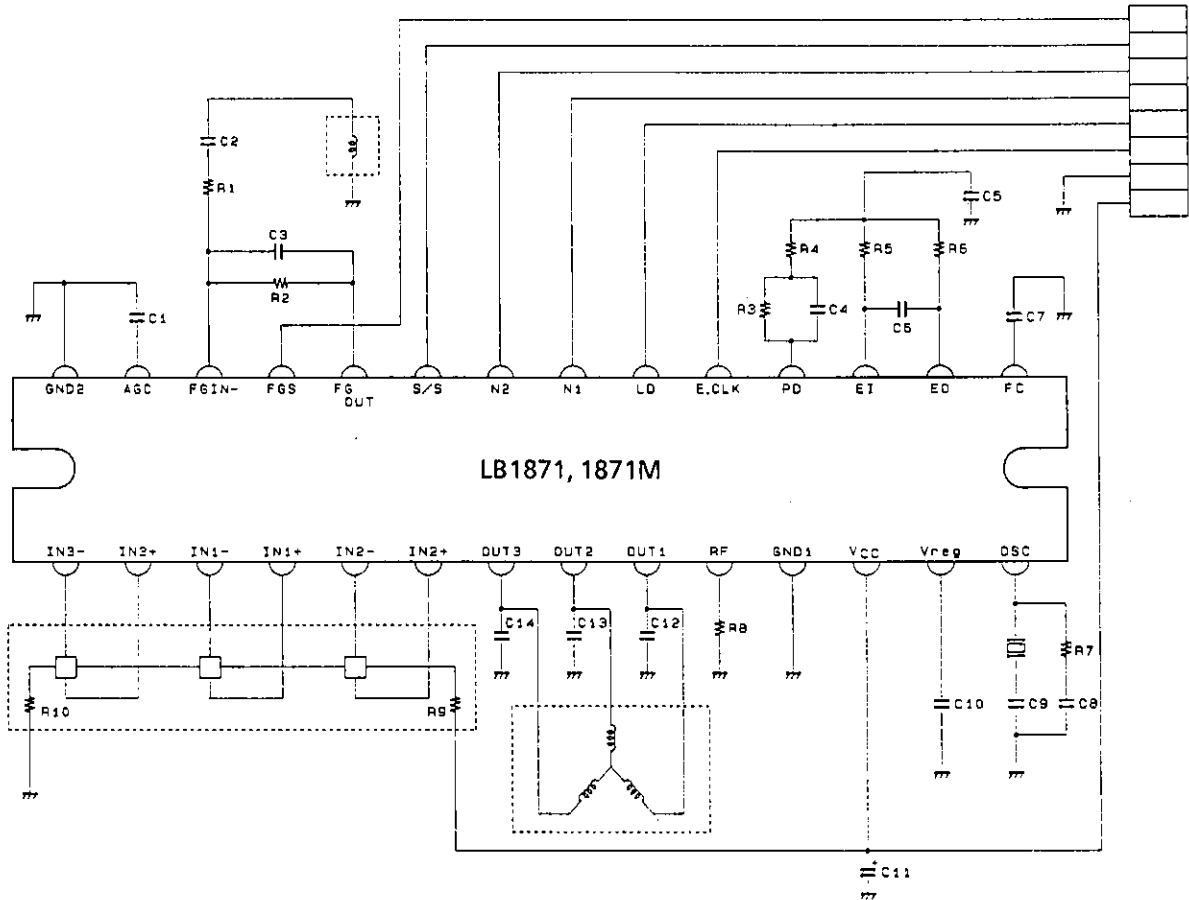
| Symbol | Function | Notes |
|-------------------------|--|---|
| IN1 to 3+, IN1 to 3- | Hall element input | Taken as high when $IN^+ > IN^-$, and as low otherwise. |
| OUT1 to 3 | Outputs | Capacitors are inserted between these pins and ground. |
| GND1 | Sub-ground | Output block ground. Connect to GND2. |
| GND2 | Ground | Ground for circuits other than the output block. |
| R_f | Output current detection | Connect a small resistor between this pin and ground. Set the maximum output current so that $I_{OUT} = 0.58/R_f$. |
| V_{CC} | Power supply | |
| V_{REG} | Power supply stabilization output | Connect a capacitor between this pin and GND2. Internal circuit power supply stabilization. |
| OSC | Crystal oscillator | 8 MHz max |
| E. CLK | External clock | 7 kHz max |
| FC | Control amplifier frequency correction | Connect a capacitor between this pin and GND2. |
| EI | Error amplifier input | |
| EO | Error amplifier output | |
| LD | Phase lock detector output | On when the PLL phase is locked. This pin is an open collector output. |
| PD | Phase comparator output | PLL phase comparator output |
| N1, N2 | Divisor switching | |
| S/S | Start/stop | Start on low. Stop on high or open. |
| FGS | FG pulse output | Pulse output following the FG Schmitt comparator. This pin is an open-collector output. |
| FG OUT | FG amplifier output | A minimum amplitude of 400 mVp-p is required. |
| FG IN- | FG amplifier input | |
| AGC | AGC amplifier frequency characteristics correction | Connect a capacitor between this pin and GND2. |

Equivalent Circuit Block Diagram



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Sample Application Circuit



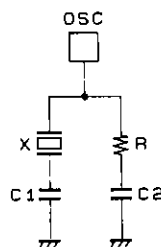
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Clock Divisor Switching

| Pin N1 | Pin N2 | Divisor |
|--------|--------|----------------------|
| H | H | 5120 (5 × 1 × 1024) |
| L | H | 10240 (5 × 2 × 1024) |
| H | L | 8192 (4 × 2 × 1024) |
| L | L | 6144 (3 × 2 × 1024) |
| — | M | EXT. CLK |

Note: An open input is taken as a high level input.

$$\text{PLL servo frequency} = (\text{crystal oscillator frequency}) / (\text{divisor})$$



A00935

Crystal Oscillator Usage

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External Component Values (reference values)

| Crystal (MHz) | C1 (pF) | C2 (pF) | R (kΩ) |
|---------------|---------|---------|--------|
| 3 to 4 | 39 | 82 | 0.82 |
| 4 to 5 | 39 | 82 | 1.0 |
| 5 to 7 | 39 | 47 | 1.5 |
| 7 to 10 | 39 | 27 | 2.0 |

Note: Use a crystal that has a ratio of at least 1:5 between the fundamental f0 impedance and the 3f0 impedance.

Three Phase Logic Truth Table

| H1 | H2 | H3 | OUT1 | OUT2 | OUT3 |
|----|----|----|------|------|------|
| H | L | H | L | H | M |
| H | L | L | L | M | H |
| H | H | L | M | L | H |
| L | H | L | H | L | M |
| L | H | H | H | M | L |
| L | L | H | M | H | L |

Columns H1 to H3

H: H+ > H-

L: H+ < H-

Columns OUT1 to OUT3

H: Source

L: Sink

LB1871 Functional Description and External Components

1. Speed control circuit

This IC provides high-precision stable motor control with minimal jitter by adopting a PLL speed control scheme. This PLL circuit compares the rising edge of the CLK signal with the falling edge of the FG Schmitt output and outputs that phase error.

When an internal clock is used, the FG servo frequency is determined by the formula shown below. Thus the motor speed is determined by the number of FG pulses and the crystal oscillator frequency.

$$f_{FG(\text{servo})} = f_{OSC}/N$$

f_{OSC} : Crystal oscillator frequency
 N: Clock divisor

2. Three-phase full-wave current linear drive

This IC adopts a three-phase full-wave current linear drive to hold motor noise to an absolute minimum. When switching the output transistor phase, it creates a two-phase excitation state, suppresses kickback, and smooths the output waveform. This suppresses motor noise. Note that since oscillation may occur with some motors, the capacitors C12, C13, and C14 (about 0.1 μF) are connected between the OUT pins and ground.

3. Current limiter circuit

The current limiter circuit limits the current (i.e., the peak current) to a level determined by the formula $I = 0.58/R_f$. A scheme in which the output stage drive current is limited is adopted for the limiting operation. Therefore, the phase compensation capacitor C7 (about 0.1 μF) is inserted between FC and ground.

4. Grounding

GND1 (pin 11 in the LB1871, pin 5 in the LB1871M)Output block ground (sub-ground)

GND2 (pin 28 in the LB1871, pins 1, 2, 17 to 20, 35, and 36 in the LB1871M)..Control circuit ground.

GND1 and GND2 should be connected on the circuit board by the shortest distance that occurs in the pattern. Also, the R_f resistor R8 ground node and the GND1 and GND2 pattern line should be grounded to a single point on the connector.

5. External interface pins

- LD pin
Output type: open collector
Breakdown voltage: 30 V absolute maximum
Saturation voltage manufacturing variation reference value ($I_{LD} = 10 \text{ mA}$): 0.10 to 0.15 V
- FGS pin
Output type: open collector
Breakdown voltage: 30 V absolute maximum
Saturation voltage manufacturing variation reference value ($I_{FGS} = 4 \text{ mA}$): 0.15 to 0.30 V
A hysteresis comparator converts the FG amplifier output to a pulse signal to create the FGS output, which is used for speed monitoring. The pull-up resistor is not required if this pin is not used.
- S/S pin (start/stop pin)
Input type: A pnp transistor whose base is pulled up to the internal 6.3 V power supply through a 23 k Ω resistor, and is pulled down to ground through a 40 k Ω resistor.
Threshold level (low \rightarrow high): about 2.8 V
Threshold level (high \rightarrow low): about 2.4 V
The LB1871 goes to stop mode with this pin in the open state.
- CLK input pin
Input type: A pnp transistor whose base is pulled up to the internal 6.3 V power supply through a 23 k Ω resistor, and is pulled down to ground through a 40 k Ω resistor.
Threshold level (low \rightarrow high): about 2.8 V
Threshold level (high \rightarrow low): about 2.4 V
- N1 pin
Input type: A pnp transistor whose base is pulled up to the internal 6.3 V power supply through a 23 k Ω resistor, and is pulled down to ground through a 40 k Ω resistor.
Threshold level (typical): about 2.6 V
- N2 pin
Input type: The base of a pnp transistor is pulled up to the internal 6.3 V power supply through a 23 k Ω resistor, and is pulled down to ground through a 40 k Ω resistor.
Threshold level (low \rightarrow high): about 1.5 V
Threshold level (high \rightarrow low): about 3.6 V

6. FG amplifier

R1 and R2 determine the FG amplifier gain, with the DC gain G being $R2/R1$. C2 and C3 determine the FG amplifier frequency characteristics, with R1 and C2 forming a high-pass filter and R2 and C3 forming a low-pass filter. Since a Schmitt comparator follows the FG amplifier directly, R1, R2, C2, and C3 must be chosen so that the FG amplifier output is at least 400 mVp-p. (It is desirable for the FG amplifier output to be set up to be between 1 and 3 V during steady state rotation.) The FG amplifier is often the cause when capacity becomes a problem in noise evaluation. One solution to that problem is to insert a capacitor of between 1000 pF and 0.1 μF between FG OUT pin and ground.

7. External capacitors

- C1
C1 is the AGC (automatic gain control) pin smoothing capacitor. This pin is an automatic gain control pin for holding the hall amplifier output amplitude fixed. This pin outputs the three-phase hall signal envelope, and is smoothed with a capacitor (about 0.1 μF) since it has ripple. When the hall input amplitude is small, the AGC pin potential will rise, and when the input amplitude is large, the AGC pin potential will fall.
 - C10
C10 is required for fixed voltage power supply stability. Since the output from the 6.3 V fixed voltage power supply is supplied to all circuits within the IC, noise on this signal must be avoided. This power supply must be adequately stabilized so that malfunctions due to noise do not occur.
 - C11
C11 is required for V_{CC} stabilization. Since, just as with C10, noise must be avoided, this capacitor is provided to adequately stabilize the power supply. The length of the pattern lines used to connect capacitors C1, C10, and C11 between their respective pins and GND2 must be kept as short as possible. C10 and C11 require special care, since the pattern line length can easily influence their characteristics.
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8. Oscillator pin

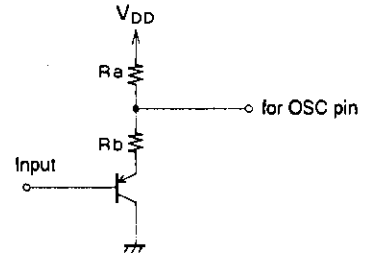
A crystal oscillator and an RC circuit is connected to the LB1871's OSC pin. To avoid problems when selecting the oscillator and the capacitor and resistor values, confirm these values with the oscillator's manufacturer. The pnp transistor and resistor circuit shown in the figure can be used to apply an external signal (of a few MHz) to the OSC pin.

$f_{in} = 1$ to 8 MHz

Input signal level: High level voltage: 4.0 V minimum

Low level voltage: 1.5 V maximum

It will be necessary to insert a capacitor of a certain size if there is overshoot or undershoot in the input waveform. Contact your Sanyo representative for more information on this point if necessary.



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| | | |
|--------------------------------------|------------------------|------------------------|
| $V_{DD} = 6.3$ V typ. (5.8 to 6.8 V) | $R_a = 4.7$ k Ω | $R_b = 1.3$ k Ω |
| $V_{DD} = 5.0$ V typ. (4.5 to 5.5 V) | $R_a = 2.0$ k Ω | $R_b = 1.0$ k Ω |

Use the LB1871 V_{REG} output for the $V_{DD} = 6.3$ V case.

9. IC internal power dissipation calculation example (calculated at $V_{CC} = 24$ V, standard ratings)

- Power dissipation due to current drain

$$P1 = V_{CC} \times I_{CC} = 24 \text{ V} \times 22 \text{ mA} = 0.53 \text{ W}$$

- Power dissipation when a -10 mA load current is drawn from the 6.3 V fixed voltage power supply.

$$P2 = (V_{CC} - V_{REG}) \times I_{load} = 17.7 \text{ V} \times 10 \text{ mA} = 0.18 \text{ W}$$

- Power dissipation due to the output drive current

(When $I_O = 0.1$ A, the inter-coil voltage $V_{Rm} = R_m \times I_O$, and the reverse voltage = 15 V)

$$P3 = (I_O/100) \times [(V_{CC} - 0.7 \text{ V}) + ((V_{CC} - V_{Rm})/2) - 0.7 \text{ V}] + V_{CC}^2/16 \text{ k}\Omega$$

$$= 1 \text{ mA} \times (23.3 \text{ V} + 3.8 \text{ V}) + 24 \text{ V}^2/16 \text{ k}\Omega = 0.06 \text{ W}$$

- Power dissipation due to the output transistor

(When $I_O = 0.1$ A, the inter-coil voltage $V_{Rm} = R_m \times I_O$, and the reverse voltage = 15 V)

$$P4 = (V_{CC} - V_{Rm}) \times I_O = 9 \text{ V} \times 0.1 \text{ A} = 0.9 \text{ W}$$

Therefore, the IC's total power dissipation is:

In stop mode:

$$P = P1 + P2 = 0.71 \text{ W}$$

In start mode (When $I_O = 0.1$ A, the inter-coil voltage $V_{Rm} = R_m \times I_O$, and the reverse voltage = 15 V)

$$P = P1 + P2 + P3 + P4 = 1.67 \text{ W}$$

10. Measuring the IC's temperature rise

- Thermocouple measurement

When using a thermocouple for temperature measurement, attach the thermocouple to a heat sink fin. This temperature measurement technique is straightforward. However, a large measurement error occurs when the heat generation is not in a steady state.

- Measurement using IC internal diode characteristics

We recommend using the parasitic diode that exists between LD and ground in this IC. Remove the external resistor when measuring. (Sanyo data indicates that $I_{LD} = -1 \text{ mA}$, about $-1.9 \text{ mV}/^\circ\text{C}$, when the LD pin is high.)

11. Servo constants

The servo constant calculation varies significantly with the motor used, and requires specialized know-how. Thus this should be handled by the motor manufacturer. Sanyo can provide the required IC characteristics data for servo constant calculation, and the motor manufacture should provide the frequency characteristics simulation data for the specified filter characteristics.

