Ordering number : EN5625A

Monolithic Digital IC

LB1872

Polygon Mirror Scanner Driver IC

Overview

The LB1872 is a 3-phase brushless motor driver IC developed for driving the polygon mirror motor used in laser printers and similar products.

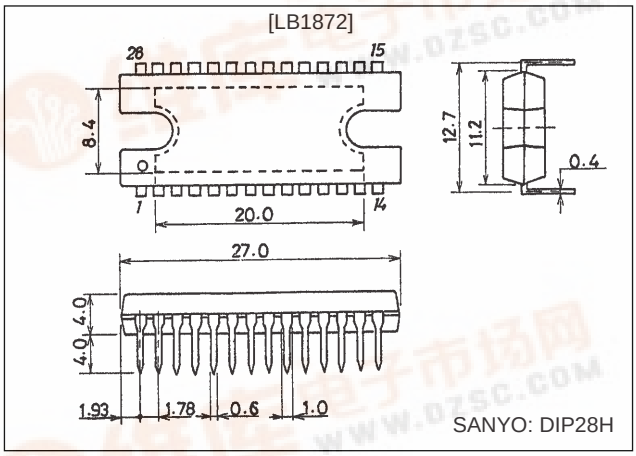
Functions and Features

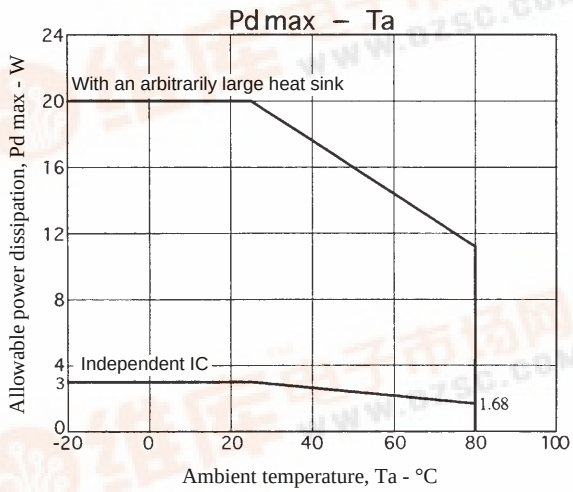
- Integrates the circuits (speed control and driver circuits) required for laser printer polygon mirror motor drive in a single chip.
- Uses a current linear drive technique for minimal motor noise. Only a small capacitors are required for output oscillation prevention.
- PLL speed control adopted for high-precision rotation with excellent jitter characteristics.
- Phase lock detection output with a chattering prevention function
- Four rotation rates can be set up using a single crystal oscillator to support 240, 300, 400, and 600 dpi operation.
- Arbitrary rotation rates can be acquired when an external clock is used.
- Deceleration function implemented by short-circuit braking (free running when stopped)
- Built-in FG and error amplifiers
- Full complement of protection circuits, including thermal protection, low voltage protection, and current limiter circuits, provided on chip.

Package Dimensions

unit: mm

3147B-DIP28H





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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		30	V
Maximum output current	I_O max	t ≤ 0.5s	2.0	A
Allowable power dissipation	Pd max1	Independent IC	3	W
	Pd max2	Arbitrarily large heat sink	20	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		10 to 28	V
5.0-V fixed-voltage output current	I_{REG}		0 to –15	mA
LD pin voltage	V_{LD}		0 to 28	V
FGS pin voltage	V_{FGS}		0 to 28	V
LD pin output current	I_{LD}		0 to 10	mA
FGS pin output current	I_{FGS}		0 to 5	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 24 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	In stop mode		20	27	mA
[Output Saturation Voltage] V_{AGC} = 2 V						
Source	V(sat)1-1	I_O = 0.7 A, R_F = 0 Ω		1.5	1.9	V
	V(sat)1-2	I_O = 1.5 A, R_F = 0 Ω		1.8	2.2	V
Sink	V(sat)2-1	I_O = 0.7 A, R_F = 0 Ω		0.3	0.5	V
	V(sat)2-2	I_O = 1.5 A, R_F = 0 Ω		0.7	1.0	V
Output leakage current	I_O (leak)	V_{CC} = 28 V			100	μA
[5-V Fixed-Voltage Output]						
Output voltage	V_{REG}		4.65	5.0	5.35	V
Voltage regulation	$\Delta V_{REG}1$	V_{CC} = 10 to 28 V		40	100	mV
Load regulation	$\Delta V_{REG}2$	I_O = 0 to 10 mA		20	100	mV
Temperature coefficient	$\Delta V_{REG}3$	Design target value		0		mV/°C
[Hall Input Block]						
Input bias current	$I_{B(HA)}$	V_{AGC} = 3 V		2	10	μA
Differential-mode input range	V_{HIN}	With a sine wave input	50		350	mV
Common-mode input range	V_{ICM}	Differential input: 50 mV p-p	3.5		V_{CC} – 3.5	V
Input offset voltage	V_{IOH}	Design target value	–20		+20	mV
[Low Voltage Protection Circuit]						
Operating voltage	V_{SD}		8.4	8.8	9.2	V
Hysteresis	ΔV_{SD}		0.2	0.4	0.6	V
[Thermal Protection Circuit]						
Shutdown temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis	ΔTSD	Design target value (junction temperature)		40		°C
[FG Amplifier]						
Input offset voltage	$V_{IO(FG)}$	Design target value	–10		+10	mV
Input bias current	$I_{B(FG)}$		–1		+1	μA
DC bias level	$V_{B(FG)}$		–5%	1/2V_{REG}	+5%	V
Output high-level voltage	$V_{OH(FG)}$	I_{OH} = –500 μA	V_{REG} – 1.2	V_{REG} – 0.8		V
Output low-level voltage	$V_{OL(FG)}$	I_{OL} = 500 μA		0.8	1.2	V
[FG Schmitt Input Block]						
Input hysteresis (high to low)	V_{SHL}			0		mV
Input hysteresis (low to high)	V_{SLH}			150		mV
Hysteresis	V_{FGL}		100	150	200	mV
Input operating level	V_{FGSIL}		400			mV

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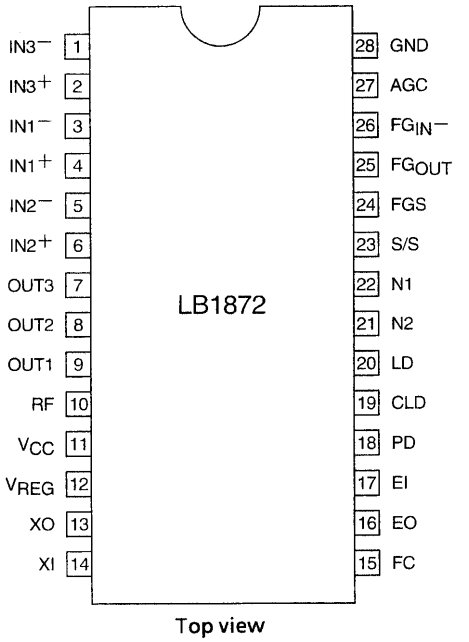
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output saturation voltage	$V_{FGS(sat)}$	I_{FGS} = 3 mA		0.2	0.4	V
Output leakage current	$I_{L(FGS)}$	V_{CC} = 28 V			10	μA
[Error Amplifier]						
Input offset voltage	$V_{IO(ER)}$	Design target value	–10		+10	mV
Input bias current	$I_{B(ER)}$		–1		+1	μA
DC bias level	$V_{B(ER)}$		–5%	$1/2V_{REG}$	+5%	V
Output high-level voltage	$V_{OH(ER)}$	I_{OH} = –500 μA	V_{REG} – 1.2	V_{REG} – 0.8		V
Output low-level voltage	$V_{OL(ER)}$	I_{ERI} = 100 μA, I_{OL} = 500 μA	0.7	1.0	1.3	V
[Phase Comparator Output]						
Output high-level voltage	V_{PDH}	I_{OH} = –100 μA	V_{REG} – 0.2	V_{REG} – 0.1		V
Output low-level voltage	V_{PDL}	I_{OL} = 100 μA		0.1	0.2	V
Output source current	I_{PD}+	$V_{PD} = V_{REG}/2$			–0.6	mA
Output sink current	I_{PD}–	$V_{PD} = V_{REG}/2$	1.5			mA
[Lock Detection Output]						
Output saturation voltage	$V_{LD(sat)}$	I_{LD} = 5 mA		0.1	0.4	V
Output leakage current	I_{LDLEAK}	V_{CC} = 28 V			10	μA
[Drive Block]						
Output idling voltage	V_{ID}				6	mV
Forward gain	$G_{DF}1$	When the phase is locked	0.4	0.5	0.6	
	$G_{DF}2$	When unlocked	2.4	3.0	3.6	
Current limiter	V_L	Rf = 2 Ω	0.45	0.5	0.55	V
Brake command voltage	V_{BRK}			2.3		V
[Reference Signal Block]						
Crystal oscillator frequency	f_{OSC}	In crystal oscillator mode	1		10	MHz
Low-level pin voltage	V_{OSCL}	I_{OSC} = –0.5 mA		1.7		V
High-level pin voltage	I_{OSCH}	$V_{OSC} = V_{OSCL}$ + 0.3 V		0.5		mA
[N1 Pin]						
External input frequency	f_I(N1)	In external clock mode	100		10000	Hz
High-level input voltage	V_{IH}(N1)		3.5		V_{REG}	V
Low-level input voltage	V_{IL}(N1)		0		1.5	V
Input open voltage	V_{IO}(NI)		V_{REG} – 0.5		V_{REG}	V
Hysteresis	V_{IS}(N1)		0.3	0.4	0.5	V
High-level input current	I_{IH}(N1)	$V_N1 = V_{REG}$	–10	0	+10	μA
Low-level input current	I_{IL}(N1)	V_N1 = 0 V	–350	–275		μA
[N2 Pin]						
High-level input voltage	V_{IH}(N2)		4.0		V_{REG}	V
Middle-level input voltage	V_{IM}(N2)		2.0		3.0	V
Low-level input voltage	V_{IL}(N2)		0		1.0	V
Input open voltage	V_{IO}(N2)		2.2	2.5	2.8	V
High-level input current	I_{IH}(N2)	$V_N2 = V_{REG}$		200	270	μA
Low-level input current	I_{IL}(N2)	V_N2 = 0 V	–270	–200		μA
[S/S Pin]						
High-level input voltage	V_{IH}(SS)		3.5		V_{REG}	V
Low-level input voltage	V_{IL}(SS)		0		1.5	V
Input open voltage	V_{IO}(SS)		V_{REG} – 0.5		V_{REG}	V
Hysteresis	V_{IS}(SS)		0.3	0.4	0.5	V
High-level input current	I_{IH}(SS)	VS/S = V_{REG}	–10	0	+10	μA
Low-level input current	I_{IL}(SS)	VS/S = 0 V	–350	–275		μA
[CLD Pin]						
Charge current	$I_{CLD}1$	V_{CLD} = 0 V (Phase locked)	–9	–7	–5	μA
Discharge current	$I_{CLD}2$	$V_{CL} = V_{REG}/2$ (Phase unlocked)	1			mA

Pin Assignment



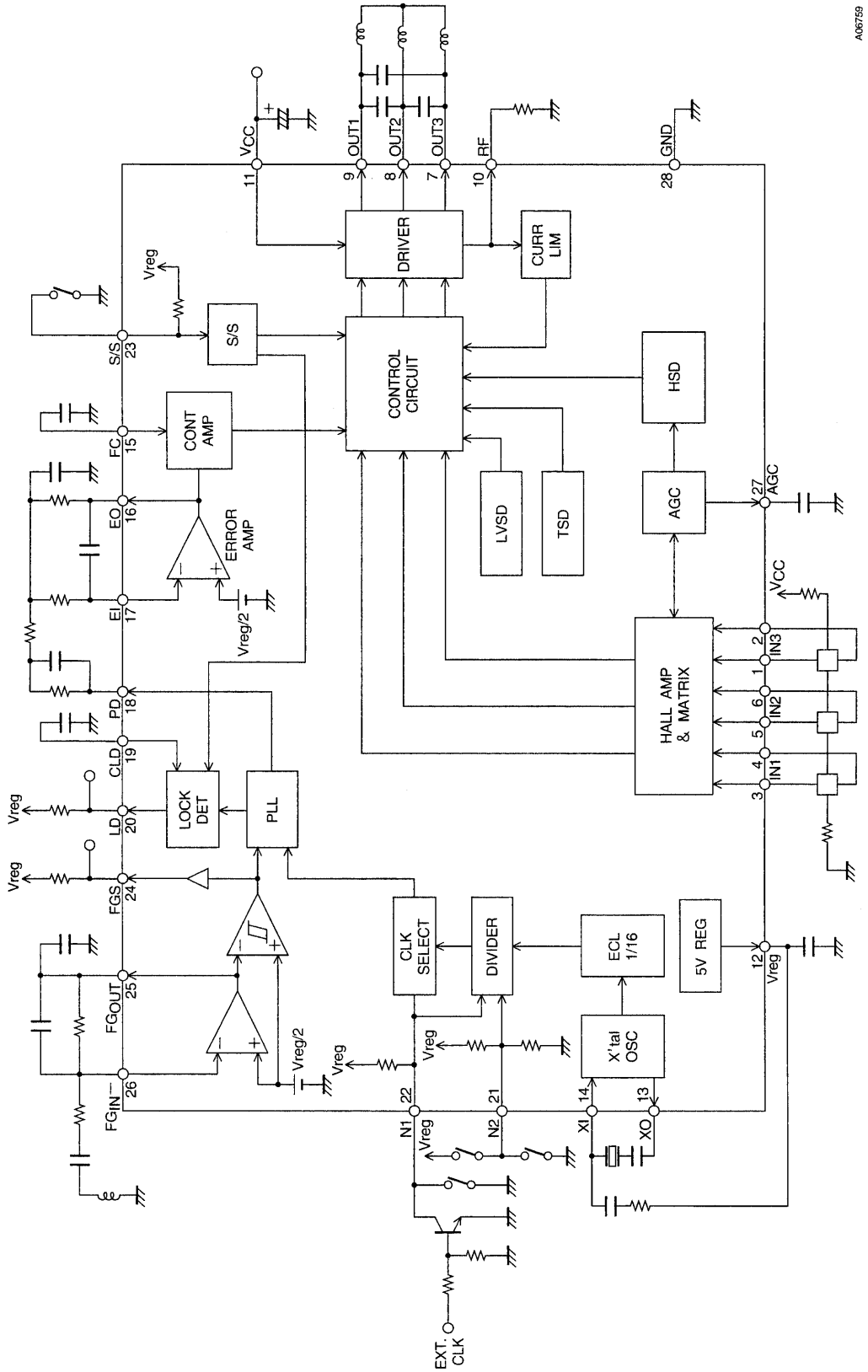
Clock Divisor Switching

N1	N2	Divisor
H	H	2048 (4 × 1 × 512)
H	L	4096 (4 × 2 × 512)
L	H	5120 (5 × 2 × 512)
L	L	3072 (3 × 2 × 512)
CLK IN	M or open	EXT. CLK

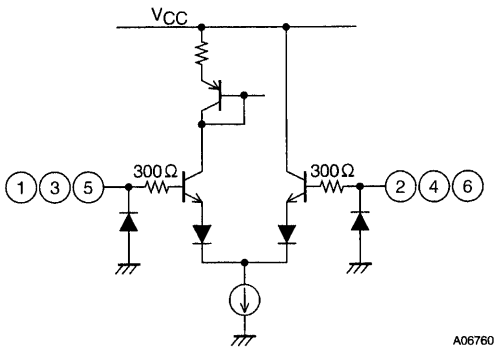
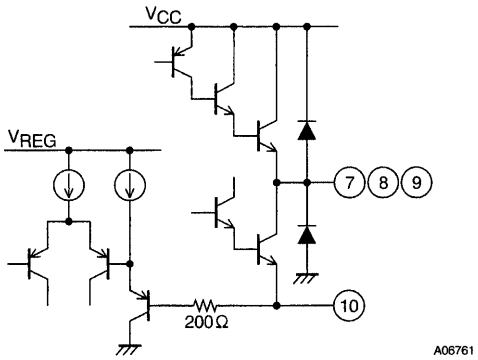
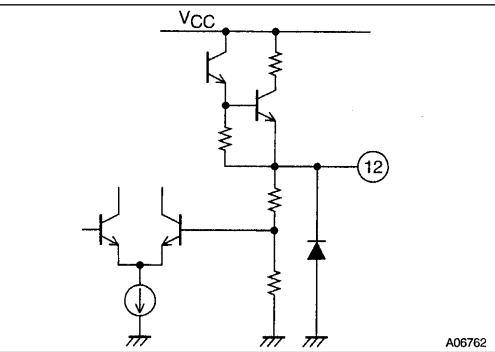
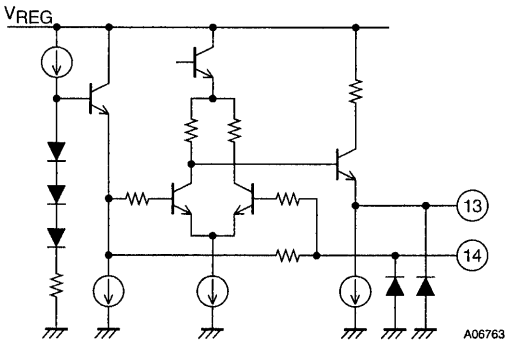
Three-Phase Logic Truth Table

H1	H2	H3	OUT1	OUT2	OUT3
H	L	H	L	H	M
H	L	L	L	M	H
H	H	L	M	L	H
L	H	L	H	L	M
L	H	H	H	M	L
L	L	H	M	H	L

Equivalent Circuit Block Diagram



Pin Functions

Pin No.	Symbol	Pin function	Equivalent circuit
1 2 3 4 5 6	$IN3^-$ $IN3^+$ $IN1^-$ $IN1^+$ $IN2^-$ $IN2^+$	Hall amplifier inputs $IN^+ > IN^-$ is the input high state, and the reverse is the input low state. Connect a capacitor between the IN^+ and IN^- inputs if there is noise in the Hall sensor signals. An amplitude of over 50 mV p-p and under 350 mV p-p is desirable in the Hall sensor signals. Kickback may occur in the output if the input signal has an amplitude greater than 350 mV p-p.	
7 8 9	OUT3 OUT2 OUT1	Motor drive outputs Connect capacitors between the motor outputs (or between the motor outputs and ground) if oscillation occurs in the outputs. (Use capacitors in the range 0.1 µF to 0.47 µF.)	
10	RF	Output current detection Connect a resistor (Rf) between this pin and ground. The output current is limited to be up to $I_{OUT} = V_{REG}/Rf$.	
11	V_{CC}	Power supply	
12	V_{REG}	Stabilized power supply output (5-V output) Connect a capacitor (about 0.1 µF) between this pin and ground for stabilization.	
13 14	XO XI	Crystal oscillator connections These pins are used to drive the reference clock oscillator element. If an external clock (with a frequency of a few MHz) is used, connect a resistor (about 13 kΩ) to the XI pin in series and input the clock signal through that resistor. Leave the XO pin open in this case.	

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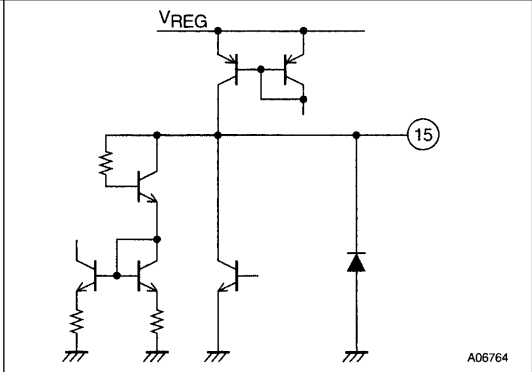
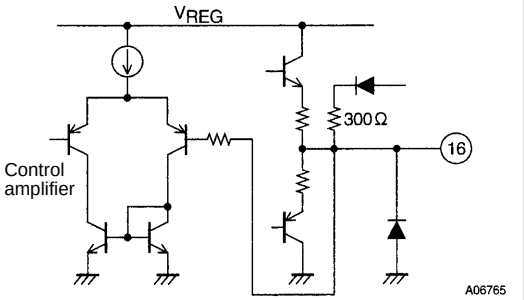
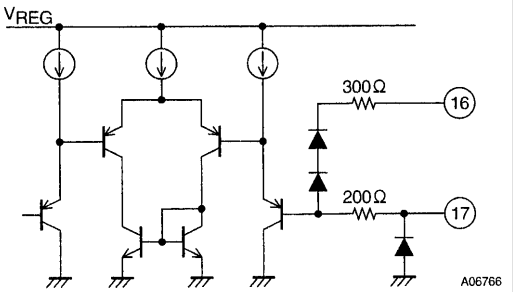
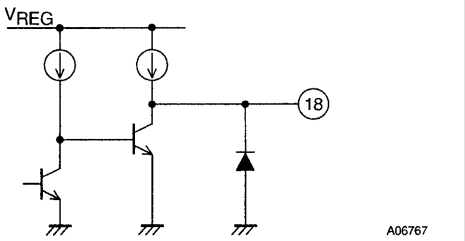
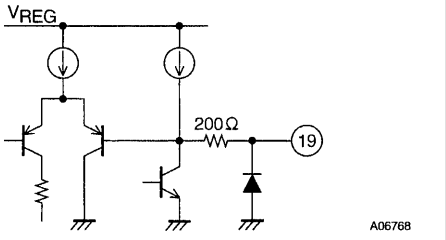
Pin No.	Symbol	Pin function	Equivalent circuit
15	FC	Control amplifier frequency correction Current limiter system closed loop oscillation can be prevented by inserting a capacitor (about 0.022 to 0.47 µF) between this pin and ground. If the capacitance of this capacitor is too large, the output current response characteristics may be degraded.	
16	EO	Error amplifier output When high, the output current is increased.	
17	EI	Error amplifier input	
18	PD	Phase comparator output (PLL output) The phase error is output as changes in the duty of a pulse waveform. The output current is increased as the duty becomes smaller.	
19	CLD	LD output mask time setting Chattering can be masked by inserting a capacitor (about 0.1 to 0.47 µF) between this pin and ground. The startup time may be increased if only masking is used and the servo constants are not re-optimized.	

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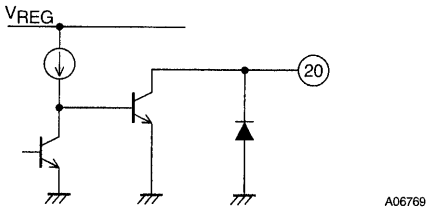
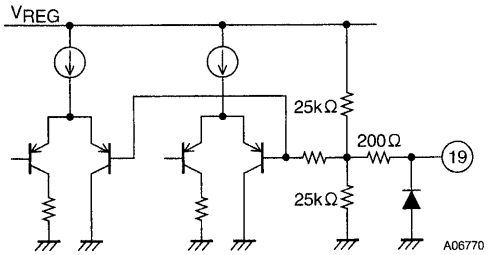
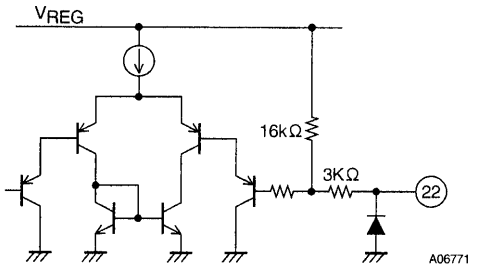
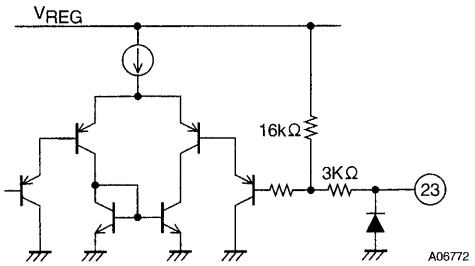
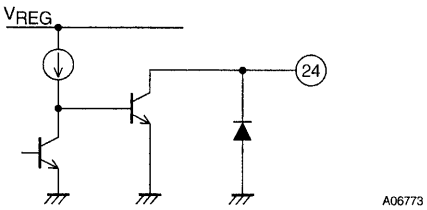
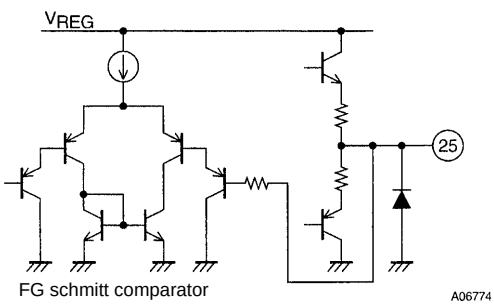
Pin No.	Symbol	Pin function	Equivalent circuit
20	LD	Phase lock detector output This pin goes to the on state when the PLL phase is locked. This is an open collector output.	
21	N2	Divisor switch Low: 0 to 1.0 V Middle: 2.0 to 3.0 V High: 4.0 V to V_{REG} This pin goes to the middle level when open.	
22	N1	Divisor switch and external clock input Low: 0 to 1.5 V High: 3.5 V to V_{REG} This pin functions as the external clock input pin when N2 is at the middle level. This pin goes to the high level when open.	
23	S/S	Start/stop control Low: Start High: Stop This pin goes to the high level when open.	
24	FGS	FG pulse-converted output This pin outputs the post-hysteresis comparator FG signal. This is an open collector output.	
25	FG_{OUT}	FG amplifier output If noise in the FG signal is a problem, e.g. if discharge noise is detected, insert a capacitor (about 0.01 to 0.1 µF) between this pin and ground.	

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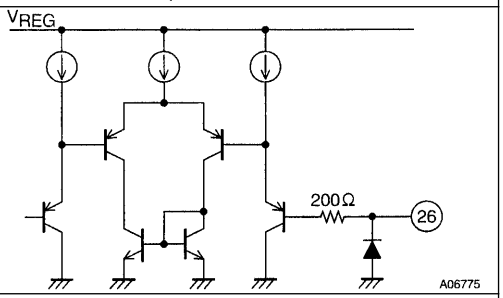
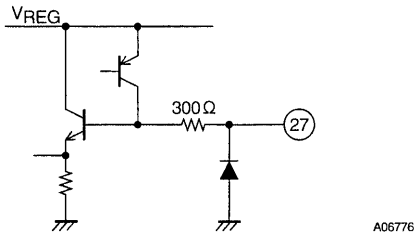
Pin No.	Symbol	Pin function	Equivalent circuit
26	$FG_{IN}-$	FG amplifier input	
27	AGC	AGC amplifier frequency characteristics correction Insert a capacitor (about 0.1 μF) between this pin and ground.	
28	GND	Ground	

LB1872 Functional Description

1. Speed control circuit

   Since this IC adopts a PLL speed control circuit, it can provide high-precision, jitter-free, and stable motor operation. This PLL circuit compares the phases of the CLK (external clock) rising edge and the FG Schmitt output rising edge and uses the error output from that comparison for control.

   If an internal clock system is used, the FG servo frequency is determined by the following formula. Therefore, the motor speed can be set by setting the number of FG pulses and the crystal oscillator frequency.

   $f_{FG}(servo) = f_{OSC}/N$

   f_{OSC}: Crystal oscillator frequency

   N: Clock divisor (See the separately provided table.)

   If an external clock (input to the N1 pin) is used, the IC controls the motor speed by holding the FG servo frequency identical to the external clock frequency.

2. Output drive circuit

   To suppress motor noise as much as possible, this IC adopts a three-phase full wave current linear drive technique. Also, it adopts a midpoint control technique to prevent ASO destruction of the output transistors.

   This IC uses short-circuit braking (lower side output) for motor deceleration during speed switching and lock pull in. In stop mode, the output is turned off.

   If a motor with a coil resistance (interphase) of 10 Ω or lower is used, diodes (rectifying) may be inserted between the outputs and ground (for all outputs) and current limitation may also be applied during braking to prevent excessive braking currents. Although this is disadvantageous from an ASO standpoint, since states with a large back EMF are states with a high switching frequency and the amount of time during which loads are applied to the transistors will be shorter, ASO problems will not be particular severe.

3. Current limiter circuit

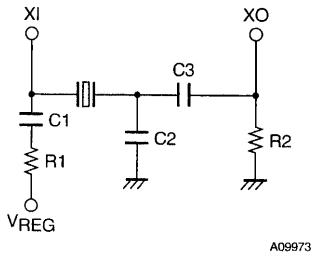
   The current limiter circuit is a peak current limiter whose limit current is determined by $I = V_{RF}/Rf$ (where VRF = 0.5 V (typical) and Rf is the current detection resistor).

4. Reference clock

Any one of the following three techniques can be used to input the reference clock used for speed control.

• Crystal oscillator generated clock

Use the following circuit, consisting of a crystal element, capacitors, and resistors, as a crystal oscillator circuit.



C1 and R1: Used for oscillator stabilization.
C3: Used for oscillator element coupling.
C2: Used for overtone prevention.
R2: Improves the oscillator margin.

Sample External Component Values

Oscillator frequency (MHz)	C1 (μF)	C2 (pF)	C3 (pF)	R1 (Ω)	R2 (Ω)
1 to 3	0.1	47	220	220 k	—
3 to 5	0.1	18	100	100 k	—
5 to 7	0.1	—	47	47 k	—
7 to 10	0.1	—	33	10 k	4.7 k

This circuit and these component values are only provided for reference purposes. Consult with the manufacturer of the crystal element concerning the influence of such factors as the characteristics of the crystal element itself and the stray capacitances due to the printed circuit board wiring pattern to assure that problems do not occur.

(Notes on printed circuit board wiring)

Since crystal oscillator circuits are high-frequency circuits, they are easily influenced by stray capacitances due to the printed circuit board wiring. Therefore, lines for external components must be kept as short as possible and lines must be made as narrow as possible. In this external circuit, the connection between the oscillator element and C3 (and C2) is particularly subject to influence by stray capacitance, and requires special care.

• External clock (crystal oscillator equivalent: a few MHz)

If a signal equivalent to a crystal oscillator signal is input from an external signal generator, input that signal through a series resistor of about 13 kΩ to the XI pin. Leave the XO pin open.

• External clock (FG frequency equivalent: a few kHz)

If a signal equivalent to the FG frequency is input from an external signal generator, set the N2 pin to the middle level (or open) and input that signal to the N1 pin. In this case, the motor will remain in the stopped state (short-circuit braking operation) even if a start input is applied when no clock is input. However, since IC heating due to the large output drive currents that flow in the short braking state (since the lower side transistors in all phases are driven) care is required if the braking state must be held for extended periods.

5. Hall input signals

Even if the amplitude of the Hall sensor input signals is changed by the motor, the influence on the output will be suppressed by the AGC circuit. However, if there are discrepancies between the amplitudes of the three phases, the output phase switching timing may be shifted.

The output current will be cut off by a protection circuit if a start signal is input when there are no signals applied to the Hall inputs.

The maximum operating frequency of the Hall inputs is affected by the saturation state of the outputs. While there are no problems for frequencies of under 1 kHz (the frequency in a single Hall phase), if a higher operating frequency is required, it can be advantageous if the outputs remain unsaturated. If the outputs remain in the unsaturated state, this IC can be used up to frequencies of about 2 kHz.

Since motors with higher speeds have higher operating frequencies, we recommend using motors with four motor magnet poles.

6. LD output

The LD output goes on when the phase is locked. Phase lock is determined not by the speed error but by the phase error only. Therefore, the speed error when the LD output is on, during, for example, lock pull-in, will change with the acceleration of the FD signal. (The speed error will be smaller for lower accelerations.) If it is necessary to

stipulate the speed error when the LD output is on, this must be determined based on the result of a speed measurement for the motor state.
This IC includes a built-in circuit that masks LD output chattering (rapid switching between on and off) during phase lock pull-in. The mask time is determined as shown below by the capacitance of the capacitor inserted between the CLD pin and ground.

$t = 0.35 \times C$
t: Mask time (s)
C: External capacitance (μF)

If LD chattering is masked, the LD output is delayed by the mask time. Therefore care is required, since the speed error when LD is on is changed by the mask time.
Leave the CLD pin open if there is no need for masking.

7. Power supply stabilization
Since this IC provides large output currents, it can easily cause fluctuations in the power supply line voltage. Therefore, capacitors with adequate capacitances for stabilization must be inserted between the V_{DD} and ground pins. If diodes are inserted in the power supply lines to prevent device destruction by reverse power supply connection, the power supply line voltage becomes especially liable to fluctuations. In this case, even larger capacitors are required.

8. External protection circuits
If an application will include external motor constraint protection and other external protection circuits, use an open collector transistor output to set the FC pin low to shut off the IC drive current.