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Monolithic Digital IC

LB1896

3-phase Brushless Motor Driver for **CD-ROM Spindle Drive Use**

Overview

The LB1896 is a 3-phase brushless motor driver IC that is ideal for driving CD-ROM spindle motors. DZSC.COM

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Functions and Features

- 120 ° voltage linear technique
- V-type control voltage
- · Switchable control gain
- · Control, noncontrol, acceleration/deceleration mode select pins built in.
- Start/Stop pin built in, Hall bias built in.

Package Dimensions

unit : mm

3219-QFP34H-C



Specifications

PDF

Absolute Maximum Ratings at $Ta = 25 \degree C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum aupply voltage	V _{CC} 1 max		20	V
Maximum supply voltage	V _{CC} 2 max		7.0	V
Applied output voltage	V _{OU, V, W}		20	V
Output current	I _{OUT}		1.2	A
Allowable power dissipation	Pd max	Independent IC	0.77	W
Operating temperature	Topr	FB.	-20 to +75	°C
Storage temperature	Tstg	152 200	-55 to +150	°C

Operating Conditions at $Ta = 25 \circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} 1		5 to 18	V
Supply vollage	V _{CC} 2	$V_{CC}1 \ge V_{CC}2$	4.3 to 6.5	V
V _{Cref} input voltage	V _{Cref}		V _{CC} 2/2 ±1.0	V
V _{NS} input voltage	V _{NS}		0 to V _{CC} 2 –1.0	V



Electrical Characteristics at Ta = 25 °C, $V_{\rm CC}1$ = 12 V, $V_{\rm CC}2$ = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current 1	I _{CC} 1	V_{C} = open, V_{Cref} = open, R_{L} = ∞ , $V_{S/S}$ = 5 V		17	30	mA
Supply current 2	I _{CC} 2	V_{C} = open, V_{Cref} = open		7.5	10.5	mA
Supply current 3	I _{CC} 3	V_{C} = open, V_{Cref} = open, R_{L} = ∞ , $V_{S/S}$ = 0 V, (I _{CC} of V _{CC} 1)		0.9	3	mA
[Drive block]				1		
Output acturation upthana	V _{O(sat)} 1	I _{OUT} = 0.4 A, sink + source		1.6	2.2	V
Output saturation voltage	V _{O(sat)} 2	I _{OUT} = 0.8 A, sink + source		2.0	3.0	V
Output TRS sustaining voltage	V _{O(sus)}	I _{OUT} = 20 mA	20			V
Output static voltage	V _{OQ}	V _C = 2.5 V, V _{Cref} = 2.5 V	5.7	6.0	6.3	V
Hall amplifier input offset voltage	V _{H offset}		-5		+5	mV
Hall amplifier input bias current	I _{H bias}			1	5	μA
Hall amplifier common-mode input	Maria		1.2		2.2	V
voltage range	V Hch		1.5		2.2	v
Hall input/output voltage gain	G _{VHO}		40	43	46	dB
Control/output drive gain 1	G _{VCO} 1	RZ1 = RZ2, GC1 = L, GC2 = L	26	29		dB
Control/output channel difference 1	ΔG_{VCO} 1	RZ1 = RZ2, GC1 = L, GC2 = L	-1.5		+1.5	dB
Control/output drive gain 2	G _{VCO} 2	RZ1 = RZ2, GC1 = L, GC2 = H	32	35		dB
Control/output channel difference 2	ΔG_{VCO}^2	RZ1 = RZ2, GC1 = L, GC2 = H	-1.9		+1.9	dB
Input dead zone voltage	V _{DZ}	RZ1 = RZ2, GC1 = L, GC2 = L V _O (voltage between out and out) = 0.1 V	±13	±38	±55	mV
Input bias current 1	IB SERVO	V _C = 1.0 V			500	nA
Input bias current 2	I _{B n.s}	V _{NS} = 1.0 V			500	nA
S/S pin high voltage	V _{S/S H}	Input is CMOS level	4			V
S/S pin low voltage	V _{S/S L}	Note) S/S pin Vth = $V_{CC}2/2$			1	V
Gain control 1 high voltage	V _{GC1 H}	Input is at CMOS level.	4			V
Gain control 1 low voltage	V _{GC1 L}	Note) GC1 pin Vth = 2.0 V			1	V
Gain control 2 high voltage	V _{GC2 H}	Input is at CMOS level.	4			V
Gain control 2 low voltage	V _{GC2 L}	Note) GC2 pin Vth = 2.0 V			1	V
S/S pin input current	I _{S/S}	Input voltage = 5 V		50	100	μA
Gain control 1, 2 current	I _{GC}	Input voltage = 5 V		53	110	μA
Rotation output saturation voltage	V _(sat) H.FG	$I_0 = -5 \text{ mA}$		0.24	0.5	V
Rotation output saturation sustaining voltage	V _(sus) H.FG				7	V
Hall bias voltage	V _H ±	$I_{O} = 5 \text{ mA}, R_{H} = 200 \Omega$	0.7	0.97	1.2	V
CTRL pin high voltage	V _{CTRL H}	Common for CTRL1 and CTRL2 input CMOS level	4			V
CTRL pin low voltage	V _{CTRL L}	Note) CTRL pin Vth = 2.5 V			1.0	V
CTRL input current	ICTRL	Input voltage = 5 V		53	110	μA
TSD operation voltage	TSD	Design target	150	180	210	°C
TSD hysteresis	ΔTSD	Design target		15		°C

Note) Vth is a design target and not measured.

Mode Switching Truth Table

CTRL0	CTRL1	Mode
L	L	Control
L	Н	Noncontrol
Н	L	Acceleration
Н	Н	Deceleration

L = 0 to 1.0 V

H = 4.0 V or more

Hall Logic Truth Table

		Hall input			E/P. Control	
	Source → Sink	U _{IN}	V _{IN}	W _{IN}	F/R Control	
1	$W \rightarrow V$	Ц	Ц		Forward	
	V o W	п	п		Reverse	
2	$W \rightarrow U$	Ц			Forward	
2	$U\toW$	п	L	L	Reverse	
2	$V \rightarrow W$				Forward	
3	$W \to V$	L			Reverse	
4	$U\toV$		ц		Forward	
4	$V \rightarrow U$	L		L	Reverse	
F	$V \rightarrow U$				Forward	
5	$U\toV$	н	L		Reverse	
C C	$U\toW$	L	н		Forward	
0	$W \rightarrow U$				Reverse	

An input is considered to be HIGH when $U_{IN}1>U_{IN}2$, $V_{IN}1>V_{IN}2$, and $W_{IN}1>W_{IN}2$ by 0.2 V or more. Forward when $V_C>V_{Cref}$ Reverse when $V_C<V_{Cref}$

Pin Assignment



Pin Functions

Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
3, 4	Frame			Frame GND.
20, 21	GND			GND must be shared.
2	GND			GND
23 22 19	Uout Vout Wout		OVCC1 (23) (19) (19) (19) (19) (19) (14490	Output pins. Motor connection
17	Rf		0VCC2	Output Tr GND. A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection.
18, 24	NC			Idle pins.
16	V _{CC} 2	4.3 to 6.5 V		 Power supply for blocks other than the output block. This supply should be kept stable to prevent ripple and noise from entering this pin.
15 14	Z1 Z2		OVCC2 OCC2 OCC2	 First-stage amplifier gain setting resistors. Z1 and Z2 normally range from several tens of kΩ to several hundreds of kΩ. The gain is about 6 dB.
13 12	V _C V _{Cref}	V _{CC} 2/2 ±1.0	VCC2 VCC2 VCC2 (3) (3) (12) (12) (12) (12) (12) (12) (12) (12	 V_C is the speed control pin. Forward when V_C > V_{Cref}. Reverse when V_C < V_{Cref}. V_C is used to control the output voltage. V_{Cref} determines the motor control stop voltage. V_{CC}2/2 in normal use.
11 10	GC1 GC2	0 to V _{CC} 2	VCC2 VCC2 VCC2 10(11) 10(11) A04494	 Input/output gain switching pins. GC1 is for first-stage amplifier Z1/Z2 switching. When GC1 is LOW, Z1 is selected; when HIGH, Z2 is selected. GC2 is for next-stage amplifier switching.

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9 CTRL6 0 to V _{CC} 2 • Operation mode switching pins. 8 CTRL1 0 to V _{CC} 2 • Operation mode switching Truth Ta To Ta To	Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
7 NS+ 0 to $V_{CC}^2 - 1 V$ Image: the put-output gain is 14 dB. (GC2: LOW) 6 S/S 0 to V_{CC}^2 Image: the put-output gain is 14 dB. (GC2: LOW) 6 S/S 0 to V_{CC}^2 Image: the put-output gain is 14 dB. (GC2: LOW) 6 S/S 0 to V_{CC}^2 Image: the put-output gain is HIGH, START; Image: the put-output gain is V_{CC}^2/2. 5 FC Image: the put-output gain is the put-output gain frequency response and to stop the oscillator. 1 Wmp1 V_12 1.3 to 2.2 V 1 Wmp1 V_12 Image: the put-output gain frequency response and to stop the oscillator. 30 Ump1 V_11 Image: the put-output gain frequency response and to stop the oscillator.	98	CTRL¢ CTRL1	0 to V _{CC} 2	VCC2 VCC2 VCC2 VCC2 VCC2 VCC2 VCC2 VCC2 VCC2	 Operation mode switching pins. Refer to the Mode Switching Truth Table for selection of control, acceleration, or deceleration.
6 S/S 0 to V _{CC} 2 • When the S/S pin is HIGH, START; when LOW, STOP. 6 S/S 0 to V _{CC} 2 • When the S/S pin is HIGH, START; when LOW, STOP. 7 FC • Connect a capacitor between this pin GND to reduce the input/output gain frequency response and to stop the oscillator. 1 W _{IN1} 1.3 to 2.2 V • Connect a capacitor between this pin GND to reduce the input/output gain frequency response and to stop the oscillator. 1 W _{IN1} 1.3 to 2.2 V • V _{CC2} 31 U _{IN1} 1.3 to 2.2 V • V _{CC2} 32 V _{IN1} 1.3 to 2.2 V • V _{CC2} 33 V _{IN1} 0 U _{IN1} 0 U _{IN1} 33 U _{IN1} 0 U _{IN1} 0 U _{IN1}	7	NS+	0 to V _{CC} 2 – 1 V	VCC2	 Input pin at noncontrol mode. The input-output gain is 14 dB. (GC2: LOW) Motor stops when V_{NS} = 0 V.
5 FC • Connect a capacitor between this pin GND to reduce the input/output gain frequency response and to stop the oscillator. 1 WIN2 • WIN2 34 WIN2 • I.3 to 2.2 V VIN2 VIN2 VIN1 UIN2 30 UIN2 0 • UIN2 0 • I.3 to 2.2 V	6	S/S	0 to V _{CC} 2	G G M M M M M M M M M M M M M M M M M M	 When the S/S pin is HIGH, START; when LOW, STOP. The threshold is V_{CC}2/2.
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	5	FC		S T T T T T T T T T T T T T T T T T T T	• Connect a capacitor between this pin and GND to reduce the input/output gain frequency response and to stop the oscillator.
$\begin{array}{c ccccc} 34 & W_{IN}^{\prime \prime} 1 \\ 33 & V_{IN}^{\prime \prime} 2 \\ 32 & V_{IN}^{\prime \prime} 1 \\ 31 & U_{IN}^{\prime \prime} 2 \\ 30 & U_{IN}^{\prime \prime} 1 \end{array}$	1	W _{IN} 2	1.3 to 2.2 V		W-phase Hall device input pins.
	34 33 32 31 30	WiN1 VIN2 VIN1 UIN2 UIN1		32 30 30 30 30 30 30 30 30 30 30	Logic "H" represent $W_{IN}1 > W_{IN}2$ V-phase Hall device input pins. Logic "H" represent $V_{IN}1 > V_{IN}2$ U-phase Hall device input pins. Logic "H" represent $U_{IN}1 > U_{IN}2$

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Pin No.	Pin Name	Pin Voltage	Equivalent Circuit Diagram	Pin Function
29 28	VH+ VH–	2.4 V 1.4 V	CC2 CC2 CC2 CC2 CC2 CC2 CC2 CC2 CC2 CC2	 Hall device power supply pins. A voltage difference of 1.0 V is developed between VH+ and VH–.
27	H.FG	0 to V _{CC} 2	VCC2 VCC2 VCC2 VCC2 A04501	 Hall FG pin. The Hall waveform is converted into a pulse signal and then used as the FG pulse signal.
26	CL	0 to V _{CC} 2	ZE WILL AD4502	• When the Rf pin voltage becomes equal to the C_L pin voltage, the current limiter operate. The C_L voltage is determined externally.
25	V _{CC} 1	5 to 18 V		 Power supply for output block. This supply should be kept stable to prevent ripple and noise from entering this pin.



Block Diagram



Sample Application Circuit



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