Ordering number : EN5383

Monolithic Digital IC



FDD Spindle Motor Driver

Overview

The LB1910 is a 3-phase disc drive motor driver that is optimal for use as a 3.5-inch FDD spindle motor driver.

WWW.DZSC.CO

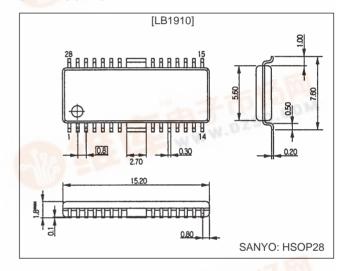
Functions and Features

- Three-phase full-wave linear driver
- Digital speed control circuit
- Start and stop circuits (active low)
- RPM switching H: 300 rpm L: 360 rpm
- · Current limiter circuit
- Built-in index comparator
- · Thermal shutdown circuit

Package Dimensions

unit: mm

3222-HSOP28



Specifications

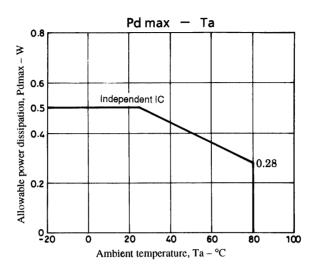
Absolute Maximum Ratings at $Ta = 25^{\circ}C$

| Parameter | Sumbol | Conditions | Potingo | Unit |
|-------------------------------------|---------------------|---|-------------|------|
| Parameter | Symbol | Conditions | Ratings | Unit |
| Maximum supply voltage | V _{CC} max | A TELL TOP IN | 7.0 | V |
| Maximum output current | I _O max1 | t ≤ 0.5 s | 1.0 | А |
| Maximum steady-state output current | I _O max2 | Philips and the second | 0.7 | А |
| Allowable power dissipation | Pd max | Independent IC | 0.5 | W |
| Operating temperature | Topr | | -20 to +80 | °C |
| Storage temperature | Tstg | | -40 to +150 | °C |

Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------------|-----------------|------------|------------|------|
| Recommended supply voltage | V _{CC} | | 4.2 to 6.5 | V |



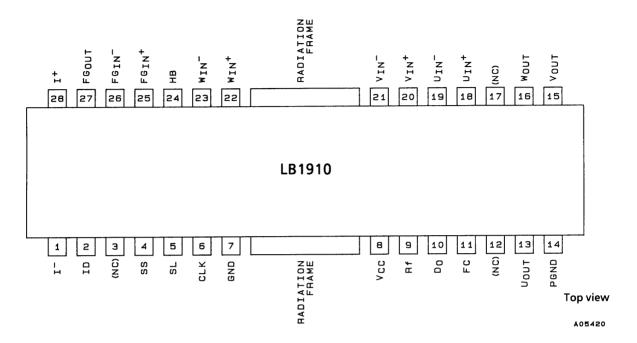


Electrical Characteristics at $Ta=25^{\circ}C,\,V_{CC}$ = 5 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|-------------------|---------------------------------------|------|--------|-----------------------|-------|
| Commont desir | Icco | S/S = 5 V (standby) | | | 10 | μΑ |
| Current drain | Icc | S/S = 0 V (steady state) | | 12 | 18 | mA |
| SL bias current | I _{SL} | V _{SL} = 0 V | | | 10 | μΑ |
| SL input low-level voltage | V _{SLL} | | 0 | | 1.0 | V |
| SL input high-level voltage | V _{SLH} | | 3.5 | | V _{CC} | V |
| S/S bias current | I _{S/S} | | | 180 | 270 | μΑ |
| S/S low-level voltage | V _{S/SL} | | 0 | | 0.8 | V |
| S/S high-level voltage | V _{S/SH} | | 3.5 | | V _{CC} | V |
| Hall amplifier input bias current | I _{HB} | | | | 10 | μΑ |
| Common-mode input voltage range | ٧ _h | | 1.5 | | V _{CC} - 1.0 | ٧ |
| Differential input voltage range | Vdif | | 50 | | 200 | mVp-p |
| Hall bias output voltage | V _H | I _H = 5 mA | | 0.8 | | V |
| Leakage current | I _{HL} | S/S = 5 V | | | ±10 | μA |
| Output saturation voltage | Vsat | I _O = 0.7 A, sink + source | | 1.3 | 1.8 | V |
| Output leakage current | l _{OL} | | | | 1.0 | mA |
| Current limiter | Vlim | | 0.27 | 0.3 | 0.33 | V |
| Control amplifier voltage gain | G _C | | | -7 | | dB |
| Voltage gain difference between phases | ΔG_{C} | | | | ±1 | dB |
| V/I conversion source current | + | | 9 | 14 | 19 | μΑ |
| V/I conversion sink current | - | | -9 | -14 | -19 | μΑ |
| V/I conversion current ratio | I+/I- | | 0.8 | 1.0 | 1.2 | |
| DSC buffer input current | I _{DSC} | | | | 1.0 | μΑ |
| FG Schmitt hysteresis | ΔVsh | * | | 50 | | mV |
| Speed discriminator counts | N | | | 1041.5 | | |
| Discriminator operating frequency | FD | * | | | 1.1 | MHz |
| Oscillator frequency range | Fosc | * | | | 1.1 | MHz |
| Index output low-level voltage | V _{IDL} | I _O = 2 mA | | | 0.4 | V |
| Index output leakage current | IDL | | | | ±10 | μA |
| FG amplifier voltage gain | G _{FG} | * | | 48 | | dB |
| FG amplifier input offset | V _{FG O} | | | | ±10 | mV |
| FG amplifier internal reference voltage | V _{FG B} | | 2.2 | 2.5 | 2.8 | ٧ |
| Thermal shutdown temperature | TSD | * | 150 | 180 | | °C |
| Hysteresis | ΔTSD | * | | 40 | | °C |

Note: * Items marked with an asterisk are design target values and are not measured.

Pin Assignment

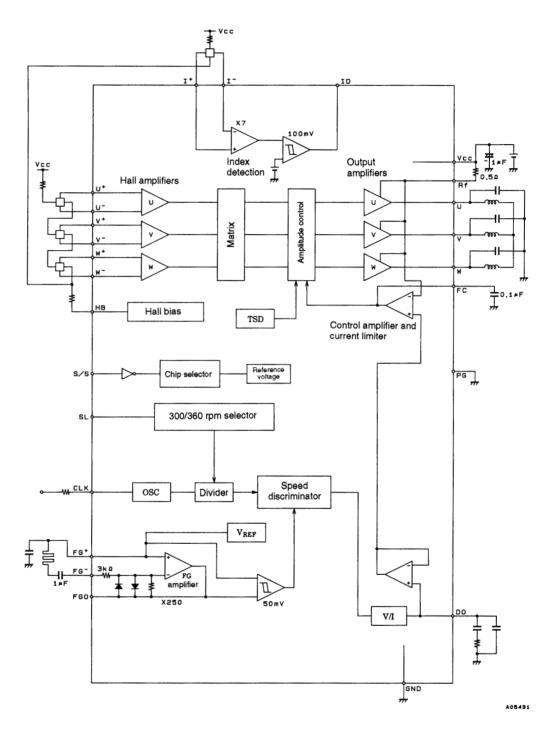


Truth Table

| | Source → sink | Hall input | | | |
|---|-------------------|------------|---|---|--|
| | Source → Sirik | U | V | W | |
| 1 | V phase → W phase | Н | Н | L | |
| 2 | V phase → U phase | L | Н | L | |
| 3 | W phase → U phase | L | Н | Н | |
| 4 | W phase → V phase | L | L | Н | |
| 5 | U phase → V phase | Н | L | Н | |
| 6 | U phase → W phase | Н | L | L | |

Note: Hall input high levels are defined as: $U_{IN}^+ > U_{IN}^- \\ V_{IN}^+ > V_{IN}^- \\ W_{IN}^+ > W_{IN}^-$

Block Diagram



Pin Functions

| Pin No. | Symbol | Pin voltage | Equivalent circuit diagram | Function |
|----------------------------------|--|---|---|---|
| 18 19 20 21 22 23 | U _{IN} + U _{IN} - V _{IN} + V _{IN} - W _{IN} + W _{IN} - | 1.5 V min V _{CC} – 1.0 V max | VCC 18 1k 0 20 W 22 1k 0 1k 0 1k 0 21 W A05421 | U phase Hall element input V phase Hall element input W phase Hall element input |
| 24 | НВ | 0.8 V typ (I _H = 5 mA) | 24 A05422 | Minus side connection for providing the Hall bias current This pin becomes open in the stopped state, thus cutting the Hall bias current. |
| 25 26 27 | FG _{IN} + FG _{IN} - FG _{OUT} | 2.5 V | VCC 25 W VCC 27 W VCC 27 W A05423 | FG amplifier plus input A 2.5-V reference voltage is generated internally. FG amplifier minus input FG amplifier output |
| 28 1 | + - | | VCC 200Ω 200Ω 1 200Ω A05424 | Index input |
| 2 | ID | L: 0.4 V max H: 4.5 V min | A05425 | Index output |

LB1910

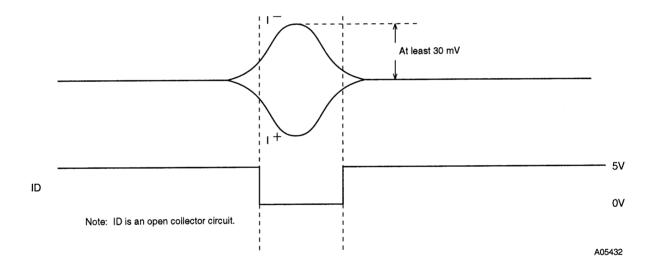
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| Pin No. | Symbol | Pin voltage | Equivalent circuit diagram | Function |
|---------|-----------------|---|----------------------------|---|
| 4 | SS | L: 0.8 V max H: 3.5 V min | VCC 4 | Start/stop mode switching This is an active-low input. |
| 5 | SL | L: 1.0 V max H: 3.5 V min | VCC VCC A05427 | Rotational speed switching |
| 6 | CLK | L: 1.0 V max H: V _{CC} – 1.0 V min | VCC VCC (6) | Reference clock input A 1-MHz input frequency corresponds to speeds of 300 and 360 rpm. |
| 7 | GND | | | Ground This pin, pin 14, and the frame must all be grounded together. |
| 8 | V _{CC} | | | Power supply This voltage must be stabilized so that ripple and noise do not enter the IC. |
| 9 | Rf | | | Output current detection The output current is detected as a voltage by connecting the resistor Rf between this pin and V_{CC} . The current limiter operates by detecting the voltage on this pin. |
| 10 | Do | | 10 W A05429 | Speed discriminator |
| 11 | F _C | | | Frequency characteristics compensation Current control system loop oscillation is prevented by connecting a capacitor between this pin and ground. |

Continued from preceding page.

| Pin No. | Symbol | Pin voltage | Equivalent circuit diagram | Function |
|----------------|--|-------------|----------------------------|--|
| 13 15 16 | U _{OUT} V _{OUT} W _{OUT} | | 9 13 15 16 16 | U phase output V phase output W phase output |
| 14 | PGND | | | Output transistor ground connection |

Index Pulse Timing Chart



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