Ordering number : ENN7099

Monolithic Digital IC

LB1929

Three-Phase Brushless Motor Driver for OA Products

Overview

The LB1929 is a three-phase brushless motor driver that is optimal for driving the drum and paper feed motors in laser printers and plain-paper copiers. It can provide drive with minimal power loss due to direct PWM drive technique, features on-chip peripheral circuits such as a speed control circuit and an FG amplifier, and can implement a drive circuit in a single chip.

Functions and Features

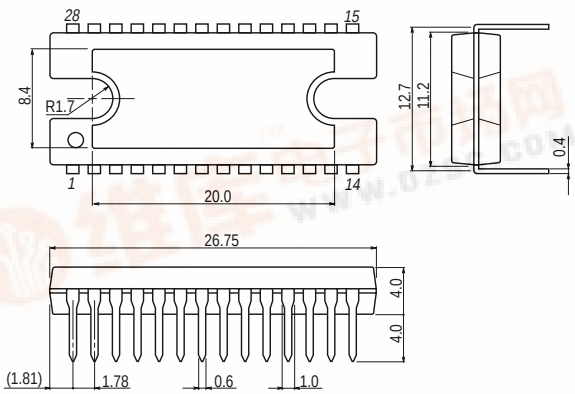
- Three-phase bipolar drive (30 V, 3.5 A)
- Direct PWM drive
- Built-in low side output kickback absorption diode
- Control technique that combines a speed discriminator with PLL speed control
- Speed lock detection output
- Built-in forward/reverse switching circuit
- Full complement of built-in protection circuits, including current limiter, thermal protection circuit, and motor lockup protection circuit.

Package Dimensions

unit: mm

3147B-DIP28H

[LB1929]



SANYO: DIP-28H (500 mil)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		30	V
Output current	I_O max	T ≤ 500 ms	3.5	A
Allowable power dissipation 1	Pd max1	Independent IC	3	W
Allowable power dissipation 2	Pd max2	Infinitely large heat sink	20	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_{CC}		9.5 to 28	V
Regulator-voltage output current	IREG		0 to –30	mA
LD output current	ILD		0 to 15	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = VM = 24 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			23	30	mA
Supply current 2	$I_{CC}2$	Stop mode		3.5	5	mA
Output block						
Output saturation voltage 1	$V_O$sat1	I_O = 1.0 A, V_O (SINK) + V_O (SOURCE)		2.0	2.5	V
Output saturation voltage 2	$V_O$sat2	I_O = 2.0 A, V_O (SINK) + V_O (SOURCE)		2.6	3.2	V
Output leakage current	I_O leak				100	µA
Lower diode forward voltage 1	VD1	ID = –1.0 A		1.2	1.5	V
Lower diode forward voltage 2	VD2	ID = –2.0 A		1.5	2.0	V
Regulator-voltage output						
Output voltage	VREG	I_O = –5 mA	4.65	5.00	5.35	V
Voltage regulation	ΔVREG1	V_{CC} = 9.5 to 28 V		30	100	mV
Load regulation	ΔVREG2	I_O = –5 to –20 mA		20	100	mV
Hall Amplifier						
Input bias current	IHB		–2	–0.5		µA
Common-mode input voltage range	VICM		1.5		VREG – 1.5	V
Hall input sensitivity			80			mVp-p
Hysteresis width	ΔV_{IN}		15	24	42	mV
Input voltage L → H	VSLH			12		mV
Input voltage H → L	VSHL			–12		mV
PWM oscillator circuit						
Output H level voltage	V_{OH} (PWM)		2.5	2.8	3.1	V
Output L level voltage	V_{OL} (PWM)		1.2	1.5	1.8	V
Oscillator frequency	f (PWM)	C = 3900pF		18		kHz
Amplitude	V (PWM)		1.05	1.30	1.55	Vp-p
CSD circuit						
Operating voltage	V_{OH} (CSD)		3.6	3.9	4.2	V
External C charge current	ICHG		–17	–12	–9	µA
Operating time	T (CSD)	C = 10 µF, Design target value		3.3		s
Current limiter operation						
Limiter	VRF	V_{CC}–VM	0.45	0.5	0.55	V
Thermal shutdown operation						
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value (junction temperature)		50		°C

Note*: These items are design target values and are not tested.

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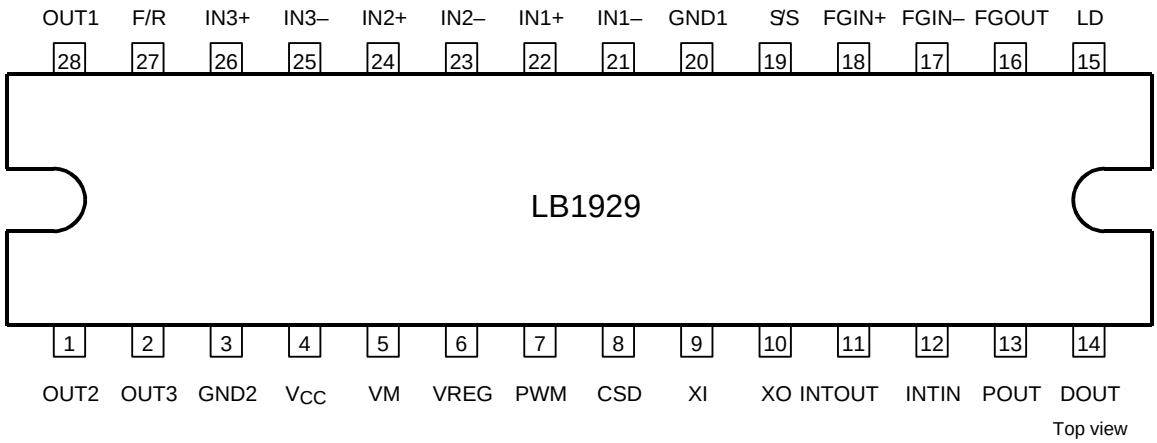
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FG amplifier						
Input offset voltage	V_{IO} (FG)		–10		10	mV
Input bias current	IB (FG)		–1		1	µA
Output H level voltage	V_{OH} (FG)	IFGO = –0.2 mA	VREG – 1.2	VREG – 0.8		V
Output L level voltage	V_{OL} (FG)	IFGO = 0.2 mA		0.8	1.2	V
FG input sensitivity		Gain 100-fold	3			mV
Next-stage Schmidt width		Design target value *	100	180	250	mV
Operating frequency range					2	kHz
Open loop GAIN		f (FG) = 2 kHz	45	51		dB
Speed discriminator						
Output H level voltage	V_{OH} (D)	IDO = –0.1 mA	VREG – 1.0	VREG – 0.7		V
Output L level voltage	V_{OL} (D)	IDO = 0.1 mA		0.8	1.1	V
No. of counts				512		
PLL output						
Output H level voltage	V_{OH} (P)	IPO = –0.1 mA	VREG – 1.8	VREG – 1.5	VREG – 1.2	V
Output L level voltage	V_{OL} (P)	IPO = 0.1 mA	1.2	1.5	1.8	V
Lock detection						
Output L level voltage	V_{OL} (LD)	ILD = 10 mA		0.15	0.5	V
Lock range				6.25		%
Integrator						
Input bias current	IB (INT)		–0.4		0.4	µA
Output H level voltage	V_{OH} (INT)	IINTO = –0.2 mA	VREG – 1.2	VREG – 0.8		V
Output L level voltage	V_{OL} (INT)	IINTO = 0.2 mA		0.8	1.2	V
Open loop GAIN		f (INT) = 1 kHz	45	51		dB
Gain-bandwidth product		Design target value *		450		kHz
Reference voltage		Design target value *	–5%	VREG/2	5%	V
Crystal oscillator						
Operating frequency range	f_{OSC}		3		10	MHz
L level pin voltage	VOSCL	IOSC = –0.5 mA		1.65		V
H level pin current	IOSCH	VOSC = VOSCL + 0.3 V		0.4		mA
Start/stop pin						
H level input voltage range	V_{IH} (S/S)		3.5		VREG	V
L level input voltage range	V_{IL} (S/S)		0		1.5	V
Input open voltage	V_{IO} (S/S)		VREG – 0.5		VREG	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
H level input current	I_{IH} (S/S)	V (S/S) = VREG	–10	0	10	µA
L level input current	I_{IL} (S/S)	V (S/S) = 0 V	–280	–210		µA
Forward/reverse pin						
H level input voltage range	V_{IH} (F/R)		3.5		VREG	V
L level input voltage range	V_{IL} (F/R)		0		1.5	V
Input open voltage	V_{IO} (F/R)		VREG – 0.5		VREG	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
H level input current	I_{IH} (F/R)	V (F/R) = VREG	–10	0	10	µA
L level input current	I_{IL} (F/R)	V (F/R) = 0 V	–280	–210		µA

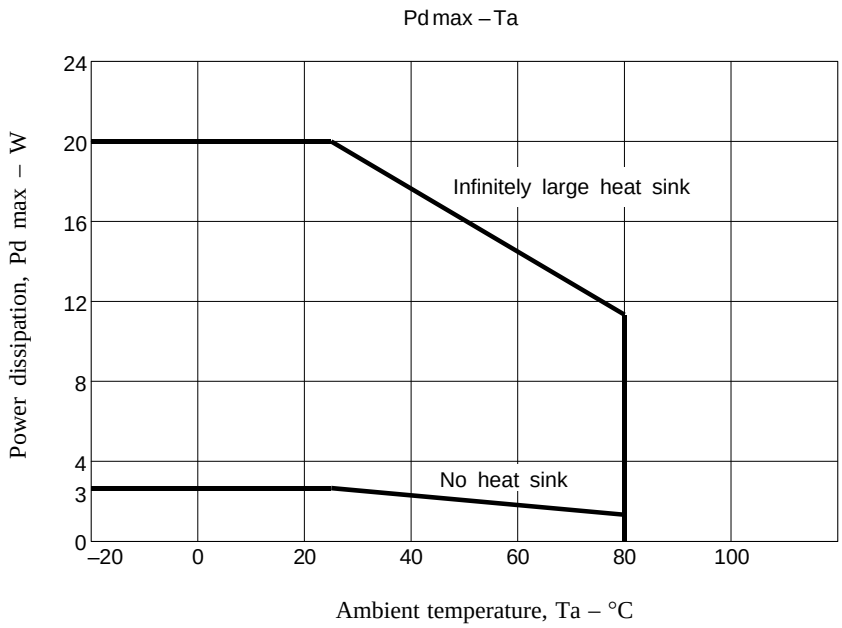
Note*: These items are design target values and are not tested.

Truth Table

	Source / Sink	F/R= "L"			F/R= "H"		
		IN1	IN2	IN3	IN1	IN2	IN3
1	OUT2 → OUT1	H	L	H	L	H	L
2	OUT3 → OUT1	H	L	L	L	H	H
3	OUT3 → OUT2	H	H	L	L	L	H
4	OUT1 → OUT2	L	H	L	H	L	H
5	OUT1 → OUT3	L	H	H	H	L	L
6	OUT2 → OUT3	L	L	H	H	H	L

Pin Assignment



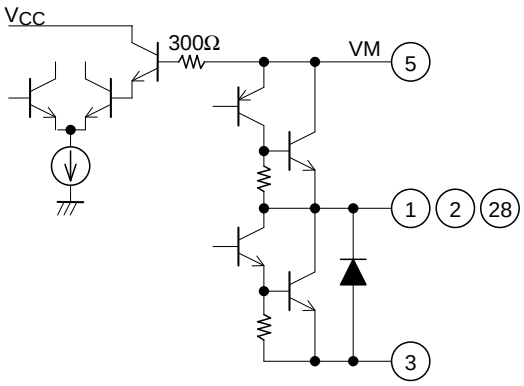
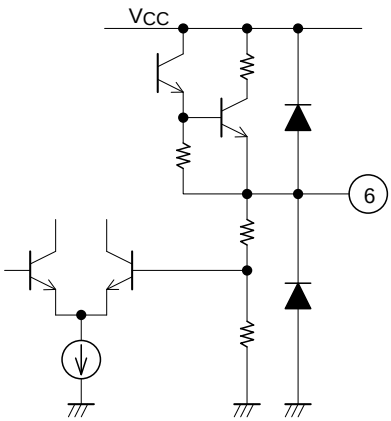
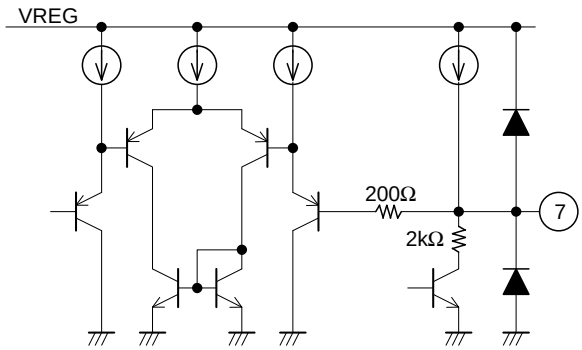
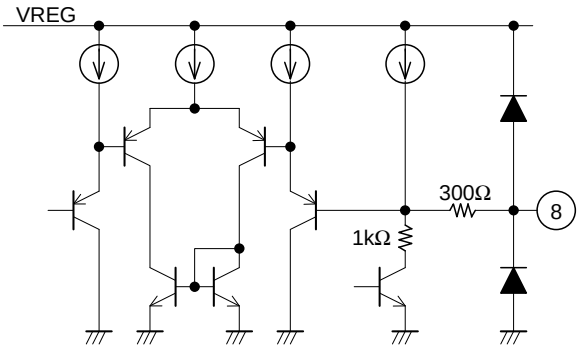


The crystal oscillation frequency fosc is related to the FG frequency f_{FG} as follows:

f_{FG} (servo) = f_{OSC}/(ECL16 division × No. of counts)

= f_{OSC}/8192

Pin Description

Pin No.	Symbol	Pin Description	Equivalent circuit
28 1 2	OUT1 OUT2 OUT3	Motor drive output pin Connect the Schottky diode between the output – V_{CC}.	
3	GND2	Output GND pin	
5	VM	Power and output current detection pins of the output. Connect a low resistance (Rf) between this pin and V_{CC}. The output current is limited to the current value set with I_{OUT} = VRF/Rf.	
4	V_{CC}	Power pin (Other than the output)	
6	VREG	Stabilized power supply output pin (5 V output) Connect a capacitor (about 0.1 µF) between this pin and GND for stabilization.	
7	PWM	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND. This can be set to about 18 kHz with C = 3900pF.	
8	CSD	Pin to set the operation time of motor lock protection circuit. Connection of a capacitor (about 10 µF) between CSD and GND can set the protection operation time of about 3.3seconds.	

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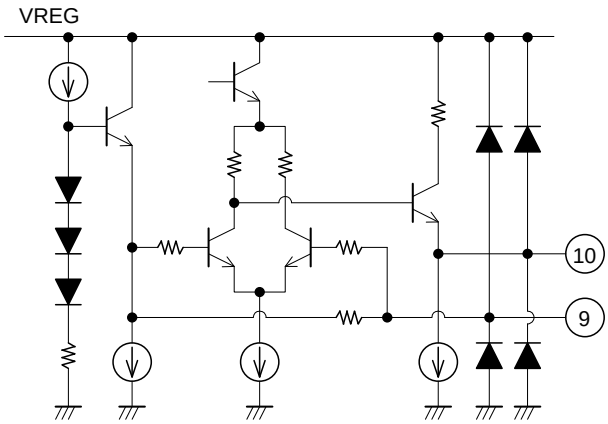
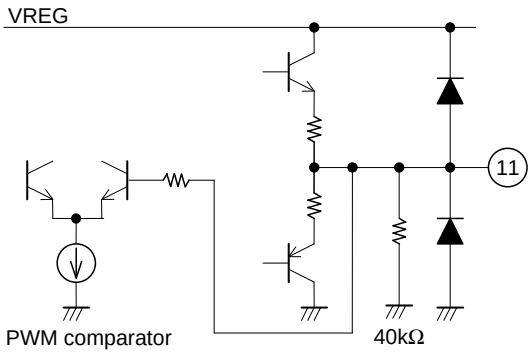
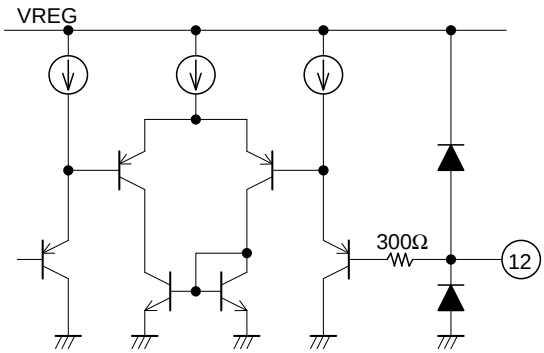
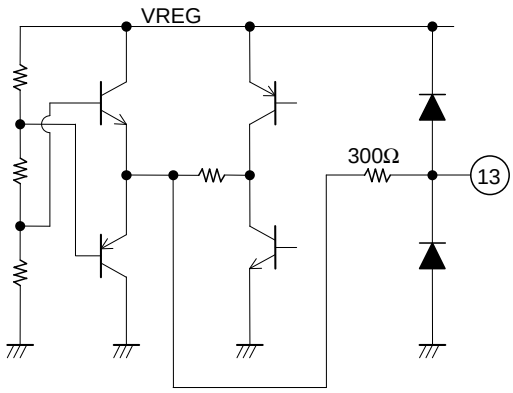
Pin No.	Symbol	Pin Description	Equivalent circuit
9 10	XI XO	Crystal oscillation pin. Connection of a crystal oscillator causes generation of the reference clock. To enter the clock (a few MHz) externally, connect a resistor of about 5.1 kΩ in series to the XI pin and enter the signal via the resistor. In this case, keep XO pin open.	
11	INT OUT	Integrating amplifier output pin (speed control pin)	
12	INT IN	Integrating amplifier input pin	
13	POUT	PLL output pin.	

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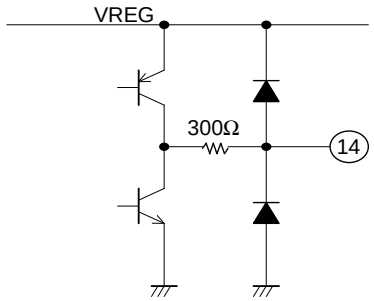
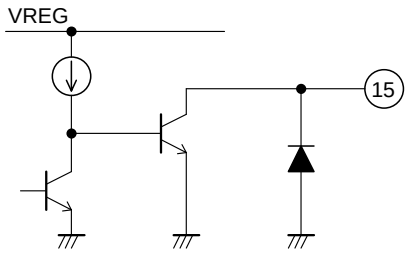
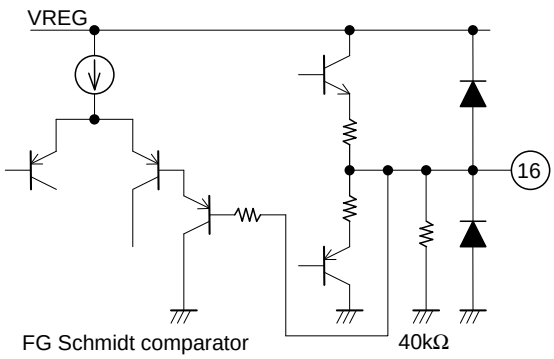
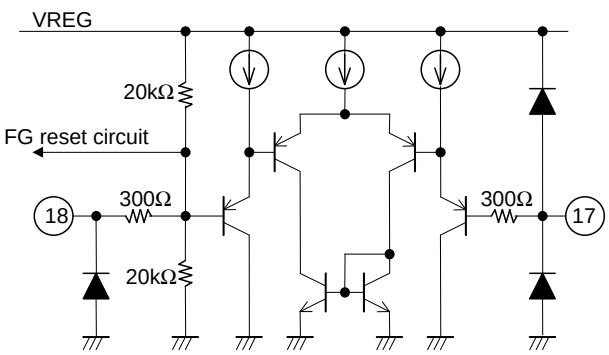
Pin No.	Symbol	Pin Description	Equivalent circuit
14	DOUT	Speed discriminator output pin Acceleration → H Deceleration → L	
15	LD	Speed lock detection output. L when the motor speed is within the speed lock range (±6.25%). Maximam Voltage 30 V	
16	FG OUT	FG amplifier output pin.	
17 18	FGIN– FGIN+	FG amplifier input pin. Connection of a capacitor (about 0.1 µF) between FGIN+ and GND causes initial reset to the logic circuit.	

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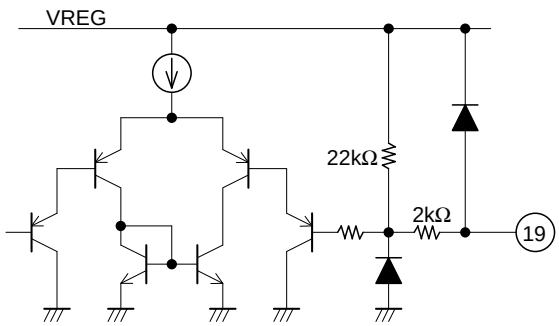
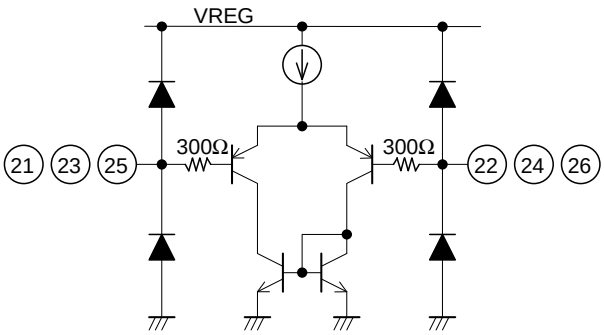
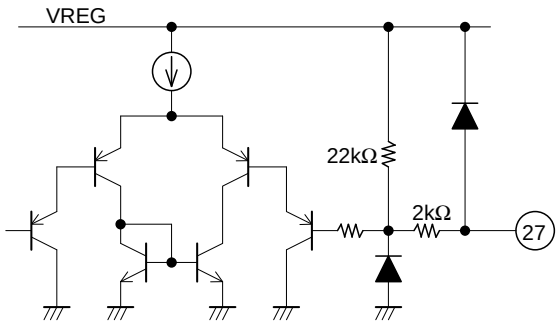
Pin No.	Symbol	Pin Description	Equivalent circuit
19	S/S	Start/stop control pin. L: 0V to 1.5V H: 3.5V to VREG H level when open. Hysteresis width about 0.5 V	
20	GND1	GND pin (Other than the output)	
22 21 24 23 26 25	IN1+ IN1– IN2+ IN2– IN3+ IN3–	Hall amplifier input. IN+ > IN– is the input high state, and the reverse is the input low state. It is recommended that the Hall signal has an amplitude of 100mVp-p(differential) or more. Connect a capacitor between the IN+ and IN– inputs if there is noise in the Hall sensor signals.	
27	F/R	Forward/reverse control pin L: 0V to 1.5V H: 3.5V to VREG H level when open Hysteresis width about 0.5V	

Function Description

1. Speed control circuit

This IC performs speed control by using both the speed discriminator circuit and PLL circuit. The speed control circuit outputs the error signal once for every two cycles of FG (one FG cycle counted). The PLL circuit outputs the phase error signal once for each cycle of FG.

As the FG servo frequency is calculated as follows, the motor speed is set with the number of FG pulses and crystal oscillation frequency.

f_{FG} (servo) = f_{OSC}/8192

f_{OSC}: Crystal oscillation frequency

2. Output drive circuit

This IC employs a direct PWM drive method to minimize the power loss at output. The output Tr is always saturated at ON, and the motor drive force is adjusted through change of the duty at which the output is turned ON. Since the output PWM switching is made with the lower-side output Tr, it is necessary to connect the schottky diode between OUT and V_{CC} (because the through current flows at an instant when the lower-side Tr is turned ON if the diode with a short reverse recovery time is not used). The diode between OUT and GND is incorporated. When the large output current presents problem (waveform disturbance at kickback on the lower side), connect a commutating diode or schottky diode externally.

3. Current limiting circuit

The current limiting circuit performs limiting with the current determined from I = VRF/Rf (VRF = 0.5 Vtyp, Rf: current detector resistance) (that is, this circuit limits the peak current).

Limiting operation includes decrease in the output on-duty to suppress the current.

4. Power save circuit

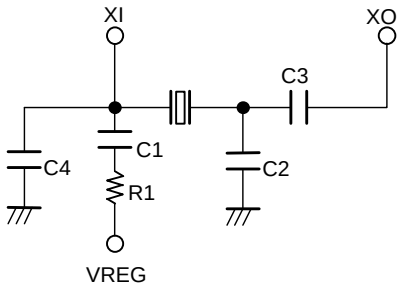
This IC enters the power save condition to decrease the current dissipation in the stop mode. In this condition, the bias current of most of circuits is cut off. Even in the power save condition, the 5 V regulator output is given.

5. Reference clock

The reference clock for speed control can be entered in two ways as described below.

(1) Oscillation with a crystal oscillator

For oscillation with a crystal oscillator, connect X'tal and C, R as shown below.



C1, R1: For oscillation stabilization
C3: For oscillator connection
C2: For over-tone oscillation prevention and stabilization
C4: For over-tone oscillation prevention

Reference value

Oscillation frequency (MHz)	C1 (μF)	C2 (pF)	C3 (pF)	C4 (pF)	R1 (Ω)
3 to 5	0.1	15	47	10	330 k
5 to 8	0.1	10	47	None	330 k
8 to 10	0.1	10	22	None	330 k

This circuit and constant are for reference only. It is necessary that each manufacturer checks for problem because of effects expected due to characteristics of a crystal oscillator and the floating capacity due to routing of a printed circuit board.

(Cautions for routing of a printed circuit board)

The crystal oscillation circuit is a high-frequency circuit and readily influenced by the a printed circuit board floating capacity, etc. Accordingly, due consideration must be made to shorten the wiring as much as possible for external circuits and to reduce the wire width. In the external circuit, the wiring between the oscillator and C3 (C2) is readily influenced particularly by the floating capacity, so that their routing requires particular attention. C4 is highly effective in reducing the negative resistance at high frequency, but due attention is necessary not to reduce excessively the negative resistance with the fundamental wave.

(2) External clock (a few MHz equivalent to the crystal oscillation frequency)

To enter the signal equivalent to the crystal oscillation frequency from the external signal source, enter the signal via resistor (reference value: about 5.1 kΩ) in series with XI pin. In this case, the XO pin must be kept OPEN.

INPUT signal level

L level voltage 0 V to 0.8 V
H level voltage 2.5 V to 5.0 V

6. Speed lock range

The speed lock range is ±6.25% of the constant speed. If the motor speed falls inside the lock range, the LD pin goes to "L" (open collector output). When the motor speed falls outside the lock range, the on-duty ratio of motor drive output changes according to the speed error, causing control to keep the motor speed within the lock range.

7. PWM frequency

PWM frequency is determined from the capacity C (F) of capacitor connected to the PWM pin.

fPWM ≒ 1/(14400 × C)

It is recommended to keep the PWM frequency at 15 – 25 kHz. GND of a capacitor to be connected must be connected to the GND1 pin with the shortest possible wiring.

8. Hall input signal

The Hall input requires the signal input with an amplitude exceeding the hysteresis width (42 mV max). Considering the effect of noise, the input with the amplitude of 100 mV or more is recommended.

When the output waveform is disturbed due to noise effects at a time of changeover of the output phase, connect a capacitor between Hall input pins (+ and –) at a point as near as possible to the pin.

9. F/R changeover

Motor rotation direction can be changed over with the F/R pin. When changing F/R while the motor is running, pay attention to following points.

- For the through current at a time of changeover, the countermeasure is taken using a circuit. However, it is necessary to prevent exceeding of the rated voltage (30 V) due to rise of V_{CC} voltage at a time of changeover (because the motor current returns instantaneously to the power supply). When this problem exists, increase the capacity of a capacitor between V_{CC} and GND.
- When the motor current exceeds the current limit value after changeover, the lower-side Tr is turned OFF. But, the upper-side Tr enters the short-brake condition and the current determined from the motor counter electromotive voltage and coil resistance flows. It is necessary to prevent this current from exceeding the rated current (3.5 A). (F/R changeover at high rotation speed is dangerous.)

10. Motor lock protection circuit

A motor lock protection circuit is incorporated for protection of IC and motor when the motor is locked.

When the LD output is “H” (unlocked) for a certain period in the start condition, the lower-side Tr is turned OFF. This time is set with the capacity of the capacitor connected to the CSD pin. The time can be set to about 3.3 seconds with the capacity of 10 µF (variance about ±30%).

Set time(s) ≒ 0.33 × C (µF)

When the capacitor used has a leak current, due consideration is necessary because it may cause error in the set time, etc.

Cancelling requires either the stop condition or re-application of power supply (in the stop condition). When the lock protection circuit is not to be used, connect the CSD pin to GND.

When the stop period during which lock protection is to be cancelled is short, the charge of capacitor cannot be discharged completely and the lock protection activation time at restart becomes shorter than the set value. It is necessary to provide the stop time with an allowance while referring to the following equation. (The same applies to restart in the motor start transient condition.)

Stop time (ms) ≥ 15 × C (µF)

11. Power supply stabilization

This IC has a large output current and is driven by switching, resulting in ready oscillation of the power line. It is therefore necessary to connect a capacitor with a sufficient capacity (several ten µF or more) between the V_{CC} pin and GND for stabilization. GND of a capacitor to be connected must be connected to the GND2 pin (GND of the power block) at a point as near as possible to the pin. If a capacitor (electrolytic) cannot be provided near the pin because of existence of a heat sink, etc., provide a ceramic capacitor of about 0.1 µF near the pin.

When a diode is inserted in the power line to prevent breakdown due to reverse connection of power supply, the power line is particularly readily oscillated. The larger capacity need be selected.

12. VREG stabilization

The VREG pin (5 V regulator output) that is a power supply for control circuit must be provided with a stabilizing capacitor (about 0.1 µF). GND of a capacitor to be connected must be connected to the GND1 pin with the shortest possible wiring.

13. Constant of integrating amplifier parts

Arrange the integrating amplifier external parts as near as possible to IC to protect them from noise effects. Arrange them by keeping the largest possible distance from the motor.

Equivalent Circuit Block Diagram and Peripheral Circuits