Asynchronous Silicon Gate CMOS LSI

SANYO No. 4816A

LC36128ML-70/85/10

128 K (16384 words × 8 bits) SRAM

Overview

The LC36128ML are fully asynchronous silicon gate CMOS static RAMs with a 16384 words × 8 bits configuration.

This series has a $\overline{CE}$ chip enable pin for device select/non-select control and an $\overline{OE}$ output enable pin for output control, and features high speed as well as low power dissipation.

For these reasons, the series is especially suited for use in systems requiring high speed, low power, and battery backup, and it is easy to expand memory capacity.

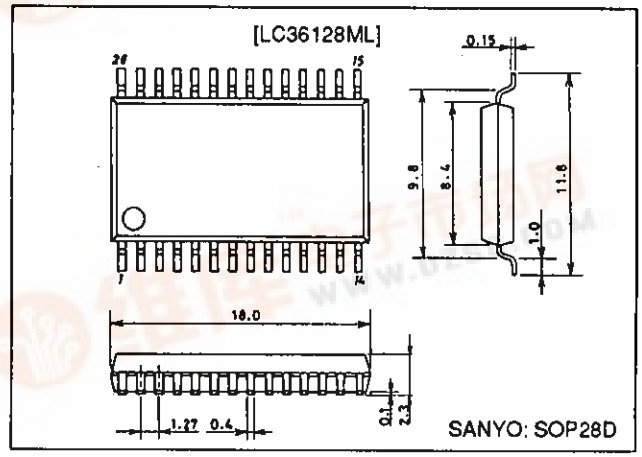
Features

- Access time
  - 70 ns (max.) : LC36128ML-70
  - 85 ns (max.) : LC36128ML-85
  - 100 ns (max.) : LC36128ML-10
- Low current dissipation
  - During standby
    - 1 µA (max.) / Ta = 25°C
    - 2 µA (max.) / Ta = 0 to +40°C
    - 12 µA (max.) / Ta = 0 to +70°C
  - During data retention
    - 0.4 µA (max.) / Ta = 25°C
    - 1 µA (max.) / Ta = 0 to +40°C
    - 5 µA (max.) / Ta = 0 to +70°C
  - During operation (DC)
    - 10 mA (max.)
- Single 5 V power supply: 5 V ± 10%
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input and output levels are TTL compatible
- Common input/output pins, with three output states
- Package
  - SOP 28-pin (450 mil) plastic package : LC36128ML

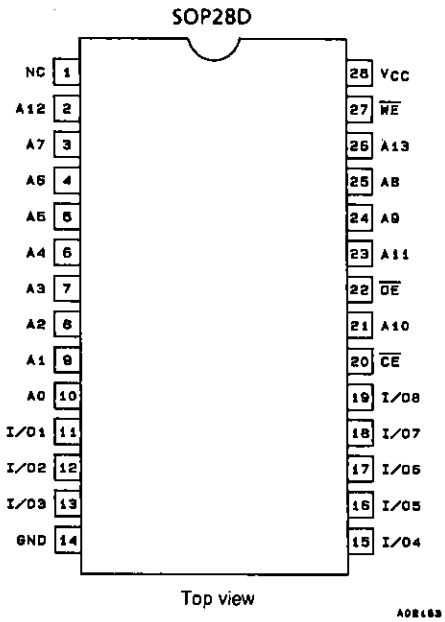
Package Dimensions

unit: mm

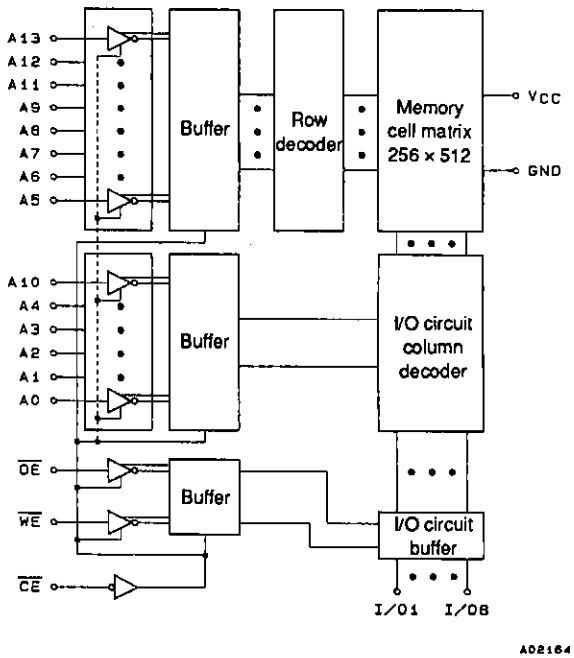
3187-SOP28D



Pin Assignment



Block Diagram



Pin Functions

A0 to A13	Address input
$\overline{WE}$	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE}$	Chip enable input
I/O1 to I/O8	Data input/output
V_{CC}, GND	Power supply pins

Functions Logic

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	L	H	Data output	I_{CCA}
Write cycle	L	X	L	Data input	I_{CCA}
Output disable	L	H	H	High impedance	I_{CCA}
Non-select	H	X	X	High impedance	I_{CCS}

X: H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Input pin voltage	V_{IN}		−0.5* to V_{CC} + 0.5	V
I/O pin voltage	$V_{I/O}$		−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	Pd max		0.7	W
Operating temperature range	Topr		0 to +70	°C
Storage temperature range	Tstg		−55 to +150	°C

* −3.0 V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high level voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Input low level voltage	V_{IL}	−0.3*		+0.8	V

* −3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Conditions			min	typ*	max	Unit
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			−1.0		+1.0	µA
I/O leakage current	I_{LO}	$V_{\overline{CE}} = V_{IH}$ or $V_{\overline{OE}} = V_{IH}$, $V_{I/O}$ = 0 to V_{CC}			−1.0		+1.0	µA
Output high level voltage	V_{OH}	I_{OH} = −1.0 mA			2.4			V
Output low level voltage	V_{OL}	I_{OL} = 2.1 mA					0.4	V
Operating supply current (DC)	I_{CCA1}	$V_{\overline{CE}} \le 0.2$ V, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V, $I_{I/O}$ = 0 mA				1	5	mA
	I_{CCA2}	$V_{\overline{CE}} = V_{IL}$, $I_{I/O}$ = 0 mA				3	10	mA
Average operating supply current	I_{CCA3}	min cycle Duty = 100% $I_{I/O}$ = 0 mA	Access time	70 ns		30	50	mA
				85 ns		25	50	
				100 ns		23	50	
Standby supply current	I_{CCS1}	$V_{\overline{CE}} \ge V_{CC} - 0.2$ V		0 to +70°C			12	µA
				0 to +40°C			2	
				25°C			1	
	I_{CCS2}	$V_{\overline{CE}} = V_{IH}$				0.4	2	mA

* Reference values at V_{CC} = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8	pF
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

AC testing conditions

Input pulse voltage level	:	0.8 V, 2.2 V
Input rise and fall time	:	5 ns
Input - output timing level	:	1.5 V
Output load	:	1 TTL gate + C_L = 100 pF (85 ns/100 ns) 1 TTL gate + C_L = 30 pF (70 ns) (including scope and jig capacitance)

Read Cycle

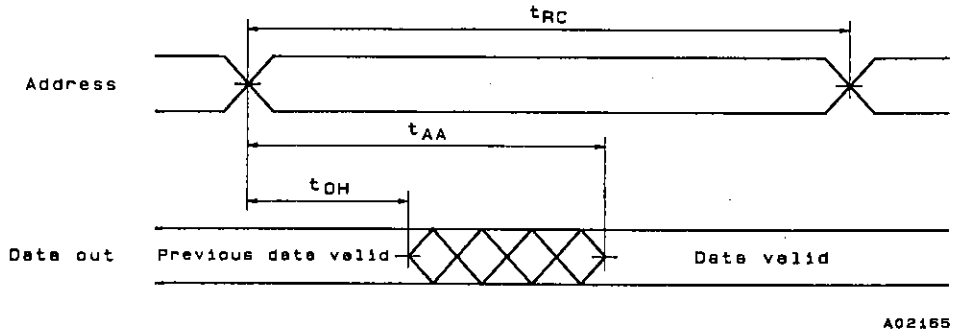
Parameter	Symbol	LC36128ML						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Read cycle time	t_{RC}	70		85		100		ns
Address access time	t_{AA}		70		85		100	ns
$\overline{CE}$ access time	t_{CA}		70		85		100	ns
$\overline{OE}$ access time	t_{OA}		35		45		50	ns
Output hold time	t_{OH}	20		20		20		ns
$\overline{CE}$ output enable time	t_{COE}	10		10		10		ns
$\overline{OE}$ output enable time	t_{OOE}	5		5		5		ns
$\overline{CE}$ output disable time	t_{COD}	0	30	0	30	0	30	ns
$\overline{OE}$ output disable time	t_{OOD}	0	30	0	30	0	30	ns

Write Cycle

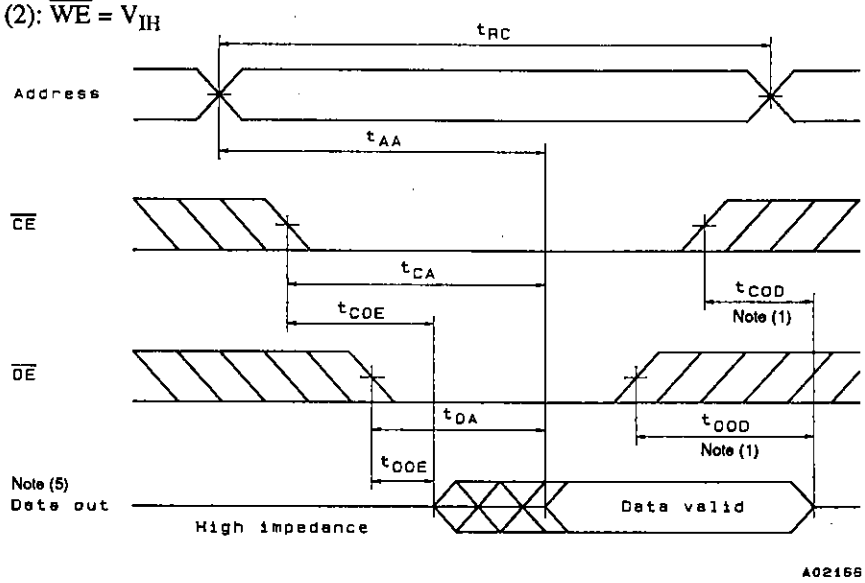
Parameter	Symbol	LC36128ML						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Write cycle time	t_{WC}	70		85		100		ns
Address valid to end of write	t_{AW}	65		75		80		ns
Address setup time	t_{AS}	0		0		0		ns
Write pulse width	t_{WP}	50		50		60		ns
$\overline{CE}$ setup time	t_{CW}	65		75		80		ns
Write recovery time ($\overline{WE}$)	t_{WR}	0		0		0		ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0		0		0		ns
Data setup time	t_{DS}	30		30		35		ns
Data hold time	t_{DH}	0		0		0		ns
$\overline{WE}$ output enable time	t_{WOE}	10		10		10		ns
$\overline{WE}$ output disable time	t_{WOD}	0	25	0	25	0	25	ns

Timing Chart

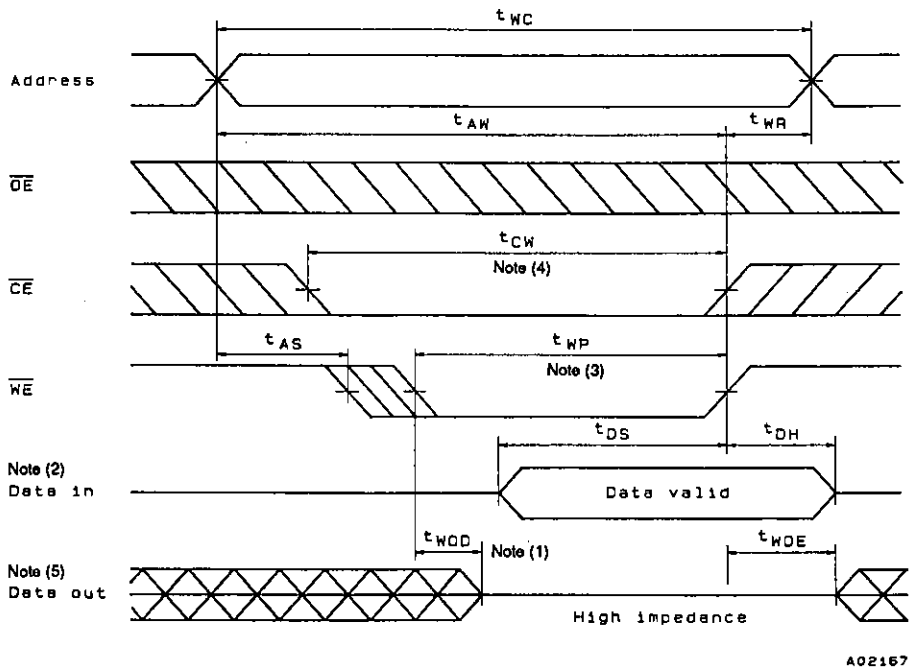
• Read Cycle (1): $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



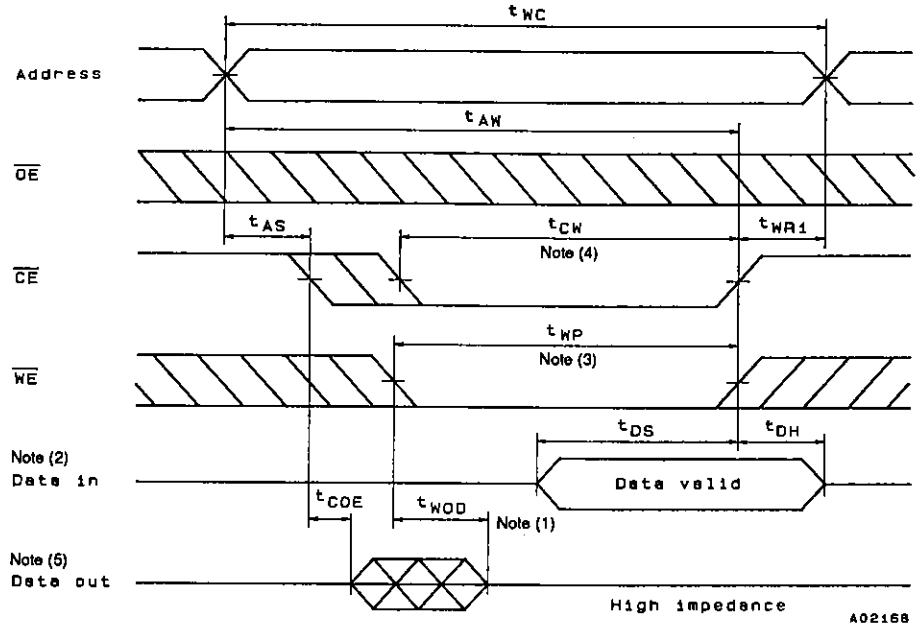
• Read Cycle (2): $\overline{WE} = V_{IH}$



• Write Cycle (1): $\overline{WE}$ Control Note (6)



• Write Cycle (2): $\overline{CE}$ Control Note (6)



Notes: (1) t_{COD}, t_{OOD}, and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.

(2) An external antiphase signal must not be applied when D_{OUT} is in the output state.

(3) t_{WP} is the time interval that $\overline{CE}$ and $\overline{WE}$ are low-level and is defined as the interval from the falling of $\overline{WE}$ to the rising of $\overline{CE}$ or $\overline{WE}$, whichever is earlier.

(4) t_{CW} is the time interval that $\overline{CE}$ and $\overline{WE}$ are low-level and is defined as the time from the falling of $\overline{CE}$ to the rising of $\overline{CE}$ or $\overline{WE}$, whichever is earlier.

(5) D_{OUT} goes to the high-impedance state when either $\overline{OE}$ is high-level, $\overline{CE}$ is high-level, or $\overline{WE}$ is low-level.

(6) When $\overline{OE}$ is high-level during the write cycle, D_{OUT} goes to the high-impedance state.

Data Retention Characteristics at Ta = 0 to +70°C

Parameter	Symbol	Conditions		min	typ	max	Unit
Data retention supply voltage	V_{DR}	$V_{\overline{CE}} \geq V_{CC} - 0.2$ V		2.0		5.5	V
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, $V_{\overline{CE}} \geq 2.8$ V	0 to +70°C			5	µA
			0 to +40°C			1	
			25°C			0.4	
	I_{CCDR2}	V_{CC} = 2.0 to 5.5 V, $V_{\overline{CE}} \geq V_{CC} - 0.2$ V				12	µA
$\overline{CE}$ setup time	t_{CDR}			0			ns
$\overline{CE}$ hold time	t_R			t_{RC}*			ns

* t_{RC} = Read Cycle time

Data Retention Waveform