

	No. 4326	Asynchronous Silicon Gate CMOS LSI LC3664BL, BML-70/85/10/12
		64 K (8192 words x 8 bits) SRAM

Overview

The LC3664BL, BML-70/85/10/12 are fully asynchronous silicon gate CMOS static RAMs with an 8192 words x 8 bits.

This series has $\overline{CE1}$ and $\overline{CE2}$ chip enable pins for device select/nonselect control and an $\overline{OE}$ output enable pin for output control, and features high speed as well as low power dissipation.

For these reasons, the series is especially suited for use in systems requiring high speed, low power, and battery backup, and it is easy to expand memory capacity.

Features

• Access time

70 ns (max.) : LC3664BL-70, LC3664BML-70

85 ns (max.) : LC3664BL-85, LC3664BML-85

100 ns (max.) : LC3664BL-10, LC3664BML-10

120 ns (max.) : LC3664BL-12, LC3664BML-12

• Low current dissipation

During standby

0.5 μ A (max.) /Ta = 25°C

1 μ A (max.) /Ta = 0 to 40°C

6 μ A (max.) /Ta = 0 to 70°C

During data retention

0.2 μ A (max.) /Ta = 25°C

0.5 μ A (max.) /Ta = 0 to 40°C

2.5 μ A (max.) /Ta = 0 to 70°C

During operation (DC)

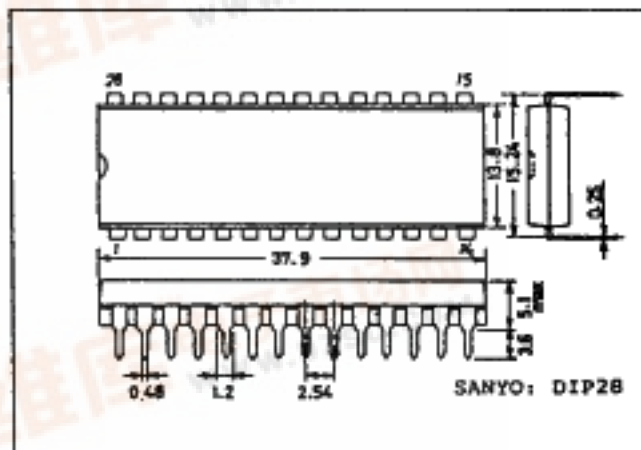
10 mA (max.)

- Single 5 V power supply: 5 V $\pm$ 10%
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Packages
 - DIP 28-pin plastic package (600 mil) : LC3664BL
 - SOP 28-pin plastic package (450 mil) : LC3664BML

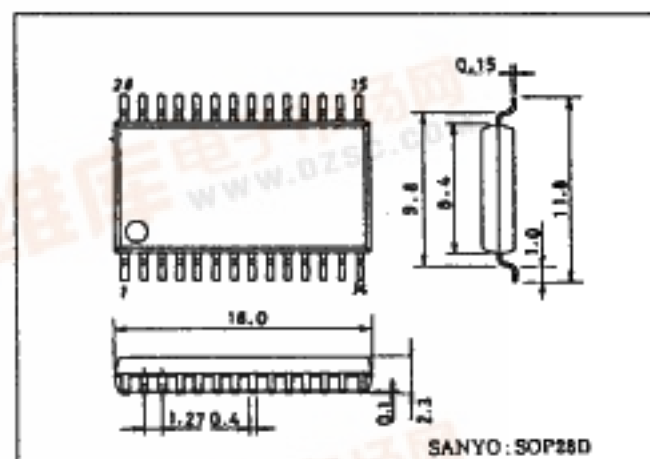
Package Dimensions

unit : mm

3012A - DIP28



3187 - SOP28D



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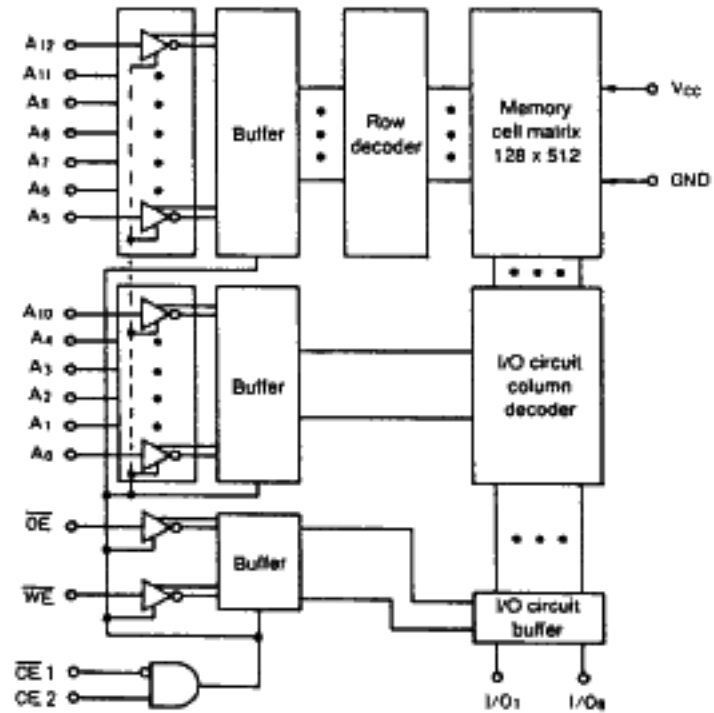
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Pin Assignment



Block Diagram



A0 to A12 : Address input
WE : Read/write control input
OE : Output enable input
CE1, CE2 : Chip enable input
I/O1 to I/O8 : Data input/output
Vcc, GND : Power supply pins

Functions

Mode	<u>CE 1</u>	<u>CE 2</u>	<u>OE</u>	<u>WE</u>	I/O	Supply current
Read cycle	L	H	L	H	Data output	ICCA
Write cycle	L	H	X	L	Data input	ICCA
Output disable	L	H	H	H	High impedance	ICCA
Nonselect	H	X	X	X	High impedance	ICCS
	X	L	X	X	High impedance	ICCS

X : H or L

Specifications

Absolute Maximum Ratings at $T_a=25^{\circ}\text{C}$

Parameter	Symbol	Condition	Rating	unit
Maximum supply voltage	$V_{CC\text{ max}}$		7.0	V
Input pin voltage	V_{IH}		-0.5* to $V_{CC}+0.5$	V
I/O pin voltage	V_{IO}		-0.5* to $V_{CC}+0.5$	V
Allowable power dissipation	$P_{d\text{ max}}$	LC3664BL	1.0	W
		LC3664BML	0.7	W
Operating temperature range	T_{opg}		0 to 70	$^{\circ}\text{C}$
Storage temperature range	T_{stg}		-55 to +150	$^{\circ}\text{C}$

* -3.0 V when pulse width is less than 50 ns

DC Allowable Operating Ranges at $T_a = 0$ to 70°C

Parameter	Symbol	min	typ	max	unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input "H" level voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input "L" level voltage	V_{IL}	-0.3*		+0.8	V

* -3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at $T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Condition		min	typ*	max	unit
Input leakage current	I _I	V _{IN} = 0 to V _{CC}		-0.5		+0.5	μA
I/O leakage current	I _{IO}	V _{CE1} = V _{IH} or V _{CE2} = V _{IL} or V _{OE} = V _{IH} or V _{WE} = V _{IL} , V _{IO} = 0 to V _{CC}		-0.5		+0.5	μA
Output "H" level voltage	V _{OH}	I _{OH} = -1.0mA		2.4			V
Output "L" level voltage	V _{OL}	I _{OL} = 2.1mA				0.4	V
Operating supply current (DC)	I _{CCA1}	V _{CE1} ≤ 0.2V, V _{CE2} ≥ V _{CC} -0.2V, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V, I _{IO} = 0mA			1	5	mA
	I _{CCA2}	V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{IO} = 0mA, V _{IN} = V _{IH} or V _{IL}			3	10	mA
Average operating supply current	I _{CCA3}	V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{IO} = 0mA, min cycle	Access time	70ns	30	50	mA
				85ns	25	50	
				100ns	23	50	
				120ns	20	50	
Standby supply current	I _{CCS1}	{V _{CE2} ≤ 0.2V} or {V _{CE1} ≥ V _{CC} -0.2V, (V _{CE2} ≥ V _{CC} -0.2V or V _{CE2} ≤ 0.2V)}	0 to 70°C	0.2	6	μA	
			0 to 40°C		1		
			25°C		0.5		
	I _{CCS2}	V _{CE2} = V _{IL} or V _{CE1} = V _{IH} , V _{IN} = 0 to V _{CC}		0.4	2	mA	

* Reference values at $V_{CC} = 5\text{ V}$, $T_a = 25^{\circ}\text{C}$

LC3664BL, BML-70/85/10/12

Input/Output Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$

Parameter	Symbol	Condition	min	typ	max	unit
Input/output capacitance	C_{IO}	$V_{IO} = 0\text{V}$			8	pF
Input capacitance	C_{IN}	$V_{IN} = 0\text{V}$			6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at $T_a = 0\text{ to }70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

AC testing conditions

Input pulse voltage level	:	0.8 V, 2.2 V
Input rise and fall time	:	5 ns
Input - output timing level	:	1.5 V
Output load	:	1 TTL gate + $C_L = 100\text{ pF}$ (85 ns/100 ns/120 ns) 1 TTL gate + $C_L = 30\text{ pF}$ (70 ns) (including scope and jig capacitance)

Read Cycle

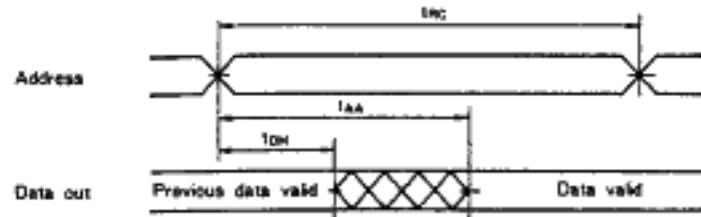
Parameter	Symbol	LC3664BL-70 LC3664BML-70		LC3664BL-85 LC3664BML-85		LC3664BL-10 LC3664BML-10		LC3664BL-12 LC3664BML-12		unit
		min	max	min	max	min	max	min	max	
Read cycle time	t_{RC}	70		85		100		120		ns
Address access time	t_{AA}		70		85		100		120	ns
CE1 access time	t_{CA1}		70		85		100		120	ns
CE2 access time	t_{CA2}		70		85		100		120	ns
OE access time	t_{OA}		35		45		50		60	ns
Output hold time	t_{OH}	20		20		20		20		ns
CE1 output enable time	t_{COE1}	10		10		10		10		ns
CE2 output enable time	t_{COE2}	10		10		10		10		ns
OE output enable time	t_{OOE}	5		5		5		5		ns
CE1 output disable time	t_{COD1}	0	30	0	30	0	30	0	30	ns
CE2 output disable time	t_{COD2}	0	30	0	30	0	30	0	30	ns
OE output disable time	t_{OOD}	0	30	0	30	0	30	0	30	ns

Write Cycle

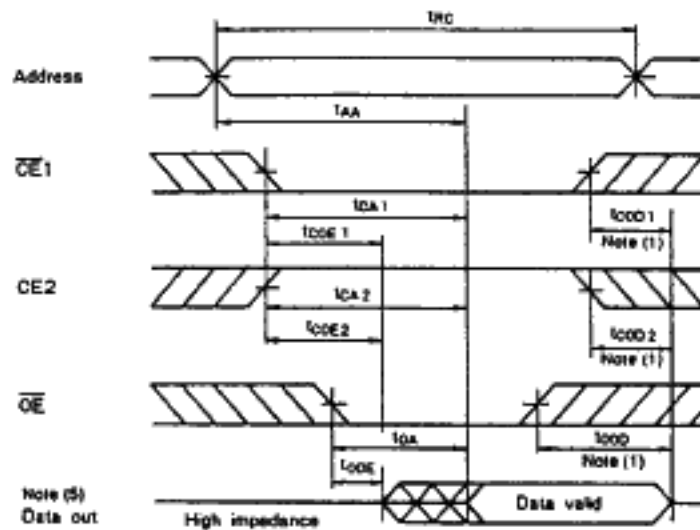
Parameter	Symbol	LC3664BL-70 LC3664BML-70		LC3664BL-85 LC3664BML-85		LC3664BL-10 LC3664BML-10		LC3664BL-12 LC3664BML-12		unit
		min	max	min	max	min	max	min	max	
Write cycle time	t_{WC}	70		85		100		120		ns
Address valid to end of write	t_{AW}	60		60		75		85		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	50		50		60		70		ns
CE1 setup time	t_{CW1}	60		60		75		85		ns
CE2 setup time	t_{CW2}	60		60		75		85		ns
Write recovery time	t_{WR}	0		0		0		0		ns
CE1 Write recovery time	t_{WR1}	0		0		0		0		ns
CE2 Write recovery time	t_{WR2}	0		0		0		0		ns
Data setup time	t_{DS}	30		30		35		40		ns
Data hold time	t_{DH}	0		0		0		0		ns
CE1 Data hold time	t_{DH1}	0		0		0		0		ns
CE2 Data hold time	t_{DH2}	0		0		0		0		ns
WE output enable time	t_{WOE}	10		10		10		10		ns
WE output disable time	t_{WOD}	0	25	0	25	0	25	0	25	ns

Timing Charts

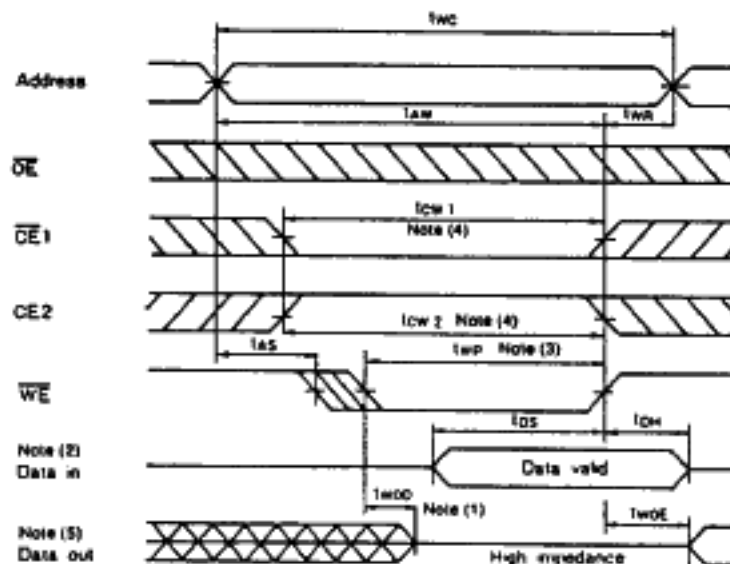
- Read Cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



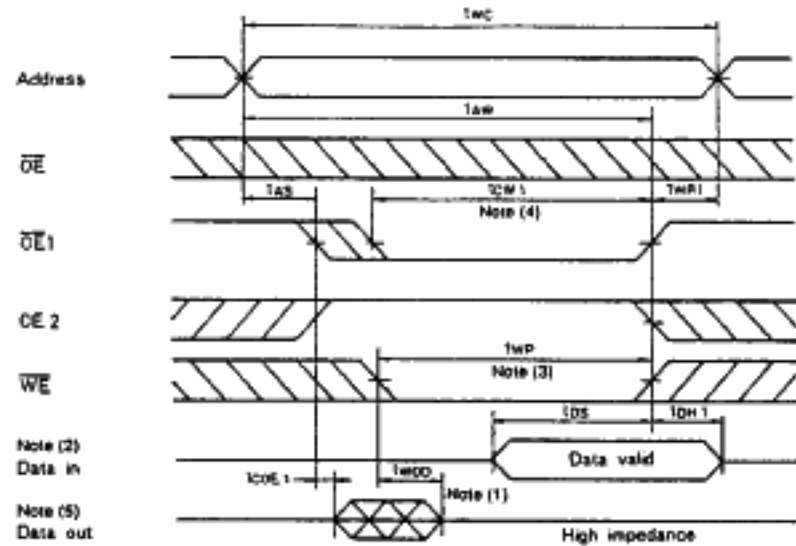
- Read Cycle (2): $\overline{WE} = V_{IH}$



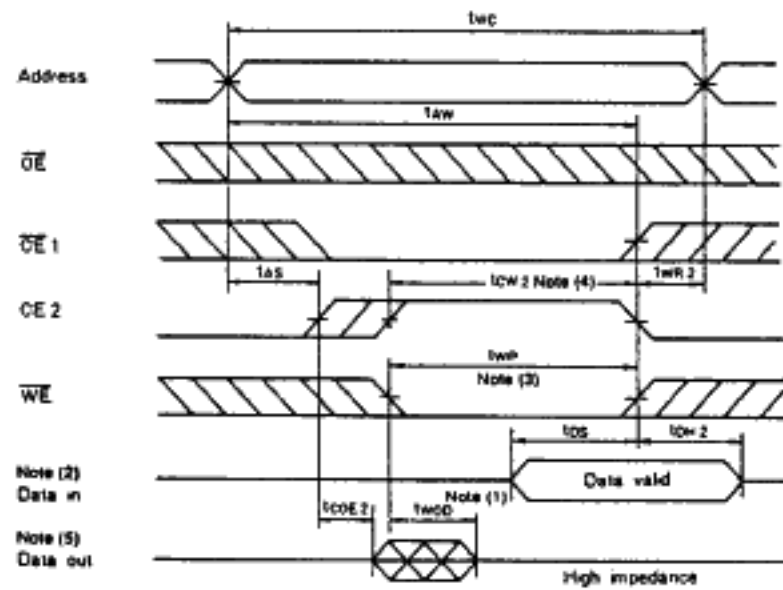
- Write Cycle (1): $\overline{WE}$ Control Note (6)



• Write Cycle (2): $\overline{CE1}$ Control Note (6)



• Write Cycle (3): $\overline{CE2}$ Control Note (6)



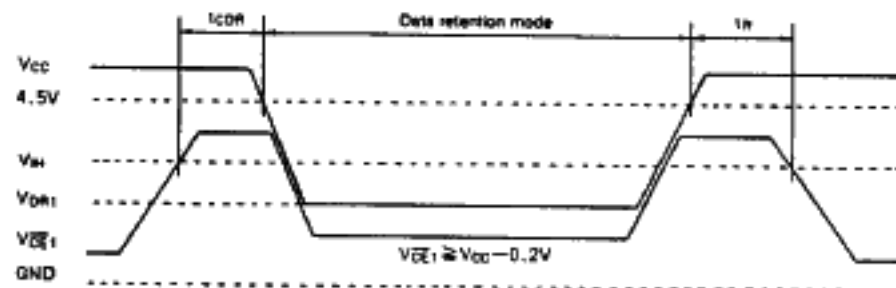
- Notes (1) t_{COD1} , t_{COD2} , t_{OOD} , and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.
- (2) An external antiphase signal must not be applied when DOUT is in the output state.
- (3) t_{WP} is the time interval that $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are low-level and CE2 is high-level, and is defined as the interval from the falling of $\overline{\text{WE}}$ to the rising of $\overline{\text{CE1}}$ or $\overline{\text{WE}}$, or the falling of CE2, whichever is earlier.
- (4) t_{CW1} and t_{CW2} are the time interval that $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are low-level and CE2 is high-level, and is defined as the time from the falling of $\overline{\text{CE1}}$ or the rising of CE2 to the rising of $\overline{\text{CE1}}$ or $\overline{\text{WE}}$, or the falling of CE2, whichever is earlier.
- (5) DOUT goes to the high-impedance state when either $\overline{\text{OE}}$ is high-level, $\overline{\text{CE1}}$ is high-level, CE2 is low-level, or $\overline{\text{WE}}$ is low-level.
- (6) When $\overline{\text{OE}}$ is high-level during the write cycle, DOUT goes to the high-impedance state.

Data Retention Characteristics at $T_a = 0$ to 70°C

Parameter	Symbol	Condition	min	typ	max	unit
Data retention supply voltage	V_{DR1}	$V_{\text{CE1}} \geq V_{\text{CC}} - 0.2\text{V}$, $V_{\text{CE2}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{CE2}} \leq 0.2\text{V}$	2.0		5.5	V
	V_{DR2}	$V_{\text{CE2}} \leq 0.2\text{V}$	2.0		5.5	V
Data retention supply current	I_{CCDR1}	$V_{\text{CC}} = 3.0\text{V}$, $V_{\text{CE1}} \geq V_{\text{CC}} - 0.2\text{V}$, $V_{\text{CE2}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{CE2}} \leq 0.2\text{V}$	0 to 70°C		2.5	μA
			0 to 40°C		0.5	
			25°C		0.2	
	I_{CCDR2}	$V_{\text{CC}} = 3.0\text{V}$, $V_{\text{CE2}} \leq 0.2\text{V}$	0 to 70°C		2.5	μA
			0 to 40°C		0.5	
			25°C		0.2	
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_{H}		t_{RC}^*			ns

* t_{RC} = Read Cycle time

Data Retention Waveform (1) ($\overline{\text{CE1}}$ control)



Data Retention Waveform (2) (CE2 control)

