Ordering number : EN*5087C

CMOS LSI



LC371100SP, SM, ST-10/20LV

1 MEG (131072 words× 8 bits) Mask ROM Internal Clocked Silicon Gate

Preliminary

Overview

The LC371100SP, LC371100SM and LC371100ST are 131,072-word × 8-bit organization (1,048,576-bit) mask programmable read only memories.

The LC371100SP-10, LC371100SM-10 and LC371100ST-10 feature an access time of 100 ns, an OE access time of 40 ns, and a standby current of 30 μ A, and are optimal for use in 5-V systems that require high-speed access.

The LC371100SP-20LV, LC371100SM-20LV and LC371100ST-20LV feature an access time of 200 ns, an OE access time of 80 ns, and a standby current of 4 μ A. Additionally, they provide high-speed access in 3.3-V systems (3.0 to 3.6 V) with a 150-ns access time and a 60-ns OE access time.

These ROMs adopt the JEDEC standard pin assignment which allows them to replace EPROM easily. To prevent bus line collisions in multi-bus microcontroller systems, pin 24 can be mask programmed to be either active high or active low.

Features

- 131072 words × 8 bits organization
- Power supply

LC371100SP, SM, ST-10: 5.0 V ± 10% LC371100SP, SM, ST-20LV: 2.7 to 3.6 V

• Fast access time (t_{AA}, t_{CA})

LC371100SP, SM, ST-10: 100 ns (max.) LC371100SP, SM, ST-20LV: 200 ns (max.)

150 ns $(V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$

· Operating current

LC371100SP, SM, ST-10: 70 mA (max.) LC371100SP, SM, ST-20LV: 20 mA (max.)

· Standby current

LC371100SP, SM, ST-10: 30 μA (max.) LC371100SP, SM, ST-20LV: 5 μA (max.)

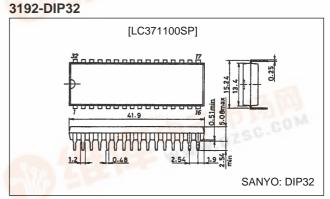
- Full static operation (internal clocked type)
- Fully TTL compatible (5 V supply)
- 3 state outputs
- JEDEC standard pin configuration
- · Package type

LC371100SP-10/20LV: DIP32 (600 mil) LC371100SM-10/20LV:SOP32 (525 mil)

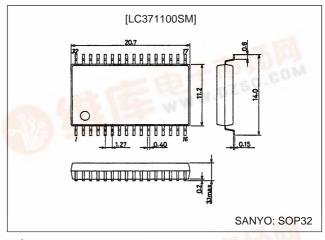
C371F00ST-10/20LV: TSOP32 (8 mm × 20 mm)

Package Dimensions

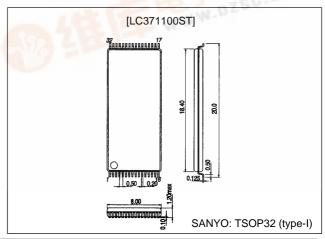
unit: mm



unit: mm 3205-SOP32

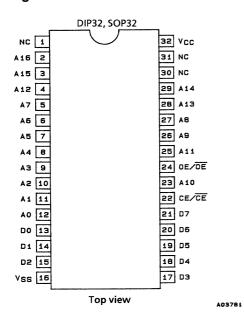


unit: mm **3224-TSOP32**



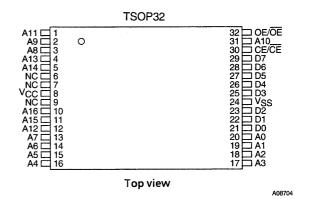
LC371100SP, SM, ST-10/20LV

Pin Assignments

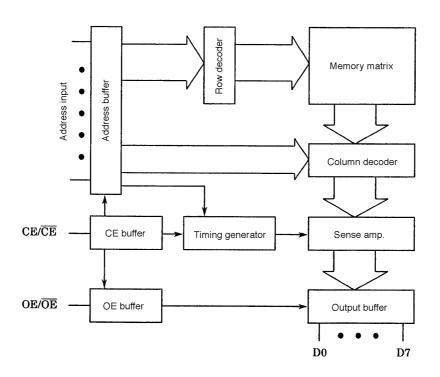


Pin Functions

A0 to A16	Address input
D0 to D7	Data output
CE/CE	Chip enable input
OE/OE	Output enable input
V _{CC}	Power supply
V _{SS}	Ground



Block Diagram



Truth Table

CE/CE	OE/OE Output		Current drain
L/H	Х	High-impedance	Standby mode
H/L	L/H	High-impedance	Operating mode
H/L	H/L	DOUT	Operating mode

LC371100SP, SM, ST-10/20LV

Specifications

Absolute Maximum Ratings *1

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		-0.3 to +7.0	V
Supply input voltage	V _{IN}		-0.3*2 to V _{CC} + 0.3	V
Supply output voltage	V _{OUT}		-0.3 to V _{CC} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C; Reference values for the SANYO DIP package	1.0	W
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Note: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions.

Input/Output Capacitance* at Ta = 25°C, f = 1.0 MHz

Parameter	Svmbol	Conditions		Unit		
Parameter Symbol		Conditions	min	typ	max] Offit
Input capacitance	C _{IN}	V _{IN} = 0 V; Reference values for the SANYO DIP package			8	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V; Reference values for the SANYO DIP package			10	pF

Note: * This parameter is periodically sampled and not 100% tested.

3 V Operation

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions		Unit		
	Symbol		min	typ	max	Oill
Supply voltage	V _{CC} max		2.7	3.0	3.6	V
Input high level voltage	V _{IH}		0.8 V _{CC}		V _{CC} + 0.3	V
Input low level voltage	V _{IL}		-0.3		+0.4	V

DC Electrical Characteristics at Ta=0 to $+70^{\circ}C,\,V_{CC}=$ 2.7 to 3.6 V

Parameter	Symbol	Conditions		- Unit		
Farameter	Symbol	Conditions	min	typ	max	1 OIIII
Operating cumply current	I _{CCA1}	CE = 0.2 V (CE = V _{CC} - 0.2 V), V _I = V _{CC} - 0.2 V/0.2 V			15	mA
Operating supply current I _{CCA2}		$\overline{\text{CE}} = \text{V}_{\text{IL}} \text{ (CE = V}_{\text{IH}}), \text{ I}_{\text{O}} = 0 \text{ mA}, \text{ V}_{\text{I}} = \text{V}_{\text{IH}}/\text{V}_{\text{IL}}, \text{ f} = 5 \text{ MHz}$			20	mA
Standby supply current	I _{CCS1}	<u>CE</u> = V _{CC} - 0.2 V (CE = 0.2 V)			5 (0.5*)	μA
Standby supply current	I _{CCS2}	CE = V _{IH} (CE = V _{IL})			50 (10*)	μA
Input leakage current	ILI	V _{IN} = 0 to V _{CC}			±1.0	μA
Output leakage current	I _{LO}	$\overline{\text{CE}}$ or $\overline{\text{OE}} = V_{\text{IH}}$ (CE or $\overline{\text{OE}} = V_{\text{IL}}$), $V_{\text{OUT}} = 0$ to V_{CC}			±1.0	μA
Output high level voltage	V _{OH}	$I_{OH} = -0.5 \text{ mA}$	V _{CC} - 0.2			V
Output low level voltage	V _{OL}	I _{OL} = 0.5 mA			0.2	V

Note: * Guaranteed at Ta = 25°C

AC Characteristics at Ta = 0 to $+70^{\circ}C$, V_{CC} = 2.7 to 3.6 V

Parameter	Symbol	Conditions		- Unit		
	Symbol		min	typ	max	Onit
Cycle time	t _{CYC}		200 (150*2)			ns
Address access time	t _{AA}				200 (150*2)	ns
CE access time	t _{CA}				200 (150*2)	ns
OE access time	t _{OA}				80 (60*2)	ns
Output hold time	tон		25			ns
Output disable time*1	t _{OD}				50	ns

Note: 1. t_{OD} is measured from the earlier edge of the $\overline{\text{CE}}$ (CE) or $\overline{\text{OE}}$ (OE)'s going high impedance. This parameter is periodically sampled and not 100% tested.

^{2.} V_{IN} (min) = -3.0 V (pulse width \leq 30 ns)

^{2.} Guaranteed at V_{CC} = 3.0 to 3.6 V

5 V Operation

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Cymphal	Conditions		Unit		
raianietei	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V _{CC} max		4.5	5.0	5.5	V
Input high level voltage	V _{IH}		2.2		V _{CC} + 0.3	V
Input low level voltage	V _{IL}		-0.3		+0.6	V

DC Characteristics at Ta = 0 to +70°C, V_{CC} = 5.0 V ±10%

Parameter	Symbol	Conditions	Ratings			
Falametei	Symbol	Conditions	min	typ	max	Unit
Operating supply current	I _{CCA1}	$\overline{\text{CE}}$ = 0.2 V (CE = V _{CC} – 0.2 V), V _I = V _{CC} – 0.2 V/0.2 V			30	mA
Operating supply current	I _{CCA2}	$\overline{\text{CE}} = \text{V}_{\text{IL}} \text{ (CE = V}_{\text{IH}}), \text{ I}_{\text{O}} = 0 \text{ mA}, \text{ V}_{\text{I}} = \text{V}_{\text{IH}}/\text{V}_{\text{IL}}, \text{ f} = 10 \text{ MHz}$			70	mA
Standby supply current	I _{CCS1}	$\overline{CE} = V_{CC} - 0.2 \text{ V (CE} = 0.2 \text{ V)}$			30 (1.0*)	μA
Standby supply current	I _{CCS2}	$\overline{CE} = V_{IH} (CE = V_{IL})$			1.0 (300*)	mA (μA)
Input leakage current	ILI	V _{IN} = 0 to V _{CC}			±1.0	μA
Output leakage current	I _{LO}	$\overline{\text{CE}}$ or $\overline{\text{OE}} = V_{\text{IH}}$ (CE or OE = V_{IL}), $V_{\text{OUT}} = 0$ to V_{CC}			±1.0	μA
Output high level voltage	V _{OH}	I _{OH} = -1.0 mA	2.4			V
Output low level voltage	V _{OL}	I _{OL} = 2.0 mA			0.4	V

Note: * Guaranteed at Ta = 25°C

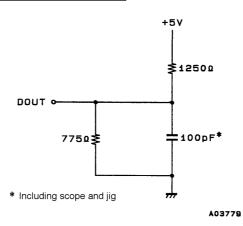
AC Characteristics at Ta = 0 to +70°C, V_{CC} = 5.0 V $\pm 10\%$

Parameter	Symbol Conditions		Unit			
		Conditions	min	typ	max	Onit
Cycle time	t _{CYC}		100			ns
Address access time	t _{AA}				100	ns
CE access time	t _{CA}				100	ns
OE access time	t _{OA}				40	ns
Output hold time	t _{OH}		20			ns
Output disable time*	t _{OD}				30	ns

Note: * t_{OD} is measured from the earlier edge of the $\overline{\text{CE}}$ (CE) or $\overline{\text{OE}}$ (OE)'s going high impedance. This parameter is periodically sampled and not 100% tested.

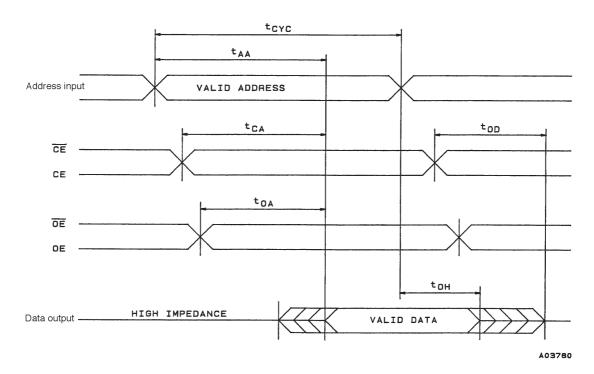
AC Test Conditions

Input pulse levels	0.4 V to 0.8 V _{CC} (3 V measurement), 0.6 V to 2.4 V (5 V measurement)
Input rise/fall time	5 ns
Input timing level	1.5 V
Output timing level	1.5 V
Output load	70 pF (3 V measurement) See figure (5 V measurement)



Output Load (5 V measurement)

Timing Chart



System Design Notes

These LSIs adopt an internal synchronization technique in which operation is started by detecting changes in either the CE input or the address inputs. As a result, the output data immediately after power on is invalid. Once power has been applied, valid data is output after the application changes the value of either the CE input or at least one of the address inputs.

Another point due to the use of the ATD technique is that these LSIs are extremely sensitive to input noise. Applications must take precautions to provide stable input signals, both for the CE input and the address inputs, to prevent incorrect operation.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of April, 1998. Specifications and information herein are subject to change without notice.