

SANYO	No.2365B	CMOS LSI
		LC7151
C MOS Si Gate LSI Meeting FCC 10-Channel Standard PLL FOR CORDLESS TELEPHONE		

Functions :

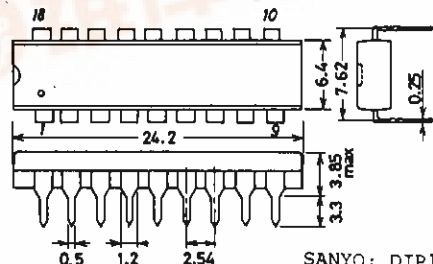
- On-chip PLL for transmission/reception
- On-chip digital unlock detector (only PLL for transmission)
- 5.0kHz/4.4kHz output pins for guard tone
- Standby function
- Pull-down resistance at CH select pins (D1 to D4)
LC7150: With (for mechanical SW)
LC7151: Without (for μ COM)

Absolute Maximum Ratings at $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

			unit
Maximum Supply Voltage	V_{DDmax}	-0.3 to 6.5	V
Maximum Input Voltage	$V_{I,max}$	All input pins -0.3 to $V_{DD}+0.3$	V
Maximum Output Voltage	V_{O1max}	$\overline{F1}, \overline{F2}$ output OFF	-0.3 to +6.5 V
	V_{O2max}	Output pins other than V_{O1}	-0.3 to $V_{DD}+0.3$ V
Output Current	I_{OUT}	$\overline{F1}, \overline{F2}, \text{LDT}$	0 to 3.0 mA
Allowable Power Dissipation	P_{dmax}	$T_a \geq 75^{\circ}\text{C}$	350 mW
Operating Temperature	T_{opr}		-30 to +75 $^{\circ}\text{C}$
Storage Temperature	T_{stg}		-40 to +125 $^{\circ}\text{C}$

Allowable Operating Conditions at $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

			min	typ	max	unit
Supply Voltage	V_{DD}		3.0		5.5	V
"H"-Level Input Voltage	V_{IH1}	D1 to D4, \overline{SB}	$0.7V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	V_{IL1}	"	0		$0.3V_{DD}$	V
"H"-Level Input Voltage	V_{IH2}	$\overline{R/B}$	$0.9V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	V_{IL2}	"	0		$0.1V_{DD}$	V
Input Frequency	f_{IN1}	PIT; $V_{IN}=0.15V_{rms}$	10		27	MHz
	f_{IN2}	PIR; "	30		42	MHz
	f_{IN3}	XIN; $V_{IN}=0.3V_{rms}$	5.0	10.24	11.0	MHz
Input Amplitude	V_{IN1}	PIT; $f_{IN}=27\text{MHz}$	0.15		$0.3V_{DD}$	Vrms
	V_{IN2}	PIR; $f_{IN}=42\text{MHz}$	0.15		$0.3V_{DD}$	Vrms
	V_{IN3}	XIN; $f_{IN}=11\text{MHz}$	0.3		$0.3V_{DD}$	Vrms

Package Dimensionsunit:mm
3007A-DIP18

SANYO: DIP18

Electrical Characteristics at Ta=25°C, under Allowable Operating Conditions

			min	typ	max	unit
"H"-Level Input Current	I _{IH1}	XIN; V _I =V _{DD}			20	µA
"L"-Level Input Current	I _{IL1}	XIN; V _I =V _{SS}			20	µA
"H"-Level Input Current	I _{IH2}	PIT, PIR; V _I =V _{DD}			40	µA
"L"-Level Input Current	I _{IL2}	PIT, PIR; V _I =V _{SS}			40	µA
"H"-Level Input Current	I _{IH3}	SB, R/B, D1 to D4; V _I =V _{DD}			10	µA
"L"-Level Input Current	I _{IL3}	SB, R/B, D1 to D4; V _I =V _{SS}			10	µA
Feedback Resistance	R _{f1}	XIN; V _{DD} =4.3V		1.0		Mohm
	R _{f2}	PIT, PIR; "		0.5		Mohm
"H"-Level Output Voltage	V _{OH1}	PDT, PDR; I _o =0.5mA	V _{DD} -1.0			V
"L"-Level Output Voltage	V _{OL1}	PDT, PDR; I _o =0.5mA			1.0	V
Output OFF Leak Current	I _{off1}	PDT, PDR; V _o =V _{DD} /V _{SS}		0.01	1.0	nA
"H"-Level Output Voltage	V _{OH2}	LDT; I _o =1mA	V _{DD} -1.0			V
Output OFF Leak Current	I _{off2}	LDT; Output OFF V _o =V _{SS}			5.0	µA
"L"-Level Output Voltage	V _{OL2}	F1, F2; I _o =1mA			1.0	V
Output OFF Leak Current	I _{off3}	F1, F2; output OFF V _o =5.5V			5.0	µA
Current Dissipation	I _{DD1}	(C3) V _{DD} =3.0V		4		mA
	I _{DD2}	(C3) V _{DD} =4.5V		7		mA
	I _{DD3}	(C3) V _{DD} =5.5V		13		mA
	I _{DD4}	(C2) V _{DD} =3.0V		3		mA
	I _{DD5}	(C2) V _{DD} =4.5V		5		mA
	I _{DD6}	(C2) V _{DD} =5.5V		10		mA

(C3): XIN=10.24MHz, Xtal connected

PIT=27MHz 150mVrms

PIR=42MHz 150mVrms

R/B=V_{DD}, SB=V_{DD}, Other pin open

(C2): XIN=10.24MHz, Xtal connected

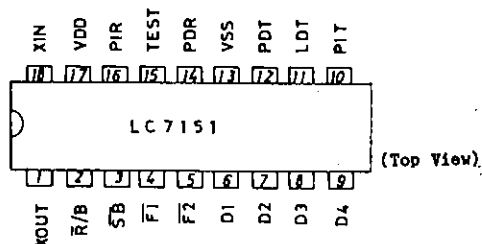
PIR=42MHz, 150mVrms

R/B=V_{DD}, SB=V_{SS}, Other pin open

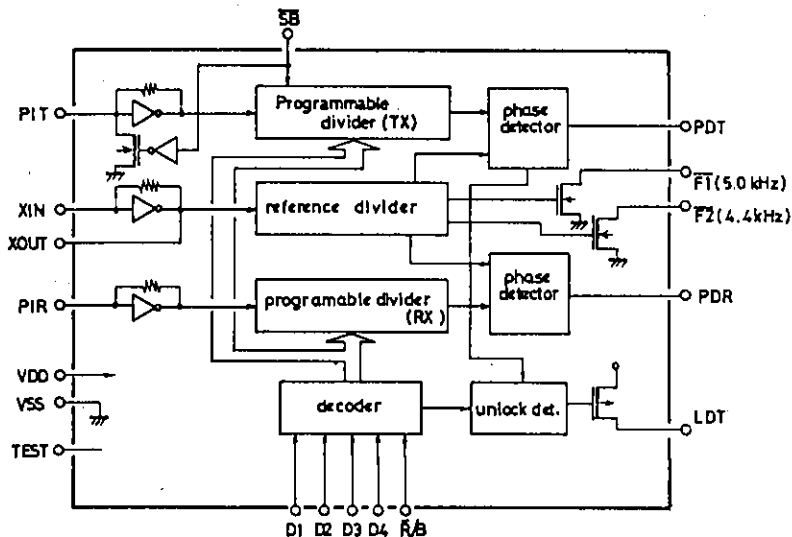
(Note)

Power V_{DD}-V_{SS}: Insert a capacitor of 2000pF or greater.

Pin Assignment

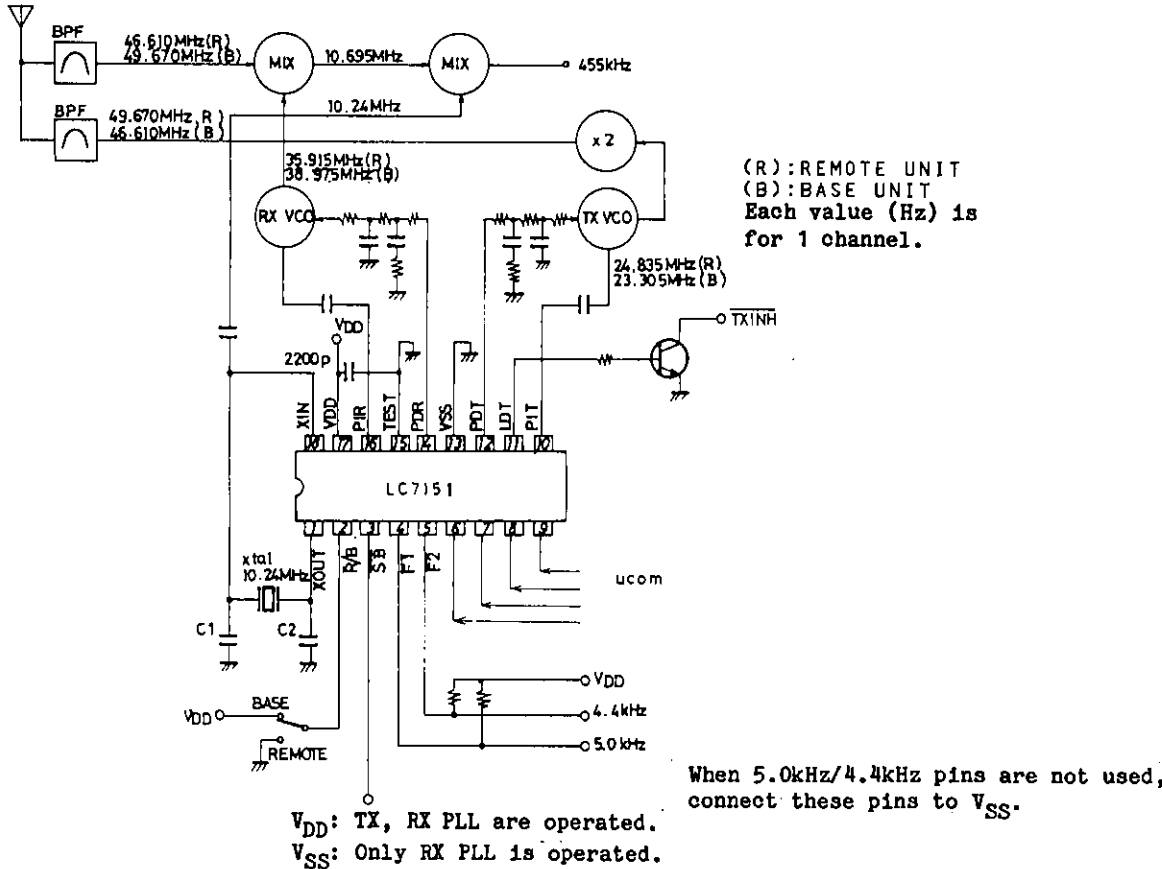


Equivalent Circuit Block Diagram



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Sample Application Circuit



Pin Description

- F1:** 5.0kHz output. When not used, connect to V_{SS} .
- F2:** 4.4kHz output ($10.24\text{MHz} \div 2304$). When not used, connect to V_{SS} .
- V_{DD}, V_{SS} :** Power supply.
- XIN, XOUT:** Crystal resonator (10.24MHz).
- D1 to D4:** Channel select pin.
- $\overline{R/B}$:** Base unit/remore unit select pin.
 $\overline{R/B} = "0" (V_{SS})$Remote unit
 $\overline{R/B} = "1" (V_{DD})$Base unit
- \overline{SB} :** Used to stop the TX PLL at the standby mode to minimize current dissipation.
 $\overline{SB} = "0" (V_{SS})$The charge pump enters a high-impedance mode. Standby mode. Only the RX PLL is operated.
 $\overline{SB} = "1" (V_{DD})$ The TX, RX PLL are operated.
- PIT:** TX programmable divider input pin.
- PIR:** RX programmable divider input pin.
- PDT:** TX charge pump output pin.
- PDR:** RX charge pump output pin.
- TEST:** LSI test input pin. Connected to V_{SS} .
- LDT:** TX PLL unlock signal output pin.

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When the phase difference becomes $t_D (=6.25\mu s)$ or more, 5.6ms output pulse is delivered at the LDT pin.

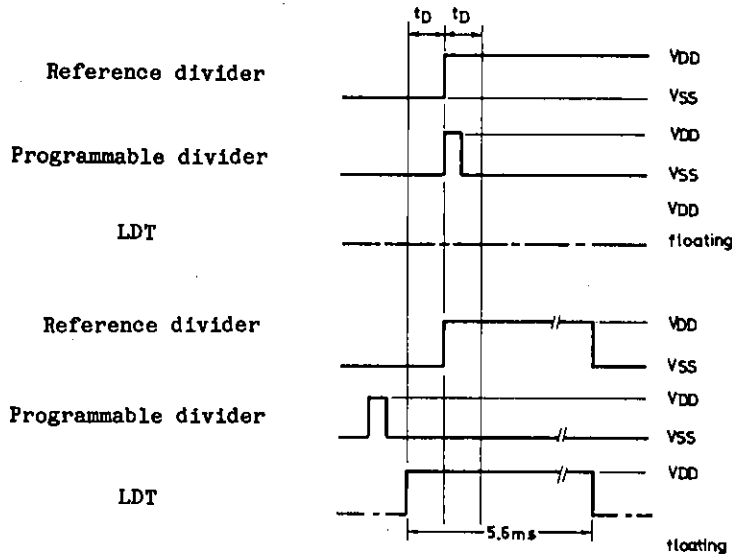


Table of Frequency Division

INPUT D1D2D3D4	C H	REMOTE ($\bar{R}/B='0'$)					BASE ($\bar{R}/B='1'$)				
		TX($f_{ref}=2.5kHz$)		RX($f_{ref}=5kHz$)			TX($f_{ref}=2.5kHz$)		RX($f_{ref}=5kHz$)		
		fTX (MHz)	fVCO (MHz)	N	fVCO (MHz)	N	fTX (MHz)	fVCO (MHz)	N	fVCO (MHz)	N
1 0 0 0	1	49.670	24.8350	9934	35.915	7183	46.610	23.305	9322	38.975	7795
0 1 0 0	2	49.845	24.9225	9969	35.935	7187	46.630	23.315	9326	39.150	7830
1 1 0 0	3	49.860	24.9330	9972	35.975	7195	46.670	23.335	9334	39.165	7833
0 0 1 0	4	49.770	24.8850	9954	36.015	7203	46.710	23.355	9342	39.075	7815
1 0 1 0	5	49.875	24.9375	9975	36.035	7207	46.730	23.365	9346	39.180	7836
0 1 1 0	6	49.830	24.9150	9966	36.075	7215	46.770	23.385	9354	39.135	7827
1 1 1 0	7	49.890	24.9450	9978	36.135	7227	46.830	23.415	9366	39.195	7839
0 0 0 1	8	49.930	24.9650	9986	36.175	7235	46.870	23.435	9374	39.235	7847
1 0 0 1	9	49.990	24.9950	9998	36.235	7247	46.930	23.465	9386	39.295	7859
0 1 0 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1 1 0 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0 0 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1 0 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0 1 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1 1 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0 0 0 0	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855

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