

Overview

The LC72140 and LC72140M are high-performance, phase-locked loop (PLL) frequency synthesizers that operate over the VHF, MW and LW wave bands. They feature excellent frequency tracking, making them ideal as a reference frequency source for use in AM/FM radio receivers.

The LC72140 and LC72140M operate from a 5 V supply. The LC72140 is available in 24-pin DIPs, and the LC72140M, in 24-pin MFPs.

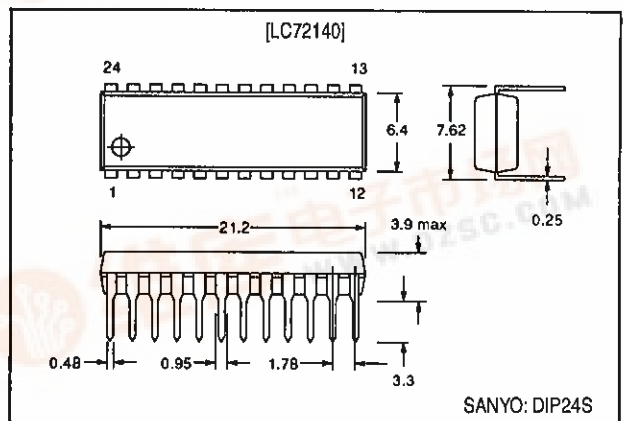
Features

- High-speed programmable dividers for
 - 10 to 160 MHz on FMIN using pulse swallower
 - 0.5 to 40.0 MHz on AMIN using pulse swallower and direct division
- General-purpose counters (used together with the SD in IF count mode)
 - HCTR for 0.4 to 25.0 MHz frequency measurement
 - LCTR for 10 to 500 kHz frequency measurement and 1 Hz to 20 kHz period measurement
- 4.5 or 7.2 MHz crystal
- Twelve selectable reference frequencies (1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 25, 30, 50 and 100 kHz)
- Phase comparator
 - Insensitive band control
 - Unlock detection
 - Sub-charge pump for high-speed locking
 - Deadlock clear circuit
- C²B input/output data interface
- Power-ON reset circuit
- Built-in MOS transistor for a low-pass filter
- Inputs/outputs (using five general-purpose input/output ports)
 - Maximum of seven inputs
 - Maximum of seven outputs (three n-channel open-drain and four CMOS outputs)
- 5 V supply
- 24-pin DIP (LC72140) and 24-pin MFP (LC72140M)

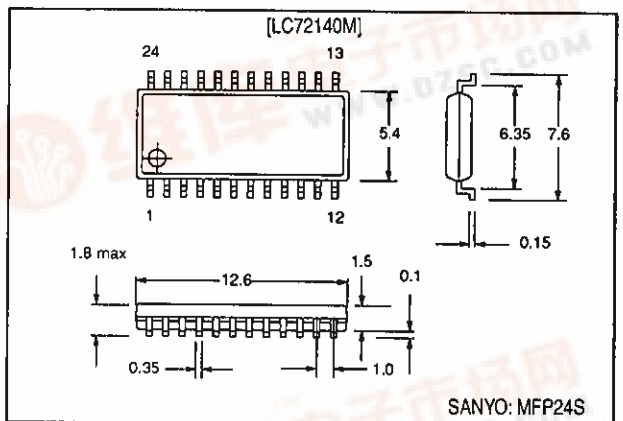
Package Dimensions

Unit: mm

3067-DIP24S

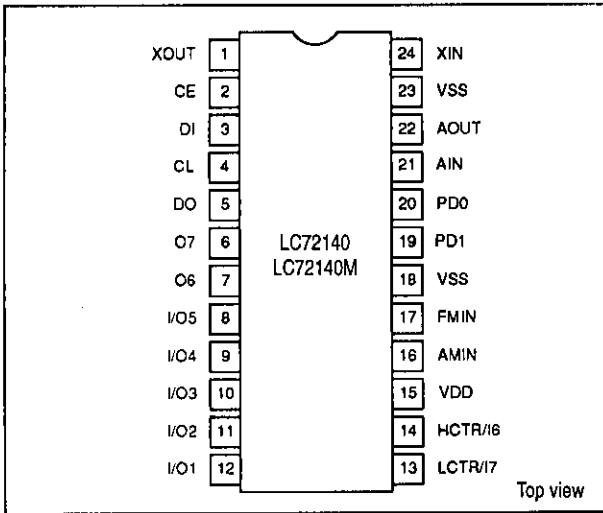


3112-MFP24S

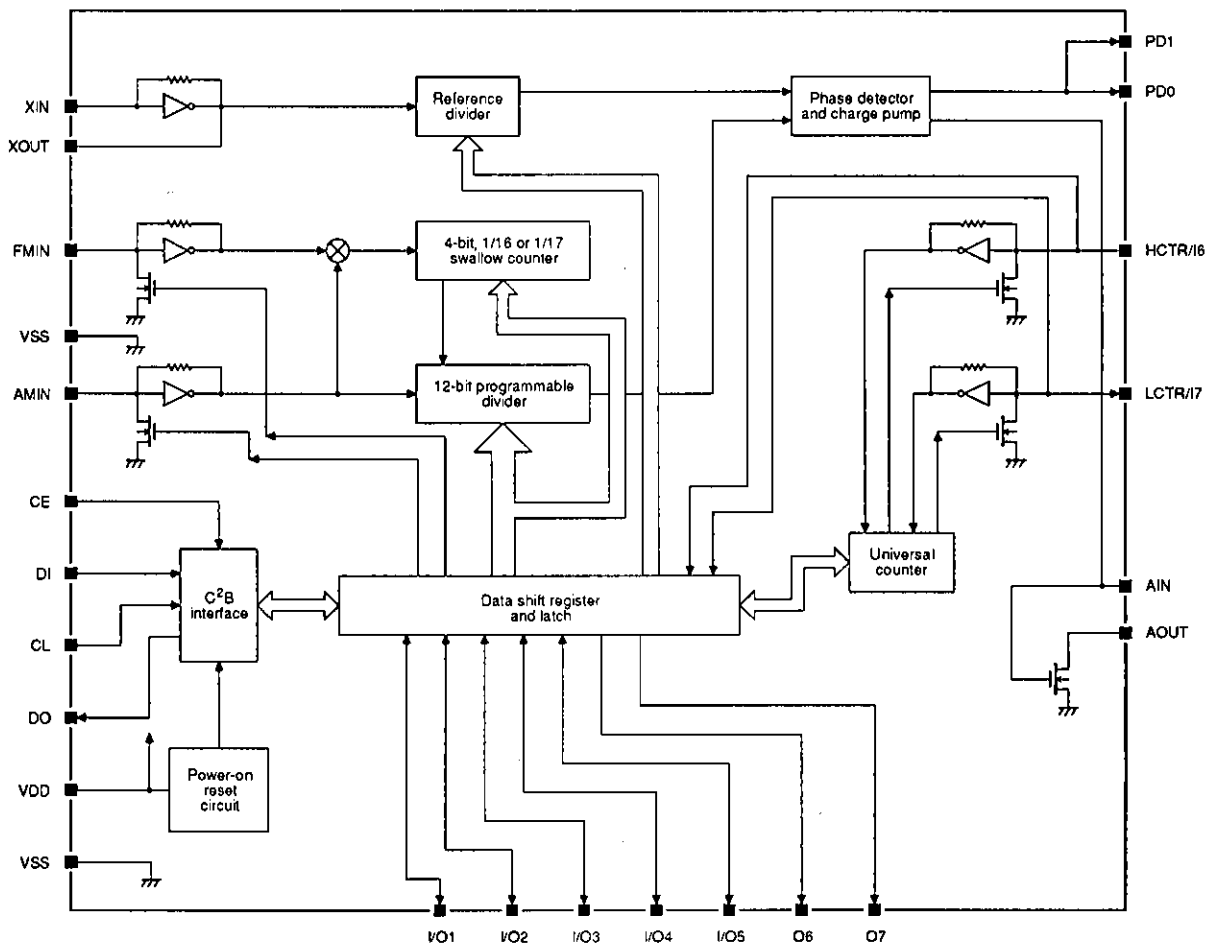


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Pin Assignment

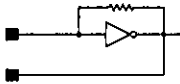

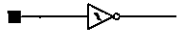
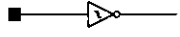
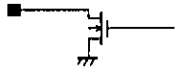
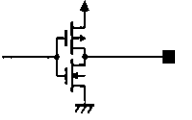
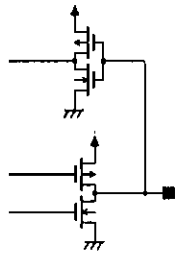
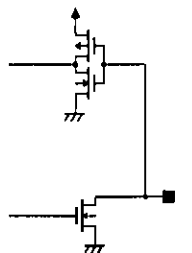
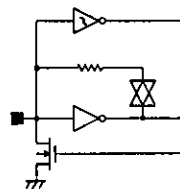


Block Diagram



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Pin Functions

Number	Name	Equivalent circuit	Function
1	XOUT		4.5 or 7.2 MHz crystal oscillator output
24	XIN		4.5 or 7.2 MHz crystal oscillator input
2	CE		Chip-enable input
3	DI		Data input from microcontroller
4	CL		Clock input
5	DO		Data output to microcontroller
6	O7		OUT7 flag output
7	O6		OUT6 flag output
8	I/O5		General-purpose input/output ports 4 and 5
9	I/O4		
10	I/O3		General-purpose input/output ports 1 to 3
11	I/O2		
12	I/O1		
13	LCTR/I7		Period or frequency measurement general-purpose counter input and input port 7

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Number	Name	Equivalent circuit	Function
14	HCTR/6		Frequency measurement general-purpose counter input and input port 6
15	VDD		Supply voltage
16	AMIN		AM band local oscillator signal input
17	FMIN		FM band local oscillator signal input
19	PD1		Phase-detector charge pump outputs
20	PD0		
21	AIN		Analog low-pass filter transistor input
22	AOUT		Analog low-pass filter transistor output
18, 23	VSS		Ground

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	-0.3 to +7.0	V
CE, CL and DI input voltage range	V_{IN1}	-0.3 to +7.0	V
I/O1 to I/O3 input voltage range	V_{IN2}	-0.3 to +15.0	V
Input voltage range for all other pins	V_{IN3}	-0.3 to $V_{DD} + 0.3$	V
DO output voltage range	V_{OUT1}	-0.3 to +7.0	V
I/O1 to I/O3 and AOUT output voltage range	V_{OUT2}	-0.3 to +15.0	V

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Parameter	Symbol	Ratings	Unit
Output voltage range for all other pins	V_{OUT3}	-0.3 to $V_{DD} + 0.3$	V
I/O4, I/O5, O6 and O7 output current range	I_{OUT1}	0 to 3.0	mA
I/O1 to I/O3, DO and AOUT output current range	I_{OUT2}	0 to 6.0	mA
Power dissipation	P_D	350 (DIP24S, $T_a \leq 85^\circ\text{C}$)	mW
		160 (MFP24S, $T_a \leq 85^\circ\text{C}$)	
Operating temperature range	T_{opr}	-40 to +85	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 to +125	$^\circ\text{C}$

Allowable Operating Ranges

$T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD1}	4.5 to 5.5	V

Electrical Characteristics

$T_a = -40$ to $+85^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5 V , $V_{SS} = 0\text{ V}$ unless otherwise noted

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{DD}	$f_{IN2} = 160\text{ MHz}$, $V_{IN2} = 100\text{ mV}$, $f_{XTAL} = 7.2\text{ MHz}$, $f_{IN4} = 25\text{ MHz}$, $V_{IN4} = 40\text{ mV}$	-	10	15	mA
		PLL inhibited, crystal oscillator running, $f_{XTAL} = 7.2\text{ MHz}$	-	0.5	-	
		PLL inhibited, crystal oscillator stopped	-	-	10	μA
CL, CE, DI, I/O1 to I/O5, HCTR/16 and LCTR/17 LOW-level input voltage	V_{IL1}		0	-	0.8	V
LCTR/17 LOW-level input voltage	V_{IL2}	Pulse wave, period measurement	0	-	0.8	V
CE, CL, DI and I/O1 to I/O3 HIGH-level input voltage	V_{IH1}		2.2	-	6.5	V
I/O4, I/O5, HCTR/16 and LCTR/17 HIGH-level input voltage	V_{IH2}		2.2	-	V_{DD}	V
LCTR/17 HIGH-level input voltage	V_{IH3}	Pulse wave, period measurement	2.2	-	V_{DD}	V
XIN rms input amplitude	V_{IN1}		0.2	-	1.5	V
FMIN rms input amplitude	V_{IN2}	$50 \leq f < 130\text{ MHz}$. See Programmable Divider section.	0.07	-	1.5	V
		$10 \leq f < 50$ and $130 \leq f \leq 160\text{ MHz}$. See Programmable Divider section.	0.10	-	1.5	

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
AMIN rms input amplitude	VIN3	2 ≤ f < 25 MHz. See Programmable Divider section.	0.04	–	1.5	V
		25 ≤ f ≤ 40 MHz. See Programmable Divider section.	0.07	–	1.5	
		0.5 ≤ f < 2.5 MHz. See Programmable Divider section.	0.04	–	1.5	
		2.5 ≤ f ≤ 10 MHz. See Programmable Divider section.	0.07	–	1.5	
HCTR/16 rms input amplitude	VIN4		0.04	–	1.5	V
LCTR/17 rms input amplitude	VIN5		0.04	–	1.5	V
PD0, PD1, I/O4, I/O5, O6 and O7 LOW-level output voltage	VOL1	IO = 1 mA	–	–	1.0	V
I/O1 to I/O3 and DO LOW-level output voltage	VOL2	IO = 5 mA	–	–	1.0	V
AOUT LOW-level output voltage	VOL3	IO = 1 mA, VAIN = 1.3 V	–	–	0.5	V
AIN LOW-level output voltage	VOL4	IO = 1 mA	–	0.7	1.5	V
PD0, PD1, I/O4, I/O5, O6 and O7 HIGH-level output voltage	VOH1	IO = 1 mA	VDD – 1.0	–	–	V
AIN HIGH-level output voltage	VOH2	IO = 1 mA	VDD – 1.5	VDD – 0.7	–	V
DO output voltage	VOU1		0	–	6.5	V
I/O1 to I/O3 and AOUT output voltage	VOU2		0	–	13	V
CE, CL and DI LOW-level input current	IIL1	VIN = 0 V	–	–	5.0	μA
I/O1 to I/O5 LOW-level input current	IIL2	VIN = 0 V	–	–	5.0	μA
HCTR/16 and LCTR/17 LOW-level input current	IIL3	VIN = 0 V	–	–	5.0	μA
XIN LOW-level input current	IIL4	VIN = 0 V	3.5	–	11	μA
FMIN, AMIN, HCTR/16 and LCTR/17 LOW-level input current	IIL5	VIN = 0 V	6.0	–	18	μA
CE, CL and DI HIGH-level input current	IIH1	VIN = 6.5 V	–	–	5.0	μA
I/O1 to I/O3 HIGH-level input current	IIH2	VIN = 13 V	–	–	5.0	μA
I/O4, I/O5, HCTR/16 and LCTR/17 HIGH-level input current	IIH3	VIN = VDD	–	–	5.0	μA
XIN HIGH-level input current	IIH4	VIN = VDD	3.5	–	11	μA
FMIN, AMIN, HCTR/16 and LCTR/17 HIGH-level input current	IIH5	VIN = VDD	6.0	–	18	μA
XIN input frequency	fIN1	Sine wave, capacitive coupling	1.0	–	8.0	MHz
FMIN input frequency	fIN2	Sine wave, capacitive coupling	10	–	160	MHz
AMIN input frequency	fIN3	Sine wave, capacitive coupling	0.5	–	40.0	MHz

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
HCTR/16 input frequency	f_{IN4}	Sine wave, capacitive coupling	0.4	-	25	MHz
LCTR/17 input frequency	f_{IN5}	Sine wave, capacitive coupling	10	-	500	kHz
		Period measurement, pulse wave, DC coupling	0.001	-	20.0	
Crystal oscillator frequency	f_{XTAL}	Crystal impedance $\leq 120 \Omega$	4.0	-	8.0	MHz
CE, CL, DI and LCTR/17 hysteresis width	V_H		-	$0.1V_{DD}$	-	V
XIN internal resistance	R_{I1}		-	1.0	-	M Ω
FMIN internal resistance	R_{I2}		-	500	-	k Ω
AMIN internal resistance	R_{I3}		-	500	-	k Ω
HCTR/16 internal resistance	R_{I4}		-	500	-	k Ω
LCTR/17 internal resistance	R_{I5}		-	500	-	k Ω
AIN sub-charge pump internal resistance	R_{IS}		-	500	-	Ω
I/O1 to I/O3 and AOUT output leakage current	I_{OFF1}	$V_O = 13 \text{ V}$	-	-	5.0	μA
DO output leakage current	I_{OFF2}	$V_O = 6.5 \text{ V}$	-	-	5.0	μA
PD0, PD1 and AIN tristate LOW-level leakage current	I_{OFFL}	$V_O = 0 \text{ V}$	-	0.01	200	nA
PD0, PD1 and AIN tristate HIGH-level leakage current	I_{OFFH}	$V_O = V_{DD}$	-	0.01	200	nA
FMIN input capacitance	C_{IN}		-	6	-	pF
DI to CL data setup time	t_{SU}		0.45	-	-	μs
DI to CL data hold time	t_{HD}		0.45	-	-	μs
CL LOW-level clock pulsewidth	t_{CL}		0.45	-	-	μs
CL HIGH-level clock pulsewidth	t_{CH}		0.45	-	-	μs
CL to CE chip enable wait time	t_{EL}		0.45	-	-	μs
CE to CL chip enable setup time	t_{ES}		0.45	-	-	μs
CL to CE chip enable hold time	t_{EH}		0.45	-	-	μs
Chip enable to data latch time	t_{LC}		-	-	0.45	μs
CL to DO data output time	t_{DC}	Depends on pull-up resistor	-	-	0.2	μs
CE to DO data output time	t_{DH}					

Functional Description

Serial Data Input

The LC72140 and LC72140M operating parameters are initialized by two 40-bit data words on the serial data input, DI, as shown in Figures 1 and 2 and Table 1.

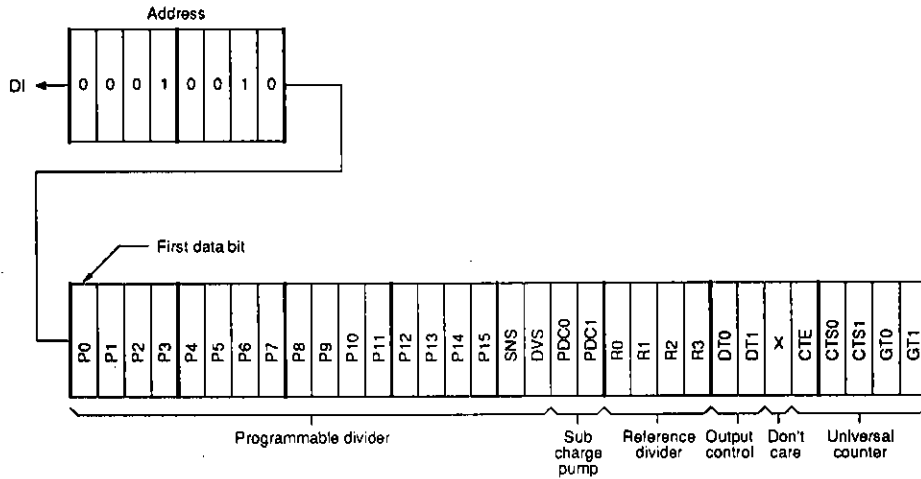


Figure 1. Input data word IN1

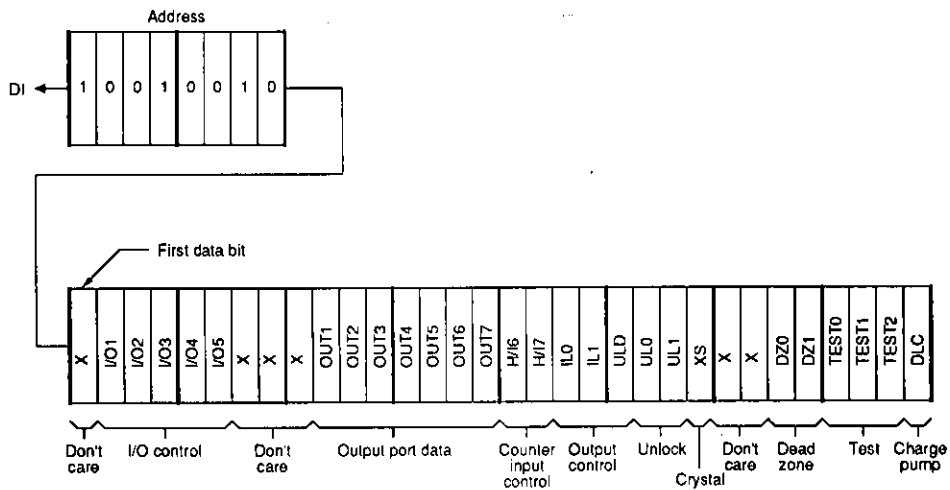


Figure 2. Input data word IN2

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Table 1. Input data functions

Name	Function	Related bits																																
<p>P0 to P15, SNS, DVS</p>	<p>Programmable divider ratio P15 is the msb. The divider ratio, frequency range and lsb are determined by the setting of the DVS and SNS flags as shown in Tables 2 and 3. P0 to P3 are ignored if P4 is the lsb.</p> <p>Table 2. Divider ratio settings</p> <table border="1" data-bbox="368 533 1236 719"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>lsb</th> <th>Divider ratio</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>×</td> <td>P0</td> <td>272 to 65535</td> </tr> <tr> <td>0</td> <td>1</td> <td>P0</td> <td>272 to 65535</td> </tr> <tr> <td>0</td> <td>0</td> <td>P4</td> <td>4 to 4095</td> </tr> </tbody> </table> <p>Note × = don't care</p> <p>Table 3. Frequency range settings</p> <table border="1" data-bbox="368 835 1236 1021"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>Input port</th> <th>Input frequency range</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>×</td> <td>FMIN</td> <td>10 to 160 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>AMIN</td> <td>2 to 40 MHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>AMIN</td> <td>0.5 to 10 MHz</td> </tr> </tbody> </table> <p>Note × = don't care</p>	DVS	SNS	lsb	Divider ratio	1	×	P0	272 to 65535	0	1	P0	272 to 65535	0	0	P4	4 to 4095	DVS	SNS	Input port	Input frequency range	1	×	FMIN	10 to 160 MHz	0	1	AMIN	2 to 40 MHz	0	0	AMIN	0.5 to 10 MHz	
DVS	SNS	lsb	Divider ratio																															
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<p>PDC0, PDC1</p>	<p>Charge pump control Bits PDC0 and PDC1 control the charge pump state as shown in Table 4. The sub-charge pump is connected to the gate of the lowpass filter transistor. This can be used in conjunction with PDO and PD1 (main charge pump) to build a fast locking PLL.</p> <p>Table 4. Charge pump state selection</p> <table border="1" data-bbox="368 1256 1236 1442"> <thead> <tr> <th>PDC0</th> <th>PDC1</th> <th>Charge pump state</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>×</td> <td>High-impedance</td> </tr> <tr> <td>1</td> <td>1</td> <td>Operating (operates continuously)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Operating (when PLL is unlocked)</td> </tr> </tbody> </table> <p>Note × = don't care</p>	PDC0	PDC1	Charge pump state	0	×	High-impedance	1	1	Operating (operates continuously)	1	0	Operating (when PLL is unlocked)	<p>UL0, UL1, DLC</p>																				
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Table 1. Input data functions—continued

Name	Function	Related bits																																																																																					
R0 to R3	Reference frequency select Bits R0 to R3 disable the PLL or select the reference frequency as shown in Table 5.																																																																																						
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	<table border="1"> <thead> <tr> <th>R₃</th> <th>R₂</th> <th>R₁</th> <th>R₀</th> <th>Reference frequency (kHz)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>100</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>50</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>25</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>25</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>12.5</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>6.25</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>3.125</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>3.125</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>10</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>9</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>5</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>3</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>30</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>PLL inhibited and crystal oscillator stopped</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>PLL inhibited</td> </tr> </tbody> </table>		R ₃	R ₂	R ₁	R ₀	Reference frequency (kHz)	0	0	0	0	100	0	0	0	1	50	0	0	1	0	25	0	0	1	1	25	0	1	0	0	12.5	0	1	0	1	6.25	0	1	1	0	3.125	0	1	1	1	3.125	1	0	0	0	10	1	0	0	1	9	1	0	1	0	5	1	0	1	1	1	1	1	0	0	3	1	1	0	1	30	1	1	1	0	PLL inhibited and crystal oscillator stopped	1	1	1	1	PLL inhibited
	R ₃		R ₂	R ₁	R ₀	Reference frequency (kHz)																																																																																	
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When the PLL is disabled, the programmable divider is stopped, AMIN and FMIN are pulled to ground, and the charge-pump outputs become high impedance.																																																																																							

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Table 1. Input data functions—continued

Name	Function	Related bits																																																						
<p>ULD, DT0, DT1, IL0, IL1</p>	<p>DO and I/O5 output control data Bits ULD, DT0, DT1, IL0 and IL1 control the mode of outputs DO and I/O5 as shown in Tables 6 and 7.</p> <p>Table 6. DO and I/O5 output flag selection</p> <table border="1" data-bbox="367 542 1244 958"> <thead> <tr> <th>ULD</th> <th>DT1</th> <th>DT0</th> <th>DO</th> <th>I/O5</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Unlock flag</td> <td rowspan="4">OUT5 flag. See Note 2.</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Open</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>End-UC flag. See note 1.</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>IN. See table 7.</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Open</td> <td rowspan="4">Unlock flag. See Note 2.</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Open</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>End-UC flag</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>IN. See table 7.</td> </tr> </tbody> </table> <p>Notes</p> <ol style="list-style-type: none"> End-UC flags that general-purpose counter operation has finished. Applicable only if I/O5 is set to be an output port.  <p>Figure 3. DO output state</p> <p>Table 7. IN state selection</p> <table border="1" data-bbox="367 1326 1244 1563"> <thead> <tr> <th>IL1</th> <th>IL0</th> <th>IN state</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Open</td> </tr> <tr> <td>0</td> <td>1</td> <td>I1 input</td> </tr> <tr> <td>1</td> <td>0</td> <td>I2 input</td> </tr> <tr> <td>1</td> <td>1</td> <td>DO goes LOW when I1 changes.</td> </tr> </tbody> </table> <p>Notes</p> <ol style="list-style-type: none"> If I/O1 or I/O2 is set to be an output port, IN becomes open. DO does not go LOW when the crystal oscillator has stopped. 	ULD	DT1	DT0	DO	I/O5	0	0	0	Unlock flag	OUT5 flag. See Note 2.	0	0	1	Open	0	1	0	End-UC flag. See note 1.	0	1	1	IN. See table 7.	1	0	0	Open	Unlock flag. See Note 2.	1	0	1	Open	1	1	0	End-UC flag	1	1	1	IN. See table 7.	IL1	IL0	IN state	0	0	Open	0	1	I1 input	1	0	I2 input	1	1	DO goes LOW when I1 changes.	<p>OUT5, I/O1, I/O2, I/O5</p>
ULD	DT1	DT0	DO	I/O5																																																				
0	0	0	Unlock flag	OUT5 flag. See Note 2.																																																				
0	0	1	Open																																																					
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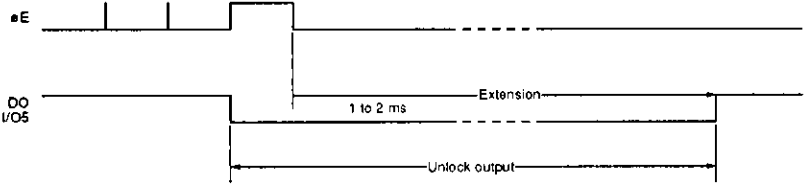
LC72140, LC72140M

Table 1. Input data functions—continued

Name	Function	Related bits																																																				
<p>CTS0, CTS1, CTE, GT0, GT1</p>	<p>Counter control Bits CTS0 and CTS1 select the counter input as shown in Table 8.</p> <p>Table 8. Counter input and measurement mode selection</p> <table border="1" data-bbox="363 510 1240 719"> <thead> <tr> <th>Switch</th> <th>CTS1</th> <th>CTS0</th> <th>Input</th> <th>Measurement mode</th> <th>Frequency range</th> <th>Input rms sensitivity</th> </tr> </thead> <tbody> <tr> <td>S1</td> <td>1</td> <td>×</td> <td>HCTR</td> <td>Frequency</td> <td>0.4 to 25.0 MHz</td> <td>40 mV</td> </tr> <tr> <td>S2</td> <td>0</td> <td>1</td> <td>LCTR</td> <td>Frequency</td> <td>10 to 500 kHz</td> <td>40 mV</td> </tr> <tr> <td>S3</td> <td>0</td> <td>0</td> <td>LCTR</td> <td>Period</td> <td>1 Hz to 20 kHz</td> <td>(Pulse)</td> </tr> </tbody> </table> <p>Note × = don't care</p> <p>Bit CTE starts the counter when 1, and resets the counter, when 0. Bits GT0 and GT1 select the measurement time in frequency measurement mode or the number of periods to count in period measurement mode as shown in Table 9.</p> <p>Table 9. Measurement duration selection</p> <table border="1" data-bbox="363 925 1240 1227"> <thead> <tr> <th rowspan="2">GT1</th> <th rowspan="2">GT0</th> <th colspan="2">Frequency measurement</th> <th>Period measurement</th> </tr> <tr> <th>Measurement duration (ms)</th> <th>Wait time (ms)</th> <th>Cycles</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>4</td> <td rowspan="2">3 to 4</td> <td rowspan="2">1</td> </tr> <tr> <td>0</td> <td>1</td> <td>8</td> </tr> <tr> <td>1</td> <td>0</td> <td>32</td> <td rowspan="2">7 to 8</td> <td rowspan="2">2</td> </tr> <tr> <td>1</td> <td>1</td> <td>64</td> </tr> </tbody> </table>	Switch	CTS1	CTS0	Input	Measurement mode	Frequency range	Input rms sensitivity	S1	1	×	HCTR	Frequency	0.4 to 25.0 MHz	40 mV	S2	0	1	LCTR	Frequency	10 to 500 kHz	40 mV	S3	0	0	LCTR	Period	1 Hz to 20 kHz	(Pulse)	GT1	GT0	Frequency measurement		Period measurement	Measurement duration (ms)	Wait time (ms)	Cycles	0	0	4	3 to 4	1	0	1	8	1	0	32	7 to 8	2	1	1	64	<p>H/16, L/17</p>
Switch	CTS1	CTS0	Input	Measurement mode	Frequency range	Input rms sensitivity																																																
S1	1	×	HCTR	Frequency	0.4 to 25.0 MHz	40 mV																																																
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GT1	GT0	Frequency measurement		Period measurement																																																		
		Measurement duration (ms)	Wait time (ms)	Cycles																																																		
0	0	4	3 to 4	1																																																		
0	1	8																																																				
1	0	32	7 to 8	2																																																		
1	1	64																																																				
<p>I/O1 to I/O5</p>	<p>Input/output port control Bits I/O1 to I/O5 set the direction of the ports. Each pin is an input when the corresponding bit is 0, and an output, when the bit is 1. All ports are set to be inputs after power-ON reset.</p>	<p>OUT1 to OUT5, ULD</p>																																																				
<p>OUT1 to OUT7</p>	<p>Output port data Bits OUT1 to OUT7 set the output values of the O1 to O7 output ports. Each output is open or HIGH when the corresponding bit is 1, and LOW, when the bit is 0. A bit is ignored if the corresponding port is an input port or the unlock output.</p>	<p>I/O1 to I/O5, ULD</p>																																																				
<p>H/16, L/17</p>	<p>Counter input control Bits H/16 and L/17 select the operation of the HCTR/16 and LCTR/17 pins. When H/16 is 0, HCTR/16 is an input port, and when H/16 is 1, HCTR/16 is the HCTR input. When L/17 is 0, LCTR/17 is an input port, and when L/17 is 1, LCTR/17 is the LCTR input.</p>	<p>CTS0, CTS1</p>																																																				

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Table 1. Input data functions—continued

Name	Function	Related bits																				
UL0, UL1	<p>PLL unlock detect control Bits UL0 and UL1 select the phase error threshold and extension (ϕ_E) used to detect the PLL unlocked state as shown in Table 10 and Figure 4. When the phase error is greater than the selected error, the PLL unlock detector output goes LOW.</p> <p>Table 10. Unlock detection and extension selection</p> <table border="1" data-bbox="368 562 1240 792"> <thead> <tr> <th>UL1</th> <th>UL0</th> <th>Phase error</th> <th>Detector output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Stopped</td> <td>Open</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>ϕ_E output</td> </tr> <tr> <td>1</td> <td>0</td> <td>$\pm 0.56 \mu\text{s}$</td> <td>ϕ_E with 1 to 2 ms extension</td> </tr> <tr> <td>1</td> <td>1</td> <td>$\pm 1.11 \mu\text{s}$</td> <td>ϕ_E with 1 to 2 ms extension</td> </tr> </tbody> </table>  <p>Figure 4. Phase-error extension</p>	UL1	UL0	Phase error	Detector output	0	0	Stopped	Open	0	1	0	ϕ_E output	1	0	$\pm 0.56 \mu\text{s}$	ϕ_E with 1 to 2 ms extension	1	1	$\pm 1.11 \mu\text{s}$	ϕ_E with 1 to 2 ms extension	ULD, DT0, DT1
UL1	UL0	Phase error	Detector output																			
0	0	Stopped	Open																			
0	1	0	ϕ_E output																			
1	0	$\pm 0.56 \mu\text{s}$	ϕ_E with 1 to 2 ms extension																			
1	1	$\pm 1.11 \mu\text{s}$	ϕ_E with 1 to 2 ms extension																			
XS	<p>Crystal oscillator control Bit XS selects the oscillator frequency. When XS is 1, the frequency is 7.2 MHz, and when XS is 0, 4.5 MHz. 4.5 MHz is selected after power-ON reset.</p>																					
DZ0, DZ1	<p>Phase comparator control Bits DZ0 and DZ1 select the phase comparator insensitive band, or dead zone.</p> <p>Table 11. Insensitive band mode selection</p> <table border="1" data-bbox="368 1384 1240 1615"> <thead> <tr> <th>DZ1</th> <th>DZ0</th> <th>Insensitive band (dead zone) mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>DZA</td> </tr> <tr> <td>0</td> <td>1</td> <td>DZB</td> </tr> <tr> <td>1</td> <td>0</td> <td>DZC</td> </tr> <tr> <td>1</td> <td>1</td> <td>DZD</td> </tr> </tbody> </table> <p>DZA is selected after power-ON reset.</p>	DZ1	DZ0	Insensitive band (dead zone) mode	0	0	DZA	0	1	DZB	1	0	DZC	1	1	DZD						
DZ1	DZ0	Insensitive band (dead zone) mode																				
0	0	DZA																				
0	1	DZB																				
1	0	DZC																				
1	1	DZD																				
DLC	<p>Charge pump control Bit DLC controls the charge pump operation. When DLC is 1, the charge pump outputs are forced to LOW, and when DLC is 0, the charge pump operates normally. This feature can be useful to remove the PLL from a deadlock state. The PLL can deadlock if its VCO control voltage V_{tune} becomes 0 V, halting the VCO. Setting DLC to 1 sets V_{tune} to V_{cc}, restarting the VCO. Normal operating mode is selected after power-ON reset.</p>																					
TEST0 to TEST2	<p>Test data Bits TEST0 to TEST2 are used for in-factory device testing. Set them all to 0. They are set to zero after a power-ON reset.</p>																					

Serial Data Input Timing

The timing for the serial data input words is shown in Figure 5. The first eight bits are the mode select bits.

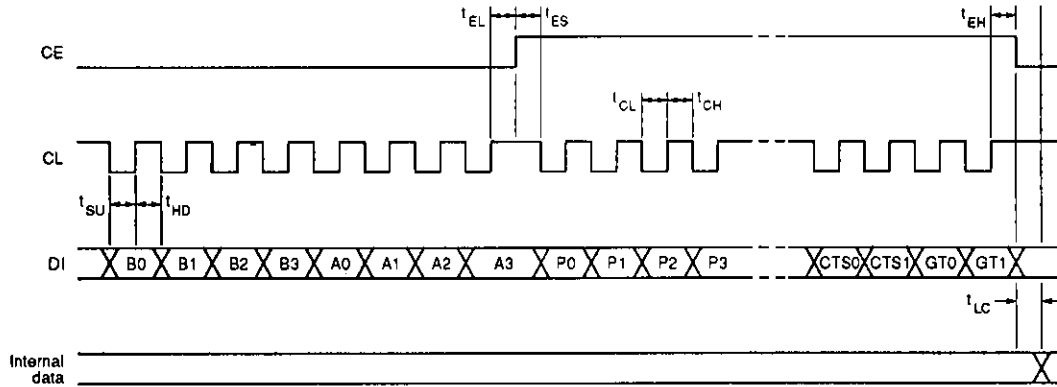


Figure 5. Input timing

Notes

1. t_{SU} , t_{HD} , t_{EL} , t_{ES} , t_{CL} , t_{CH} and t_{EH} > 0.45 μ s
2. t_{LC} < 0.45 μ s

Serial Data Output

The 40-bit data word output on DO has the format and functions as shown in Figure 6 and Table 12, respectively.

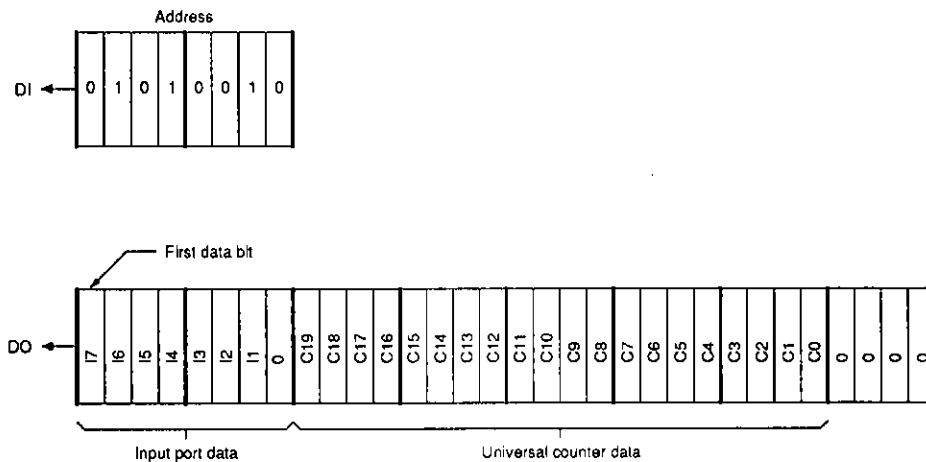


Figure 6. Output data word OUT

Table 12. Input data functions

Name	Function	Related bits
I1 to I7	Input port data Bits I1 to I7 reflect the data latched into each input port when the device changes to data output mode. I6 and I7 are zero when the corresponding port is a counter input. I1 to I5 correspond to the I/O1 to I/O5 ports, and I6 and I7, to the HCTR/I6 and LCTR/I7 inputs, respectively.	I/O1 to I/O5, H/I6, L/I7
C0 to C19	Counter contents Bits C0 to C19 are the latched contents of the 20-bit binary counter. C0 is the lsb.	CTS0, CTS1, CTE

Serial Data Output Timing

The timing for the serial data output is shown in figure 7. The first eight bits are the mode select bits.

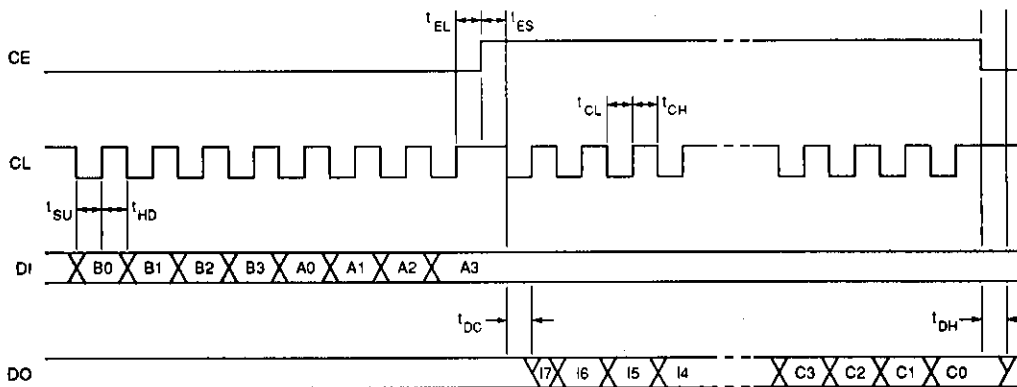


Figure 7. Output timing

Notes

1. t_{SU} , t_{HD} , t_{EL} , t_{ES} , t_{CL} and t_{CH} > 0.45 μ s
2. t_{DC} and t_{DH} < 0.2 μ s
3. Since DO is an open-drain output, the data transition time depends on the value of the pull-up resistor.
4. DO is normally open.

Serial Data Input/Output Mode Selection

The LC72140 and LC72140M use the C²B (computer control bus) serial data format. The first 8 bits form the

address, shown in Figure 8, used to select the mode of operation as shown in Table 13.

Table 13. Serial data input/output mode selection

Input/output mode	Address								Description
	B0	B1	B2	B3	A0	A1	A2	A3	
IN1	0	0	0	1	0	0	1	0	32-bit control data input
IN2	1	0	0	1	0	0	1	0	32-bit control data input
OUT	0	1	0	1	0	0	1	0	Output data. Data is output if the clock is active.

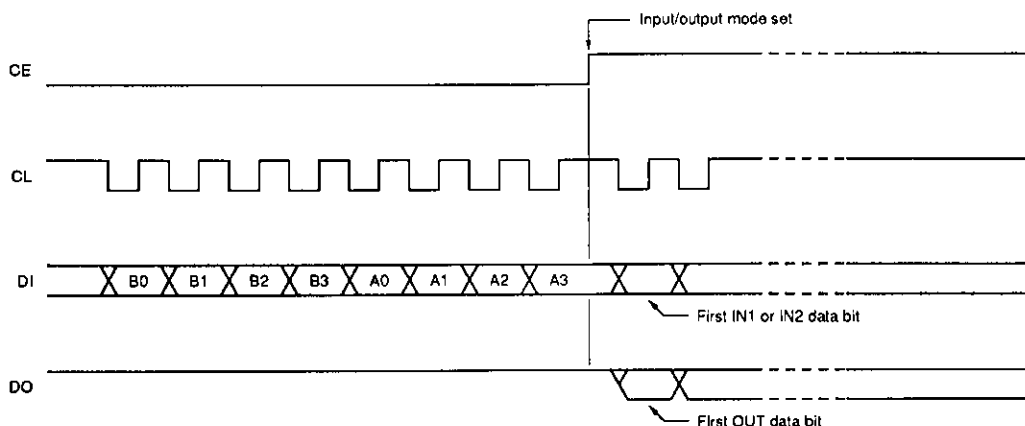


Figure 8. Mode selection address bits

Programmable Divider

The configuration of the programmable divider is shown in Figure 9. The input mode selection is shown in Table 14, and the input sensitivity, in Table 15.

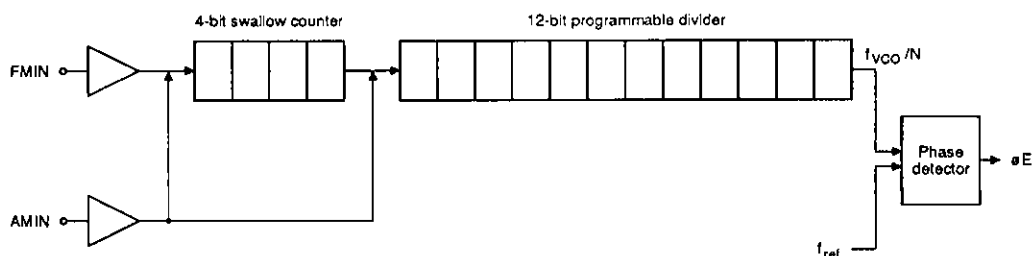


Figure 9. Programmable divider

Table 14. Programmable divider selection

DVS	SNS	1/16 and 1/17 pulse swallower	12-bit programmable divider	Input port
1	×	✓	✓	FMIN
0	1	✓	✓	AMIN
0	0	-	✓	AMIN

Note

× = don't care

Table 15. Input sensitivity

DVS	SNS	Input	Frequency (MHz)	Input rms sensitivity (mV)
1	×	FMIN	$10 \leq f < 50$	100
			$50 \leq f < 130$	70
			$130 \leq f < 160$	100
0	1	AMIN	$2 \leq f < 25$	40
			$25 \leq f < 40$	70
0	0	AMIN	$0.5 \leq f < 2.5$	40
			$2.5 \leq f < 10$	70

Note

× = don't care

General-purpose Counter

The 20-bit general-purpose counter is used for both frequency and period measurement as shown in Figure 10. The measurement mode is selected by bits CTS0 and CTS1. The counter contents, C, in frequency measurement mode are given by

$$C = FIF \times GT$$

and in period measurement mode by

$$C = \left(\frac{1}{T}\right) + 900 \text{ kHz}$$

The counter contents are output on DO, msb first.

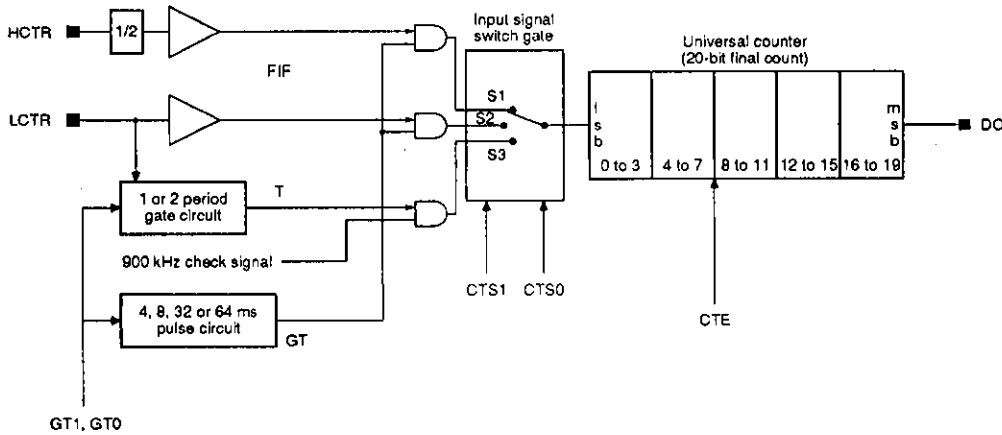


Figure 10. General-purpose counter

The LCTR signal is passed directly to the counter input. The HCTR signal is passed through a divide-by-two prescaler. The actual HCTR frequency is, therefore, two

times the measured frequency. The timing for the general-purpose counter is shown in Figure 11.

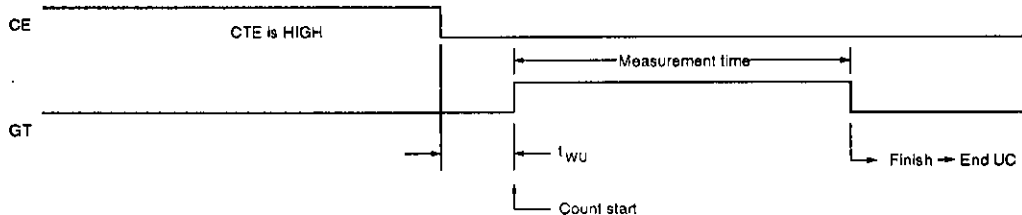


Figure 11. General-purpose counter timing

Note

t_{wu} = wait time

The counter starts when the CTE flag is set. The serial input data is latched in on the falling edge of CE. Note that the HCTR or LCTR input signal should be input within the wait time of this transition.

The period or frequency count should be read while CTE is set to 1, because the counter is reset when CTE is set to 0. Note that CTE should be set to 0 before each measurement.

In IF count mode, the IF IC's SD (station detector) signal presence is determined by the microcontroller and if an SD signal is present, the IF count buffer output turns ON and IF count becomes active. During auto-search in IF count only, there is a possibility of the count stopping even when there is no station present due to the IF count buffer output leakage.

Integrating count

When integrating the count, the count value is added to the general-purpose counter as shown in Figure 12. However, the counter can overflow. The maximum

count is $2^{20} - 1$, or FFFFF in hexadecimal. DO can also be used to monitor for frequency or period measurement completion as shown in Figure 12.

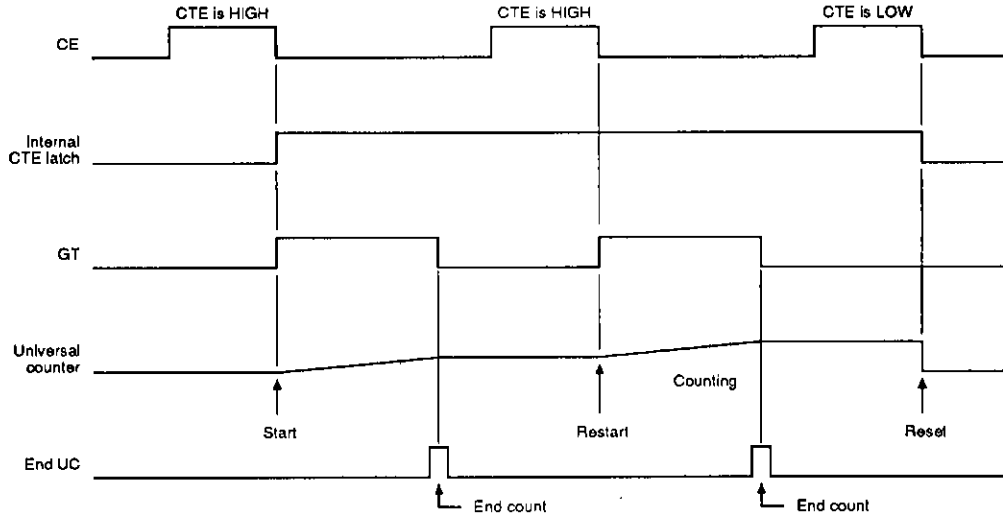


Figure 12. Integrating count timing

Charge Pump

The charge pump configuration is shown in Figure 13.

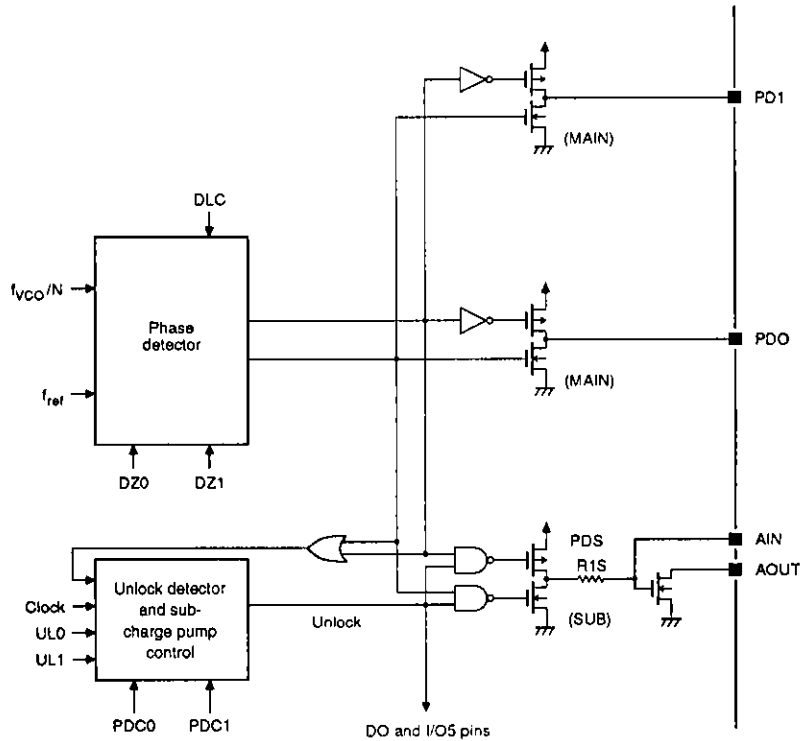


Figure 13. Charge pump

When unlock is detected following a channel change, PDS (the sub-charge pump) operates. The value of R1 changes to $R1M||R1S$ ($R1S \cong 500 \Omega$), as shown in Figure 14, decreasing the low-pass filter time-constant and accelerating PLL locking.

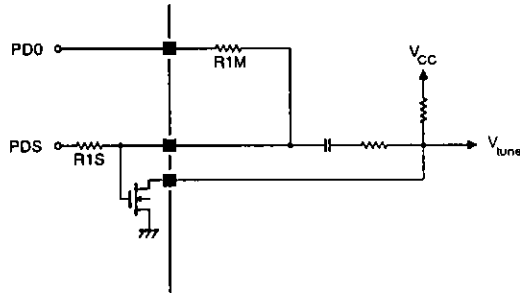


Figure 14. Charge pump connections

The local oscillator signal is divided by N. When the frequency of the divided signal is higher than the reference frequency, PD0 and PD1 are HIGH, and when lower, they are LOW. Both outputs are floating when the two signals are equal in frequency.

Pin States After Power-ON Reset

The state of the input/output ports after power-ON reset is shown in Table 16.

Table 16. Power-ON reset states

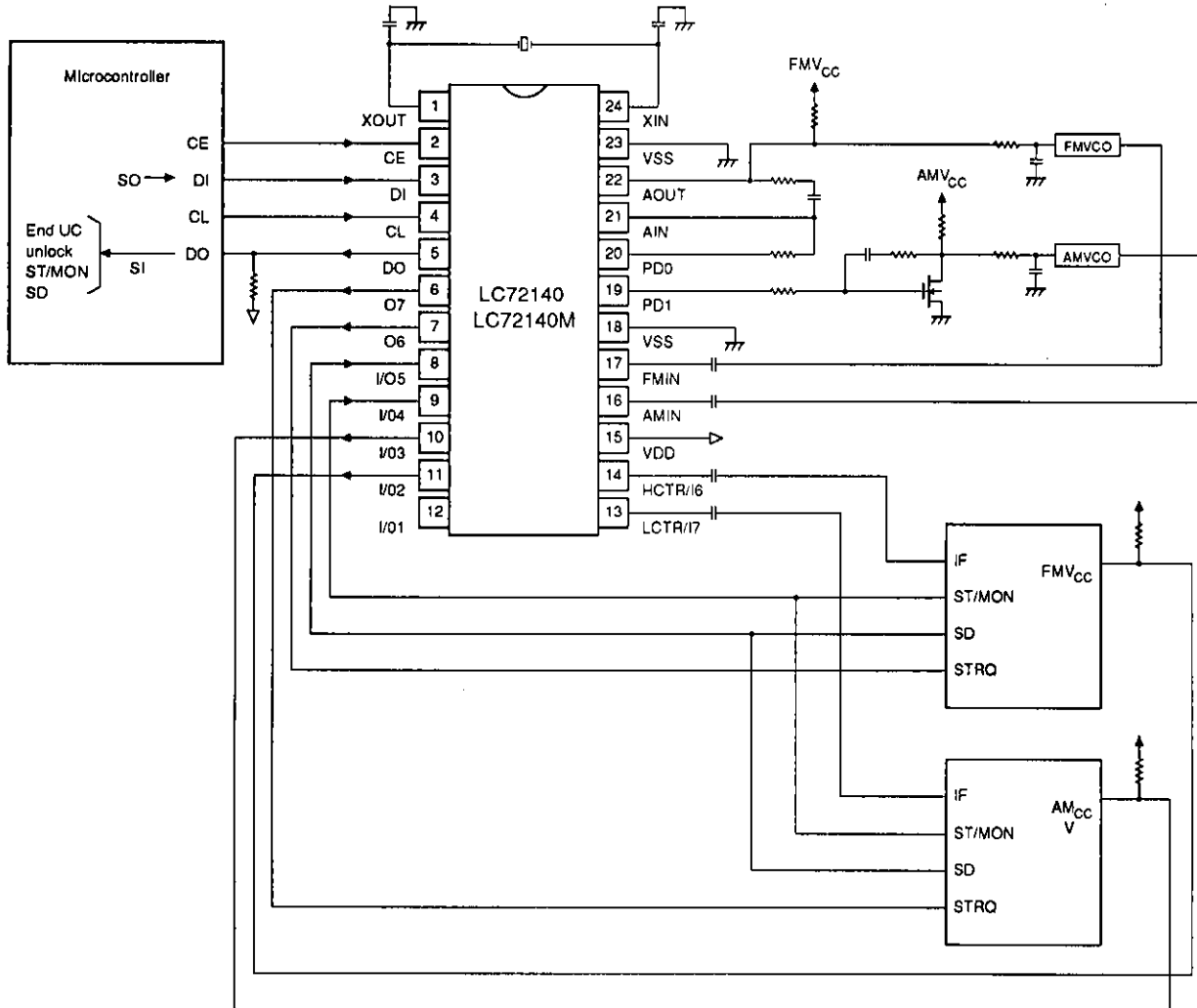
Pin	Reset state	Pin type
I/O1	I1	Open-drain
I/O2	I2	Open-drain
I/O3	I3	Open-drain
I/O4	I4	CMOS
I/O5	I5	CMOS
O6	O6	CMOS
O7	O7	CMOS
HCTR/16	16	
LCTR/17	17	

Notes

- Phase comparator control**
 Modes DZA and DZB do not have insensitive bands (dead zones) and, therefore, the charge pump operates continuously. Consequently, measures should be taken to ensure reference frequency sidebands do not occur.
 Modes DZC and DZD do have insensitive bands. Consequently, measures should be taken to ensure phase noise is not generated.
- FMIN, AMIN, HCTR and LCTR**
 These inputs should each be capacitively coupled using a 50 to 100 pF capacitor. Also, these capacitors should be mounted as close as possible to their respective inputs.
- IF counting using HCTR or LCTR**
 The LC72140 and LC72140M can perform IF count tuning when connected to an SD (station detector) signal from an IF IC. IF counting should start when the SD signal becomes active.
- Using the general-purpose counter**
 In IF count mode, the IF IC's SD (station detector) signal presence is determined by the microcontroller and if an SD signal is present, the IF count buffer output turns ON and IF count becomes active. During auto-search in IF count only, there is a possibility of the count stopping even when there is no station present due to the IF count buffer output leakage.

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Typical Application



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
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