Ordering number: EN 3584B

Silicon-gate CMOS LSI

# LC7215, 7215F, 7215FM

## MW/LW PLL Frequency Synthesizers

## Overview

The LC7215, LC7215F and LC7215FM are phase-locked-loop frequency synthesizer LSIs that provide accurate reference frequencies over the MW and LW bands, making them ideally suited for AM tuners.

## Features

- PLL frequency synthesizer LSIs for MW and LW bands.
- Reference frequencies of 1, 5, 9 and 10 kHz.
- On-chip transistor for the low-pass filter amplifier.
- Single output pin (CMOS output)
- Controller clock output pin.
- Time-base output pin.
- All devices can be used for double conversion demodulation.
- The LC7215F and 7215FM have expanded input frequency ranges.

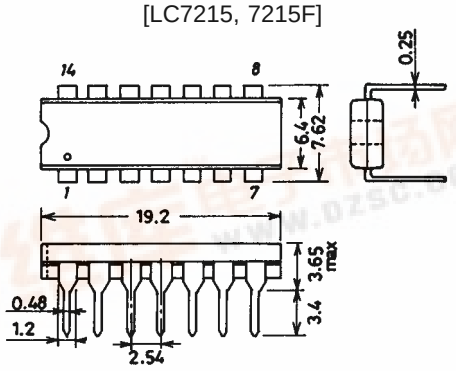
| | | |
|---|---|---|
| LC7215 | 0.5 to 13 MHz | : (DIP14) |
| LC7215F/FM | 0.5 to 20 MHz | : (DIP14/MFP14S) |

## Package Dimensions

unit : mm

### 3003A-DIP14

[LC7215, 7215F]

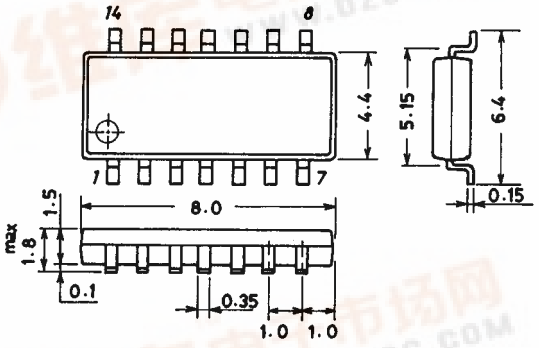



SANYO : DIP14

unit : mm

### 3111-MFP14S

[LC7215FM]




SANYO : MFP14S



SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

# Specifications

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

Values in parentheses are for the LC7215F and LC7215FM.

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | –0.3 to +6.5 | V |
| Input voltage | $V_{IN}1$ | All input pins | –0.3 to $V_{DD}$ +0.3 | V |
| | $V_{IN}2$ | CE, CL, DATA | (Note) –0.3 to +6.5 | V |
| Output current | $I_{OUT}$ | AOUT | 0 to 5 | mA |
| Output voltage | $V_{OUT}1$ | AOUT | –0.3 to +15 | V |
| | $V_{OUT}2$ | $\overline{SYC}$, $\overline{TB}$ | –0.3 to +6.5 | V |
| | $V_{OUT}3$ | All output pins except $V_{OUT}1$ and $V_{OUT}2$ | –0.3 to $V_{DD}$ +0.3 | V |
| Allowable power dissipation | Pd max | Ta ≦ 85°C | 150 | mW |
| Operating temperature | Topr | | –40 to +85 | °C |
| Storage temperature | Tstg | | –55 to +125 | °C |

Note: Voltage that is applied to the resistors when resistors totaling at least 10 kΩ are connected to a pin in series.

## Allowable Operating Conditions at $V_{SS}$ = 0 V

Values in parentheses are for the LC7215F and LC7215FM.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}1$ | $V_{DD}$ | (4.5)3.0 | | (5.5)5.5 | V |
| | $V_{DD}2$ | $V_{DD}$ (Crystal OSC oscillation guaranteed) | 3.0 | | 5.5 | V |
| High-level input voltage | $V_{IH}$ | CE, CL, DATA | 2.0 | | $V_{DD}1$ | V |
| Low-level input voltage | $V_{IL}$ | CE, CL, DATA | 0 | | 0.5 | V |
| Output voltage | $V_{OUT}1$ | AOUT | | | 13 | V |
| | $V_{OUT}2$ | $\overline{SYC}$, $\overline{TB}$ | | | 5.5 | V |
| Input frequency | $f_{IN}1$ | PIN: Sine wave, capacitive coupling $V_{DD}1$, *S = 1 | (2.3)2.3 | | (20)13 | MHz |
| | $f_{IN}2$ | PIN: Sine wave, capacitive coupling $V_{DD}1$, *S = 0 | 0.5 | | 2.5 | MHz |
| Oscillation guaranteed crystal oscillator | X'tal | XIN, XOUT: CI ≦ 30 Ω | 8.00 | 11.16 | 12.00 | MHz |
| Input amplitude | $V_{IN}1$ | PIN: Square wave, capacity connection $V_{DD}1$, *S = 1 | 100 | | 1000 | mVrms |
| | $V_{IN}2$ | PIN: Square wave, capacity connection $V_{DD}1$, *S = 0 | 100 | | 1000 | mVrms |
| Power supply | — | $V_{DD}$, $V_{SS}$: A capacitor of at least 1000 pF must be inserted. | 1000 | | | pF |

## Electrical Characteristics within the allowable operating ranges

Values in parentheses are for LC7215F and LC7215FM.

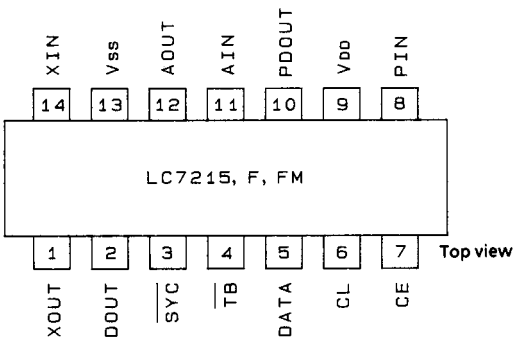
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| High-level input currents | $I_{IH}1$ | XIN: $V_I = V_{DD}$ | | | 20 | µA |
| | $I_{IH}2$ | PIN: $V_I = V_{DD}$ | | | 40 | µA |
| | $I_{IH}3$ | CE, CL, DATA: $V_I = V_{DD}$ | | | 3.0 | µA |
| | $I_{IH}4$ | AIN: $V_I = V_{DD}$ | | 0.01 | 1.0 | µA |
| Low-level input currents | $I_{IL}1$ | XIN: $V_I = V_{SS}$ | | | 20 | µA |
| | $I_{IL}2$ | PIN: $V_I = V_{SS}$ | | | 40 | µA |
| | $I_{IL}3$ | CE, CL, DATA: $V_I = V_{SS}$ | | | 3.0 | µA |
| | $I_{IL}4$ | AIN: $V_I = V_{SS}$ | | 0.01 | 1.0 | µA |
| High-level output voltages | $V_{OH}1$ | DOUT: $I_O$ = 1 mA | $V_{DD}$ –1.0 | | | V |
| | $V_{OH}2$ | PDOUT: $I_O$ = 0.5 mA | $V_{DD}$ –1.0 | | | V |
| Low-level output voltages | $V_{OL}1$ | DOUT: $I_O$ = –1 mA | | | 1.0 | V |
| | $V_{OL}2$ | PDOUT: $I_O$ = –0.5 mA | | | 1.0 | V |
| | $V_{OL}4$ | $\overline{SYC}$, $\overline{TB}$: $I_O$ = 0.5 mA | | | 1.0 | V |
| | $V_{OL}5$ | AOUT: $I_O$ = 1 mA | | | 1.0 | V |
| Output off-state leakage currents | $I_{OFF}1$ | $\overline{SYC}$, $\overline{TB}$: $V_O = V_{DD}$ | | | 3.0 | µA |
| | $I_{OFF}2$ | AOUT: $V_O$ = 13 V | | | 5.0 | µA |
| Tristate output High-level off-state leakage current | $I_{OFF}H$ | PDOUT: $V_O = V_{DD}$ | | 0.01 | 1.0 | nA |
| Tristate output Low-level off-state leakage current | $I_{OFF}L$ | PDOUT: $V_O = V_{SS}$ | | 0.01 | 1.0 | nA |
| High-level output voltage | $V_{OH}3$ | XOUT: $I_O$ = –0.1 mA | $V_{DD}$ –1.0 | | | V |
| Low-level output voltage | $V_{OL}3$ | XOUT: $I_O$ = 0.1 mA | | | 1.0 | V |
| Supply current | $I_{DD}1$ | $V_{DD}$: $f_{IN}1$ = 13 MHz, *S = 1 (High speed) (Note 1) | | | 10 | mA |
| | | $f_{IN}1$ = 20 MHz, *S = 1 (High speed) (Note 1) | | | (12) | mA |
| | $I_{DD}2$ | $V_{DD}$: $f_{IN}1$ = 2.5 MHz, *S = 0 (Low speed) (Note 1) | | | 5 | mA |
| | $I_{DD}3$ | $V_{DD}$: $V_{DD}$ = 5.5 V, *O = 0, P = 1 (Note 2) | | 1.2 | 2.0 | mA |
| | | $V_{DD}$ = 4.5 V, *O = 0, P = 1 (Note 2) | | 0.7 | 1.5 | mA |
| | | $V_{DD}$ = 3.0 V, *O = 0, P = 1 (Note 2) | | 0.4 | 1.0 | mA |

* S, O and P are serial control bits.

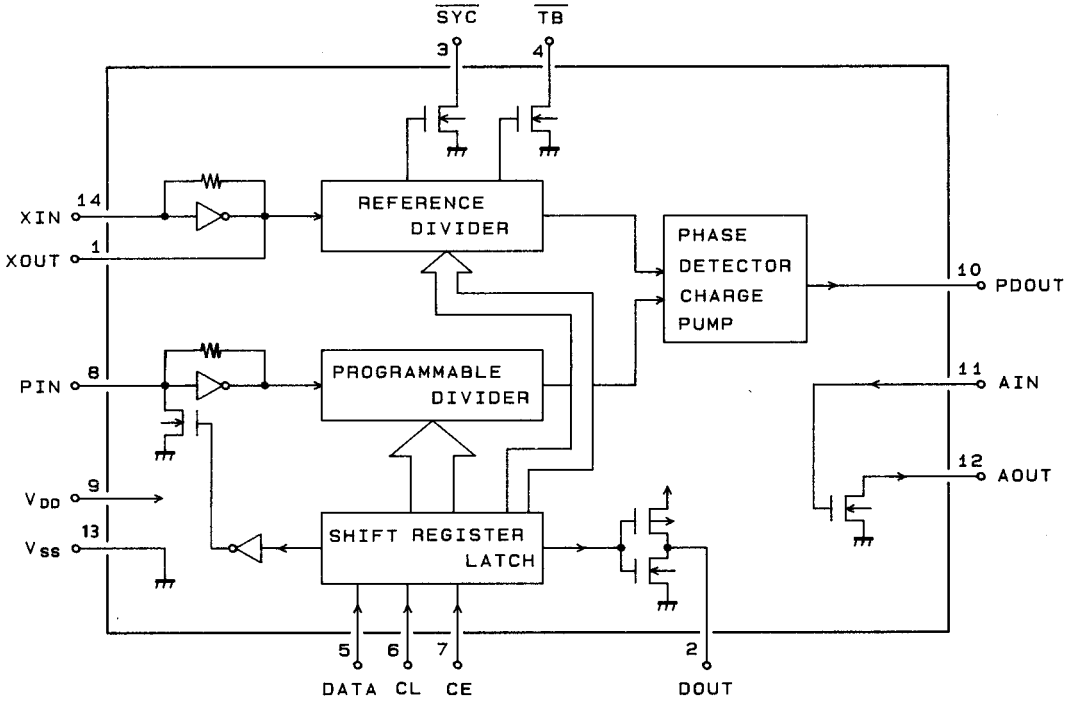
Note 1. $V_{IN}1 = V_{IN}2$ = 100 mVms. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to $V_{SS}$ and all other outputs are open.

2. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to $V_{DD}$ and all other outputs are open. (Backup mode when PLL is halted.)

## Pin Assignment



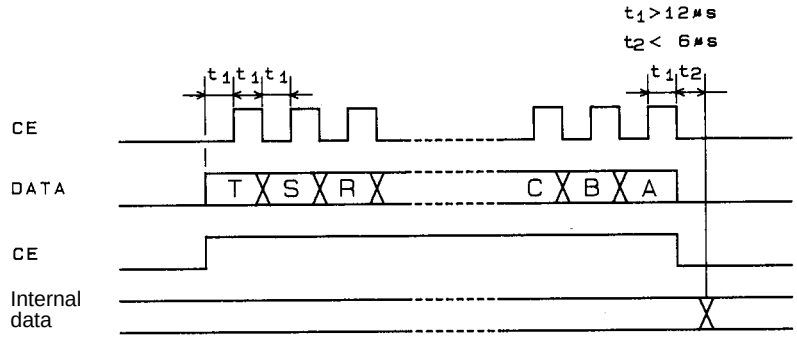
## Block Diagram

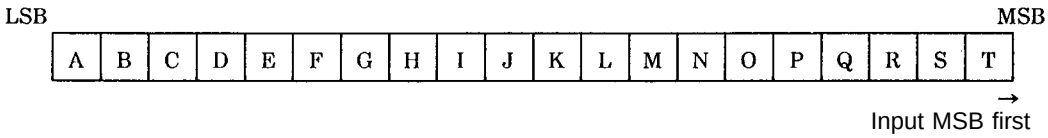



## Pin Description

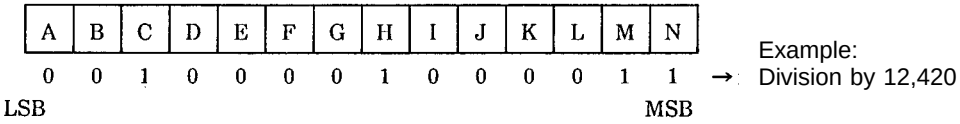
| Name | Description |
|---|---|
| XIN, XOUT | 11.16 MHz crystal oscillator connection, feedback resistance built-in |
| PIN | Local oscillator signal input |
| $V_{DD}$, $V_{SS}$ | Power supply |
| DATA, CL, CE | Data input |
| DOUT | Single bit data output |
| AIN, AOUT | Low-pass filter amplifier |
| PDOUT | Charge pump output |
| $\overline{TB}$ | 8 Hz time-base output |
| $\overline{SYC}$ | 60 kHz controller clock output |

## Data Input




(1) A to N: Divider data




(2) O, P: Mode selection

| Mode | O | P | DOUT | $\overline{TB}$ | Operation |
|---|---|---|---|---|---|
| NOR1 | 0 | 0 | T | 8 Hz | Normal operation (with PLL operating) |
| NOR2 | 0 | 1 | T | 8 Hz | Normal operation (backup when PLL is halted) |
| TEST1 | 1 | 0 | (Device test mode) | | |
| TEST2 | 1 | 1 | (Device test mode) | | |

(3) Q, R: Reference frequency selection

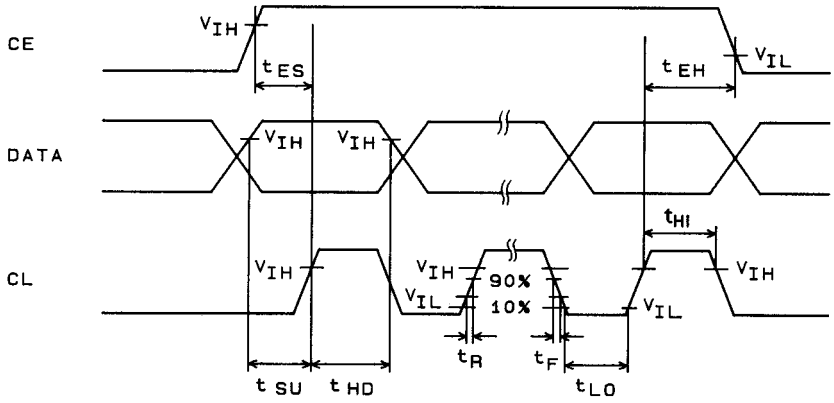
| Q | R | Reference frequency |
|---|---|---|
| 0 | 0 | 9 kHz |
| 0 | 1 | 10 kHz |
| 1 | 0 | 1 kHz |
| 1 | 1 | 5 kHz |

(4) S: Programmable divider input sensitivity switch
S = 1: for High speed
S = 0: for Low speed

(5) T: Output to DOUT
T = 1: DOUT = 1
T = 0: DOUT = 0

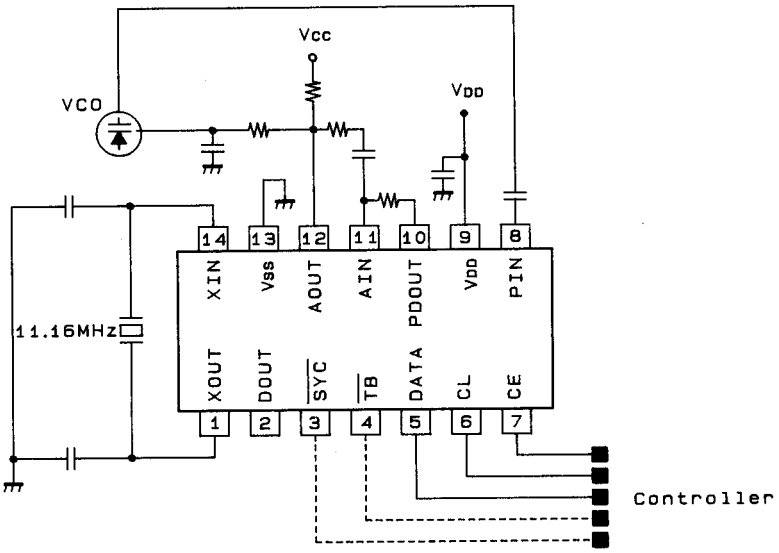
## Data Input Timing

$V_{IH}$ = 2.0 to $V_{DD}$, $V_{IL}$ = 0 to 0.5 V
X'tal = 8.00 to 11.16 (typ) to 12.00 MHz
Data latch: Rising edge of CL




| Item | Symbol | 11.16 MHz crystal | Other crystal frequencies | Effective value |
|---|---|---|---|---|
| Enable setup time | $t_{ES}$ | At least 12 µs | At least 2 × (1/fXtal × 62) | 1/2 of the value shown at left |
| Enable hold time | $t_{EH}$ | ↑ | ↑ | |
| Data setup time | $t_{SU}$ | ↑ | ↑ | |
| Data hold time | $t_{HD}$ | ↑ | ↑ | |
| Clock Low-level time | $t_{LO}$ | ↑ | ↑ | |
| Clock High-level time | $t_{HI}$ | ↑ | ↑ | |
| Rise time | $t_R$ | 1 µs or less | 1 µs or less | |
| Fall time | $t_F$ | ↑ | ↑ | |

## (1) Sample Application Circuit




## (2) Double-conversion Receiver