CMOS LSI

SANYO No. 3355A

LC7216M

PLL Frequency Synthesizer for Electronic Tuning

Features

Various reference frequencies, input/output ports, and a universal counter, and unlock detector.

(1) Programmable divider
- FMIN pin: 130MHz: 70mVrms/160MHz: 110mVrms input (Prescaler built-in)
- AMIN pin: Pulse swallow and direct frequency-divide method.

(2) Reference frequency: 10 user selectable reference frequencies.
100, 50, 25, 12.5, 6.25, 3.125, 10, 9, 5, and 1kHz

(3) Output port: 5 ports
2 complementary outputs
3N-channel open drain outputs

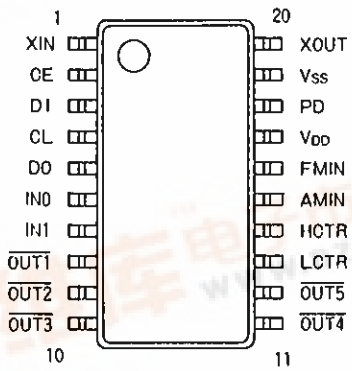
(4) Input port: 2 ports

(5) Universal counter: Used to measure IF signals, etc. (The IF signals counting must be sure to use together with the SD (Station Detect) signals from IF-IC.)
- HCTR pin: For frequency measurement (>70MHz input capable)
- LCTR pin: For frequency or period measurement

(6) Unlock detection for PLL: 0.55, 1.11, 2.22, 3.33 μsec phase difference

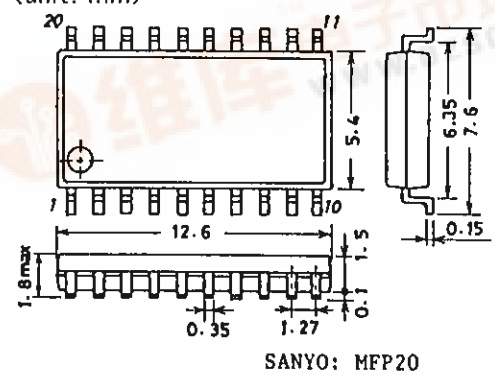
(7) Package: MFP20 (Miniflat)

Pin Assignment



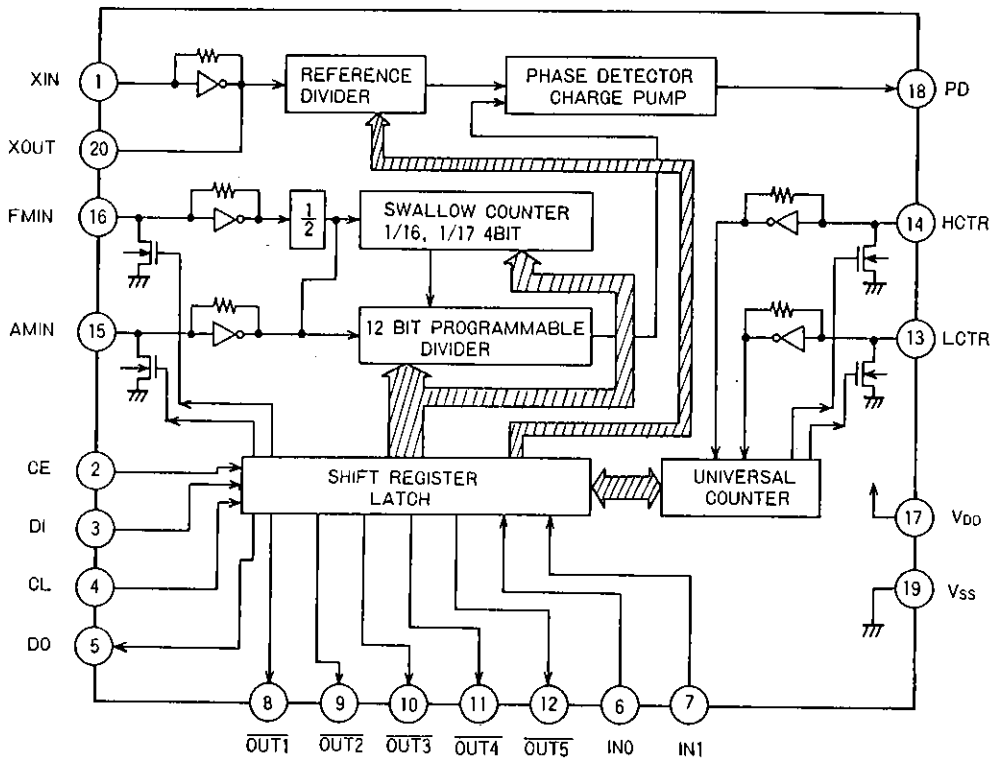
Package Dimensions 3036B

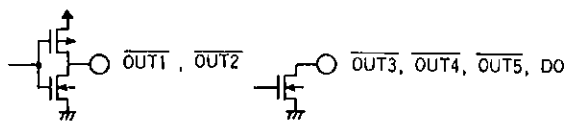
(unit: mm)



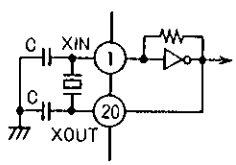
SANYO: MFP20

Block Diagram





※Sample Crystal Resonator:
7.200MHz CL16pF (C=27pF)
- LN-X-0702 (NR-18 type)
- LN-P-0001 (AT-51 type)



Nihon Dempa Kogyo Co., Ltd.

Pin Description

XIN, XOUT	:Crystal OSC (7.2MHz)
FMIN, AMIN	:Local oscillating signal input
CE, CL, DI, DO	:Serial data input/output
$\overline{OUT1}$ to $\overline{OUT5}$	:Output ports
IN0, IN1	:Input ports
HCTR, LCTR	:Universal counter signal input
PD	:Charge pump output

Maximum Ratings at Ta=25℃, Vss=0V

				unit
Maximum Supply Voltage	V_{DD}max	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_{IN}(1)	CE,CL,DI,IN0,IN1	−0.3 to +7.0	V
	V_{IN}(2)	Input ports other than V_{IN}(1)	−0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}(1)	DO	−0.3 to +7.0	V
	V_{OUT}(2)	OUT1,OUT2	−0.3 to V_{DD}+0.3	V
	V_{OUT}(3)	OUT3,OUT4,OUT5	−0.3 to +15	V
	V_{OUT}(4)	Output ports other than V_{OUT}(1),(2),(3)	−0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta≦85℃	200	mW
Operating Temperature	**Topr**		−40 to +85	℃
Storage Temperature	Tstg		−55 to +125	℃

Allowable Operating Conditions at Ta=−40 to +85°C, V_{SS}=0V

					min	typ	max	unit
Supply Voltage	$V_{DD}(1)$	V_{DD}			4.5		6.5	V
	$V_{DD}(2)$	V_{DD}	Crystal OSC		3.5		6.5	V
High Level Input Voltage	$V_{IH}(1)$	CE,CL,DI IN0,IN1			2.2		6.5	V
	$V_{IH}(2)$	LCTR	Pulse wave, DC coupling	Note 4)	$0.7V_{DD}(1)$		$V_{DD}(1)$	V
Low Level Input Voltage	$V_{IL}(1)$	CE,CL,DI IN0,IN1			0		0.7	V
	$V_{IL}(2)$	LCTR		Note 4)	0		$0.3V_{DD}(1)$	V
Output Voltage	$V_{OUT}(1)$	DO					6.5	V
	$V_{OUT}(2)$	$\overline{OUT3}$ to $\overline{OUT5}$					13	V
Input Frequency	$f_{IN}(1)$	XIN	Sine wave, capacitive coupling, $V_{DD}(2)$		1.0	7.2	8.0	MHz
	$f_{IN}(2)$	FMIN	Sine wave,capacitive coupling, $V_{DD}(1)$	Note 1)	10		130	MHz
				Note 5)			(160)	MHz
	$f_{IN}(3)$	AMIN	Sine wave, capacitive coupling, $V_{DD}(1)$	Note 1)	0.5		40	MHz
	$f_{IN}(4)$	HCTR	Sine wave, capacitive coupling, $V_{DD}(1)$	Note 2)	10		60	MHz
				Note 6)			(70)	MHz
	$f_{IN}(5)$	LCTR	Sine wave, capacitive coupling,$V_{DD}(1)$	Note 3)	15		500	kHz
	$f_{IN}(6)$	LCTR	Pulse wave, DC coupling	Note 4)	1.0		20×10^3	Hz
Crystal Oscillator Frequency	X'tal	$X_{IN}-X_{OUT}$	CI≦50Ω		3.0	7.2	8.0	MHz
Input Amplitude	$V_{IN}(1)$	X_{IN}	Sine wave, capacitive coupling, $V_{DD}(1)$		0.5		1.5	Vrms
	$V_{IN}(2)$	FMIN	Sine wave, capacitive coupling, $V_{DD}(1)$		0.07		0.5	Vrms
				Note 5)	(0.11)			Vrms
	$V_{IN}(3)$	AMIN	Sine wave, capacitive coupling, $V_{DD}(1)$		0.07		0.5	Vrms
	$V_{IN}(4)$	HCTR	Sine wave, capacitive coupling,$V_{DD}(1)$	Note 2)	0.07		0.5	Vrms
				Note 6)	(0.11)			Vrms
	$V_{IN}(5)$	LCTR	Sine wave, capacitive coupling, $V_{DD}(1)$	Note 3)	0.07		0.5	Vrms

Note 1) DV and SP represent 1 bit within serial data. ＊:Don't care

DV	SP	Input frequencyt	1/2 divider	1/16,17 swallow	12-bit main divider	Input pin
1	＊	10 to 130(160)MHz	○	○	○	(FMIN)
0	1	2 to 40 MHz	—	○	○	(AMIN)
0	0	0.5 to 10 MHz	—	—	○	(AMIN)

Note 2) Freqeuncy measurement
Note 3) Frequency measurement
Note 4) Period measurement
Note 5) $f_{IN}(2)$ 10 to 160MHz/$V_{IN}(2)$ 0.11Vrms (min)
Note 6) $f_{IN}(4)$ 10 to 70MHz/$V_{IN}(4)$ 0.11Vrms (min)

Electrical Characteristics under allowable operating conditions

				min	typ	max	unit
Built-in Feedback Resistance	$R_f(1)$	XIN			1.0		MΩ
	$R_f(2)$	FMIN			500		kΩ
	$R_f(3)$	AMIN			500		kΩ
	$R_f(4)$	HCTR			500		kΩ
	$R_f(5)$	LCTR			500		kΩ
Hysteresis Width	V_H	LCTR		$0.1V_{DD}$		$0.6V_{DD}$	V
High Level Input Current	$I_{IH}(1)$	CE,CL,DI	$V_I=6.5$			5.0	μA
	$I_{IH}(2)$	IN0,IN1	$V_I=V_{DD}$			5.0	μA
	$I_{IH}(3)$	XIN	$V_I=V_{DD}$			20	μA
	$I_{IH}(4)$	FMIN,AMIN	$V_I=V_{DD}$			40	μA
	$I_{IH}(5)$	HCTR,LCTR	$V_I=V_{DD}$			40	μA
Low Level Input Current	$I_{IL}(1)$	CE,CL,DI	$V_I=V_{SS}$			5.0	μA
	$I_{IL}(2)$	IN0,IN1	$V_I=V_{SS}$			5.0	μA
	$I_{IL}(3)$	XIN	$V_I=V_{SS}$			20	μA
	$I_{IL}(4)$	FMIN,AMIN	$V_I=V_{SS}$			40	μA
	$I_{IL}(5)$	HCTR,LCTR	$V_I=V_{SS}$			40	μA
High Level Output Voltage	$V_{OH}(1)$	$\overline{OUT1}$,$\overline{OUT2}$	$I_O=1mA$	$V_{DD}-1.0$			V
	$V_{OH}(2)$	PD	$I_O=0.5mA$	$V_{DD}-1.0$			V
Low Level Output Voltage	$V_{OL}(1)$	$\overline{OUT1}$,$\overline{OUT2}$	$I_O=1mA$			1.0	V
	$V_{OL}(2)$	PD	$I_O=0.5mA$			1.0	V
	$V_{OL}(3)$	$\overline{OUT3}$ to $\overline{OUT5}$	$I_O=5mA$			1.0	V
	$V_{OL}(4)$	DO	$I_O=5mA$			1.0	V
Output Off Leak Current	$I_{OFF}(1)$	$\overline{OUT3}$ to $\overline{OUT5}$	$V_O=13V$			5.0	μA
	$I_{OFF}(2)$	DO	$V_O=6.5V$			5.0	μA
High Level 3-State Off Leak Current	I_{OFFH}	PD	$V_O=V_{DD}$		0.01	10.0	nA
Low Level 3-Stage Off Leak Current	I_{OFFL}	PD	$V_O=V_{SS}$		0.01	10.0	nA
Input Capacitance	C_{IN}	FMIN, HCTR		1	2	3	pF
Supply Current	$I_{DD}(1)$	V_{DD}	$f_{IN}(2)=130MHz$ $V_{IN}(2)=70mVrms$ Crystal 7.2MHz OSC is connected. Other input pins=V_{SS} Output pins=Open		20	30	mA
	$I_{DD}(2)$	V_{DD}	PLL partially stops (PLL inhibit). Crystal OSC operates. Crystal 7.2MHz OSC is connected. Other input pins=V_{SS} Output pins=Open		1.0		mA

Note) Use a capacitor of 2000pF or more between power supplies V_{DD} and V_{SS}.

Pin Description

Symbol	Pin No.	Description	Function	Input/output
XIN XOUT	1 20	X'tal OSC	• Crystal oscillator (7.2MHz) is connected.	Input Output
FMIN	16	Local oscillation signal input	• FMIN is selected by sepcifying serial data input: DV=1 • Frequency between 10 and 130MHz is input (70mVrms min). • Signals are set to the swallow counter via built-in prescaler (1/2). • From 256 to 65536 frequency divisions are selected but this value can be doubled with built-in prescaler (1/2).	Input
AMIN	15	Local oscillation signal input	• AMIN is selected by specifying serial data input: DV=0. • When serial data input: SP=1 is specified. – Input frequency is between 2 and 40 MHz (70mVrms min). – Signals are not sent to built-in prescaler (1/2), but are directly transferred to swallow counter. – From 256 to 65536 frequency divisions are selected and used as is. • When serial data input: SP=0 is specified, – Input frequency is between 0.5 and 10MHz (70mVrms min). – Signals are directly transferred to a 12-bit programmable divider. – From 4 to 4095 frequency divisions are selected and used as is.	Input
PD	18	Charge pump output	• This is an output terminal for PLL charge pump signals. If the local oscillation signal frequency divided by N is higher than the reference frequency, high level signals are output from PD; if it is lower than the reference frequency, low level signals are output. If it is the same as the reference frequency, the signals are floated.	3 state
V_{DD}	17	Power supply	• Power is supplied to LC7216M via this pin. During PLL operation, 4.5 to 6.5V is applied. If only a crystal oscillation circuit is used for the controller clock and time base for the clock, the power supply can be reduced to a minimum of 3.5V.	—

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Symbol	Pin No.	Description	Function	Input/output
V_{SS}	19	Ground	• This pin is tied to the ground of LC7216M.	—
CE	2	Chip enable	• High level signals are input during serial data input (DI) or output (DO).	Input *
CL	4	Clock	• Data is synchronized by this clock signal during serial data input (DI) or output (DO).	Input *
DI	3	Input data	• Serial data transferred from controller to LC7216M is input to this pin. • A total of 36 bits of data should be input for initialization.	Input *
DO	5	Output data	• Serial data transferred from the controller to LC7216M output from this pin. • By synchronizing it with CL, 28 bits of the contents of the internal shift register can be output.	Output (N-channel open drain)
$\overline{OUT1}$ $\overline{OUT2}$ $\overline{OUT3}$ $\overline{OUT4}$ $\overline{OUT5}$	8 9 10 11 12	Output port	• Bits O_1 to O_5 of serial data, transferred from the controller, are latched, and the data is inverted and output in parallel. • $\overline{OUT1}$ and $\overline{OUT2}$ are complementary outputs. • $\overline{OUT3}$, $\overline{OUT4}$, and $\overline{OUT5}$ are N-ch open drain outputs (voltage durability: 13V).	Output
IN0 IN1	6 7	Input port	• Contents of input ports IN0 and IN1 are converted from parallel to serial form and are output from output pin DO.	Input *
HCTR	14	Universal counter frequency measuring signal input pin	• HCTR is selected by specifying spiral data input: SC=1. • Input frequency is between 10 and 60 MHz (70mVrms min). • Since signals are sent to a universal counter (20-bit binary counter) via a 1/8 of the actual frequency input to HCTR. • When HCTR is selected, either 120msec or 60msec can be specified as the measuring time in the frequency measurement mode. (GT=1/0; 120/60msec) • Result can be output from MSB of the universal counter via output pin DO.	Input

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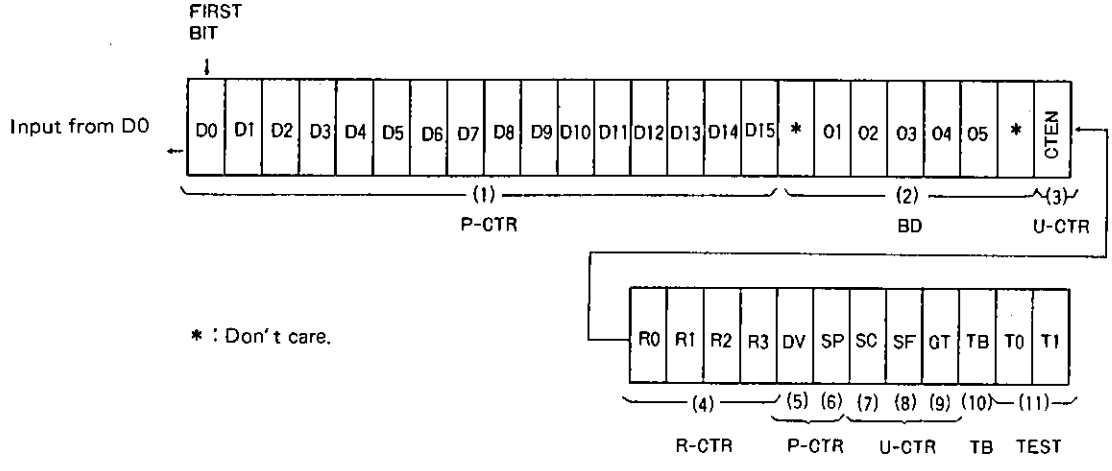
Symbol	Pin No.	Description	Function	Input/output
LCTR	13	Universal counter frequency/period measuring signal input pin	• LCTR is selected by specifying serial data input: SC=0. • If serial data input : SF=1 is set, – Frequency measurement mode is selected. – Input frequency range is between 15 and 500kHz 870mVrms min). – Signals are not sent to the internal 1/8 divider, but are directly transmitted to the universal counter. – Same measuring time options as for HCTR are provided. • If serial data input: SF=0 is set, – Period measurement mode is selected. – Input frequency range is between 1Hz and 20kHz. ($V_{IH}=0.7V_{DD}$ min, $V_{IL}=0.3V_{DD}$ max) – Either a 1- or 2-cycle measuring period can be selected. When a 2-cycle period is selected, the input frequency rang is between 2 Hz and 20kHz. (GT=1/0; 2/1 cycle) • Result is output as in HCTR.	Input

* High and low level input voltage to CE, CL, DI, IN0 and IN1 are held to the following range, respectively, regardless of the supply voltage (V_{DD}):
V_{IH}=2.2 to 6.5V, V_{IL}=0 to 0.7V

Structure of Control Data (Serial Data Input)



The control serial data of LC7216M consists of 36 bits. When power is turned on, data should be entered on every one of these bits for initialization. However, the last two bits are not related to the user, because data on these bits is used for switching the test mode.
After initialization, only the contents of DO through CTEN (the first 24 bits) can be changed without affecting the rest of the bits (the last 12 bits) using the serial data input mode. Data is input at the DI pin.

<table>
<tr><th>Symbol</th><th>Control section/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

D0 to D15</td><td>• Used to determine number of frequency divisions of the programmable divider.
Data is in binary notation and D15 is the MSB. The LSB depends on the DV and SP settings (see table below)

<table>
<tr><th>DV</th><th>SP</th><th>LSB</th><th>No. of divisions</th><th>Actual No. of divisions</th></tr>
<tr><td>1</td><td>*</td><td>D0</td><td>256 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>D0</td><td>256 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>D4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
*: Don't care.
If the LSB is D4, the data in D0 to D3 is of no value.</td><td>DV

SP</td></tr>
<tr><td>(2)</td><td>Output port data

O1 to O5</td><td>• Used to determine output from output ports $\overline{OUT1}$ to $\overline{OUT5}$.
O1 determines output from $\overline{OUT1}$. When O1=1, $\overline{OUT1}$ is set low; and when O1=0, $\overline{OUT1}$ is set high. the same applies to O2 to O5.
• Can be used to switch bands and for various other operations.</td><td></td></tr>
<tr><td>(3)</td><td>Universal counter starting data

CTEN</td><td>• Used to operate the universal counter. When CTEN=0, the universal counter, or 20-bit binary counter is reset, and both HCTR and LCTR are put into the pull-down (GND) state.
When CTEN=1, the universal counter is released from reset, and counts signals input to HCTR or LCTR (which one is specified by the universal counter select data SC setting.).
• Universal counter is reset when CTEN=0, note that count data should be transferred to the controller while CTEN=1.</td><td>SC

SF

GT</td></tr>
</table>

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<table>
<tr><th>Symbol</th><th>Control section/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(4)</td><td>Reference frequency data
R0 to R3</td><td>
• Used to select a reference frequency from among 10 options, and inhibit PLL operation of LC7216M, i.e., put it into backup mode.

(unit: kHz)
<table>
<tr><th>R0</th><th>R1</th><th>R2</th><th>R3</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1
1
1
1</td><td>1
1
1
1</td><td>0
0
1
1</td><td>0
1
0
1</td><td>*PLL INHIBIT</td></tr>
</table>
*PLL INHIBIT (Backup mode)
Programmable divider stops, and both FMIN and AMIN are set to pull-down state (GND), charge pump output is floated.
</td><td></td></tr>
<tr><td>(5)

(6)</td><td>Divider select data
DV

Sensitivity select data
SP</td><td>
• DV is used to select the input pin (either FMIN or AMIN) of local oscillation signal.
• SP is used to switch the input frequency range for AMIN selection.
<table>
<tr><th>DV</th><th>SP</th><th>Input pin</th><th>Input frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 130MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
*Don't care.
</td><td></td></tr>
</table>

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<table>
<tr><th>Symbol</th><th>Control section/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(7)

(8)</td><td>Universal counter input pin select data

SC

Universal counter frequency/period switch data

SF</td><td>• SC is used to select the input pin (either HCTR or LCTR) of the universal counter.
• SF is used to switch frequency/period measurement for LCTR selection. SF is invalid when HCTR is selected, in which case frequency measurement is automatically selected.

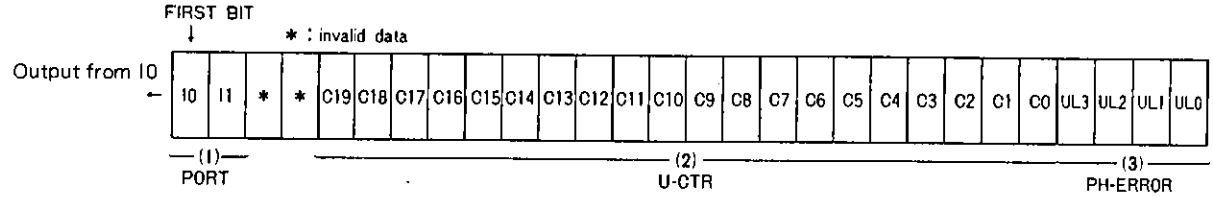
<table>
<tr><th>DV</th><th>SP</th><th>Input pin</th><th>Input frequency range</th></tr>
<tr><td>1</td><td>*</td><td>HCTR</td><td>Frequency (sine wave)</td></tr>
<tr><td>0</td><td>1</td><td>LCTR</td><td>Frequency (sine wave)</td></tr>
<tr><td>0</td><td>0</td><td>LCTR</td><td>Period (pulse)</td></tr>
</table>
* Don't care.</td><td>CTEN
GT</td></tr>
<tr><td>(9)</td><td>Universal counter count time select data

GT</td><td>• GT is used to select the measuring time for frequency measurement, or the number of cycles for period measurement.

GT = 1; 120 ms/2 cycles
GT = 0; 60 ms/1 cycle
(Frequency measurement/period measurement)</td><td>CTEN
SC
SF</td></tr>
<tr><td>(10)</td><td>Time base output data
TB</td><td>TB=0</td><td></td></tr>
<tr><td>(11)</td><td>LSI test data

T0, T1</td><td>• T0 and T1 are used to switch LSI test modes, not user-related data.
Set T0 and T1 to 0 normally.
Do not forget to enter 0 for T0 and T1 at power-on.</td><td></td></tr>
</table>

Structure of DO Output (Serial Data Output)



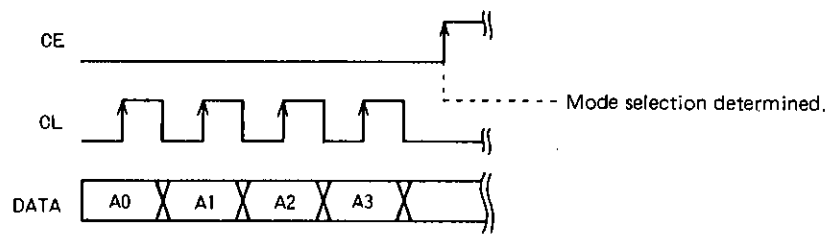
LC7216M has 28-bit shift registers which can output to the DO pin the contents of input ports IN0 and IN1, and a universal counter (20-bit binary counter).
The contents of each shift register are determined (latched) when the serial data output mode is selected.

No.	Data	Description
(1)	Input port data I_0, I_1	• Latched contents of input ports IN0 and IN1 are placed in I_0 and I_1, respectively.
(2)	Universal counter binary data C_{19} to C_0	• Latched contents of universal counter (20-bit binary counter) are placed in C_{19} to C_0. C_{19} ←MSB or 20-bit binary counter. C_0 ←LSB of 20-bit binary counter.
(3)	PLL unlock data UL3 to UL0	• Latched contents of unlocked detector are placed in UL3 to UL0. When phase difference more than shown below occurs, each of UL3 to UL0 is set to "1". UL0 : 1.11μsec. UL1 : 2.22μsec. UL2 : 3.33μsec. UL3 : 0.55μsec. (Crystal : 7.2MHz)

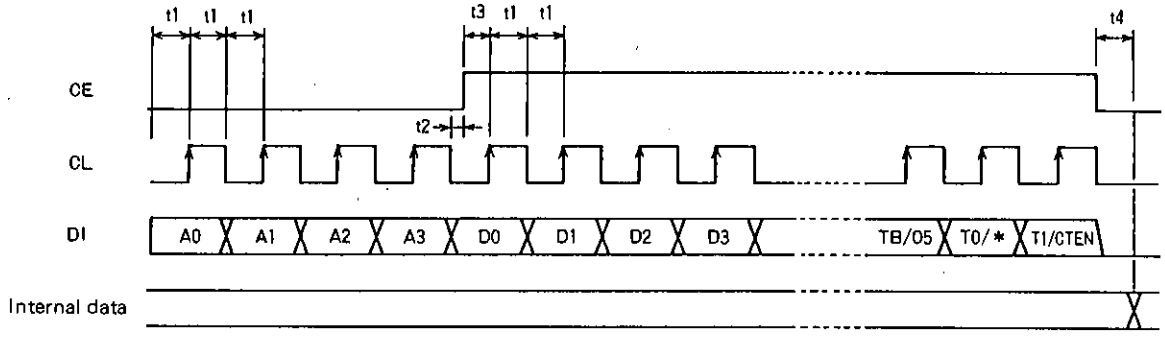
Input/Output of Serial Data

The LC7216M provides two input modes for control data (serial data input) and one output mode for DO output (serial data output). Data is input or output when one of these modes is selected.
The mode is set by the four bits A_0 to A_3 (from the DI pin) sent immediately before the CE pin is set high, then synchronized with the clock (CL), and selected when CE is set high.

Mode	A_3	A_2	A_1	A_0	Input/output	Description
1	0	0	0	1	Serial data (all bits) input	• All bits (36 bits) of control data (serial data) are input in this mode. It is used during initialization following power ON sequence, or when data that cannot be changed in mode 2 is to be changed. All 36 bits are input from the DI pin of LC7216M.
2	0	0	1	0	Serial data (part of bits) input	• A part (24 bits) of control data (serial data) is input in this mode. It is used to change the 24 bits comprising (1) the programmable divider data (D_0 to D_{15}), (2) the output port data (O_1 to O_5), and (3) the universal counter starting data (CTEN). Data in the other 12 bits does not change at this time. (If this part of data is to be changed, select mode 1.)
3	0	0	1	1	Serial data output	• This mode is used to output (1) input port data, and (2) universal counter binary data from DO.
	0 to 0	1 to 0	0 to 0	0 to 0	Invalid setting	Serial data is neither input nor output.

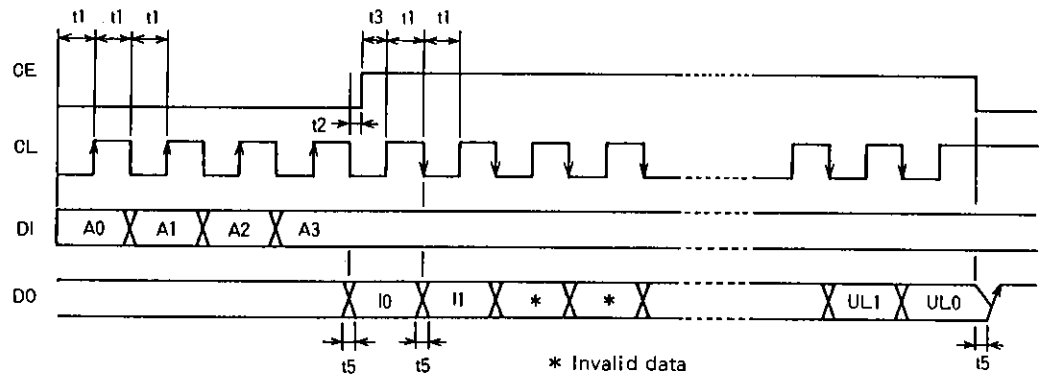


i) Input of serial data (mode 1, mode 2) $t1 \geqq 1.5\mu s$. $t2 \geqq 0\mu s$. $t3 \geqq 1.5\mu s$. $t4 < 1.5\mu s$.



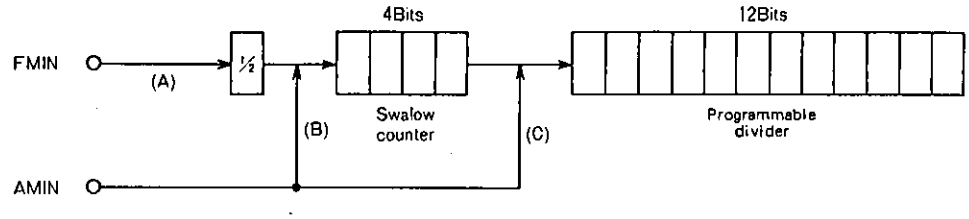
1) In mode 1: A total of 40 bits consisting of mode select data (4 bits) and control data (36 bits) are synchronized with the clock (CL) and input from the DI pin (data from D_0 to T_1).
2) In mode 2: A total of 28 bits consisting of mode select data (4 bits) and control data (24 bits) are synchronized with the clock and input from the DI pin (data from D_0 to CTEN).

ii) Output of serial data (mode 3) $t1 \geqq 1.5\mu s$. $t2 \geqq 0\mu s$. $t3 \geqq 1.5\mu s$. $t5 < 1.5\mu s$.
(DO is the N-ch open drain terminal and the change time depends on the pull-up resistance value.)



3) In mode 3: The serial data output mode (mode 3) is selected by specifying the mode select data (4 bits). Setting CE high allows I_0 to be output to DO.
Once CE is put high data is output to the DO pin when the internal shift register contents shift as CL falls. (To output data up to UL_0, 27 clocks are required after CE is set high.) When this mode is selected, DO is forcibly set high as CE goes low, and set low when the IN0 pin changes, or after the measurement using the universal counter is finished (the completion of measurement has priority over the change of IN0 level).

Structure of Programmable Divider



	DV	SP	Input pin	No. of divisions	Actual No. of divisions	Input frequency range
(A)	1	*	FMIN	256 to 65535	Twice the set value	10 to 130MHz
(B)	0	1	AMIN	256 to 65535	Set value	2 to 40MHz
(C)	0	0	AMIN	4 to 4095	Set value	0.5 to 10MHz

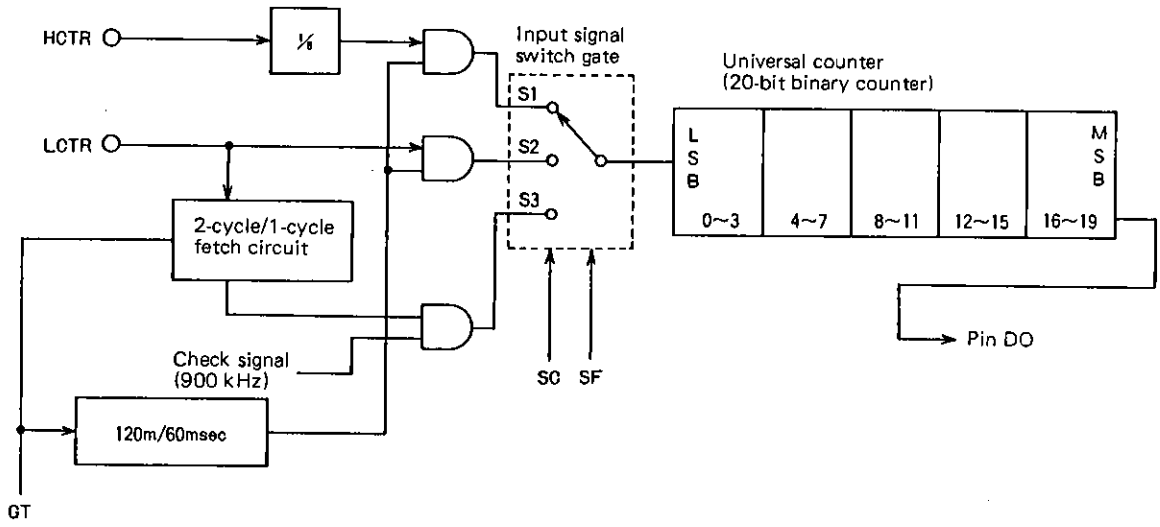
Notes:

1) When FMIN (A) is selected, the actual number of frequency divisions is twice the set number of divisions. For example, if the set number of divisions=1000, the actual number of divisions=2000. If set number of divisions=1001, the actual number of divisions=2002. In other words, the reference frequency multiplied by 2 is used for the channel step.

2) To set the channel step to 9, 5, or 1kHz during FMIN (A), the crystal OSC should be changed to 3.6MHz. Remember that the times listed in the following table also refer to the crystal OSC, and therefore, change as the crystal OSC changes.
When 3.6MHz is used for the crystal OSC, care should be taken for overtone oscillation.

Parameter	X'tal	
	7.2MHz	3.6MHz
Frequency measuring time	120/60ms	240/120ms
Frequency measuring check signal	900kHz	450kHz
Reference frequency	100, 50, 25,... 10, 9, 5, 1kHz	50, 25, 12.5,... 5, 4.5, 2.5, 0.5kHz
Serial data input/output (CL)	t1≧1.5μs t3≧1.5μs	t1≧3.0μs t3≧3.0μs

Structure of Universal Counter



	SC	SF	Input pin	Measurement	Frequency range	GT (1/0)
S1	1	*	HCTR	Frequency	10 to 60MHz (sine wave)	120ms /60ms
S2	0	1	LCTR	Frequency	15 to 500kHz (sine wave)	120ms /60ms
S3	0	0	LCTR	Period	1Hz to 20kHz (pulse)	2-cycle/1-cycle

The universal counter of LC7216M consists of a 20-bit binary counter. The count value can be read from the MSB via pin DO.

When the universal counter is used to measure the frequency, the measuring time can be selected from between 120ms and 60ms by setting the GT value. The frequency of the signals input to the HCTR or LCTR pin is determined by the pulse count on the universal counter within the selected measuring time.

When the universal counter is used to measure the period, the period of signals input to the LCTR pin is determined by the check signal (900kHz) count on the universal counter within the selected cycle (2- or 1-cycle) of signals input to LCTR.

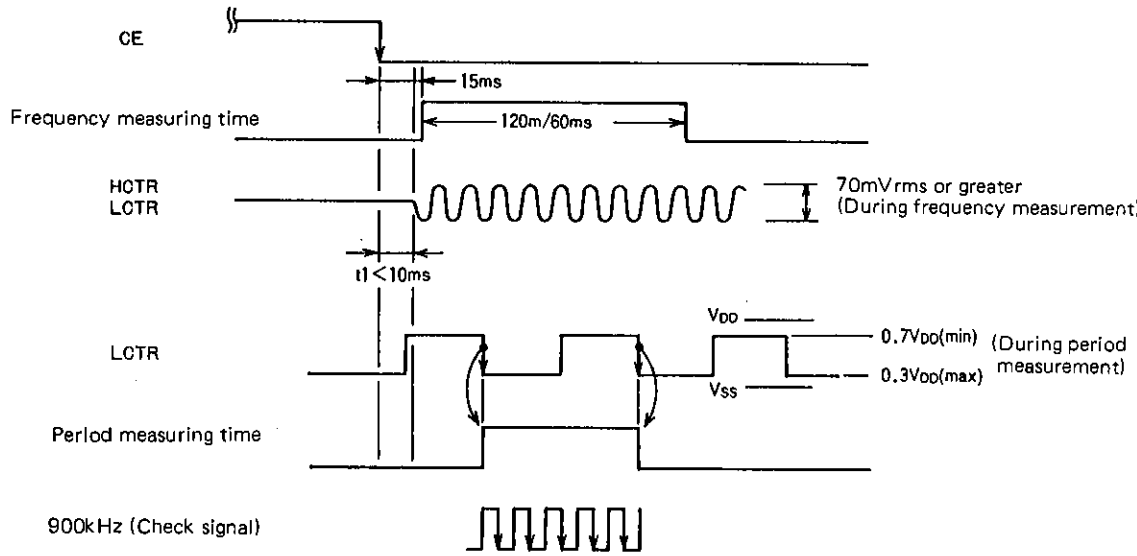
The universal counter starts counting when serial data CTEN is set to 1. Serial data is determined inside the LC7216M by dropping CE from high to low. However, signal must be input to the HCTR or LCTR pin within 10ms after CE goes low.

Upon completion of measurement, the result on the universal counter must be read out while CTEN=1 (when CTEN=0, the universal counter is reset).

It should be noted that the universal counter should be reset by setting CTEN to 0 before counting is started.

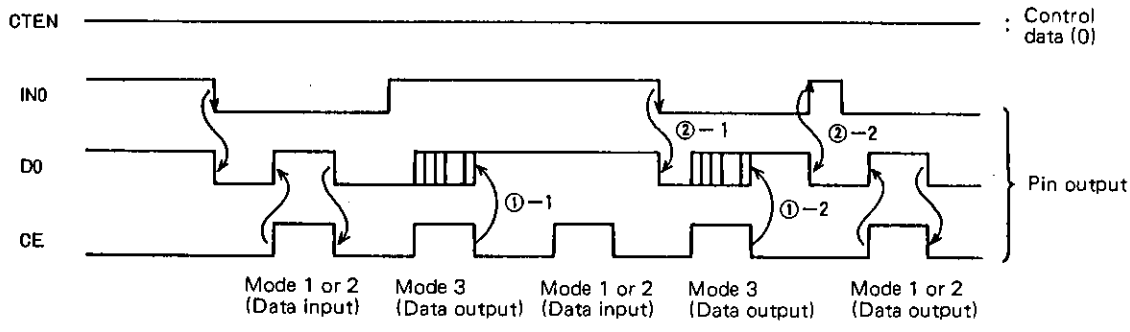
The signal input to the LCTR pin are sent directly to the universal counter while those input to the HCTR pin are 1/8 divided before being sent to the universal counter. The result on the universal counter is, therefore, 1/8 value of the actual frequency input to HCTR.

When the universal counter is used as the IF counter, the state of the IF-IC SD (station detect) signal must be checked by the microcontroller and the IF counter buffer output turned on only after the SD signals are activated. Auto-search techniques using only the IF counter are not advisable since it is possible that the search can stop incorrectly at a location that does not have a station due to IF counter buffer leakage output.



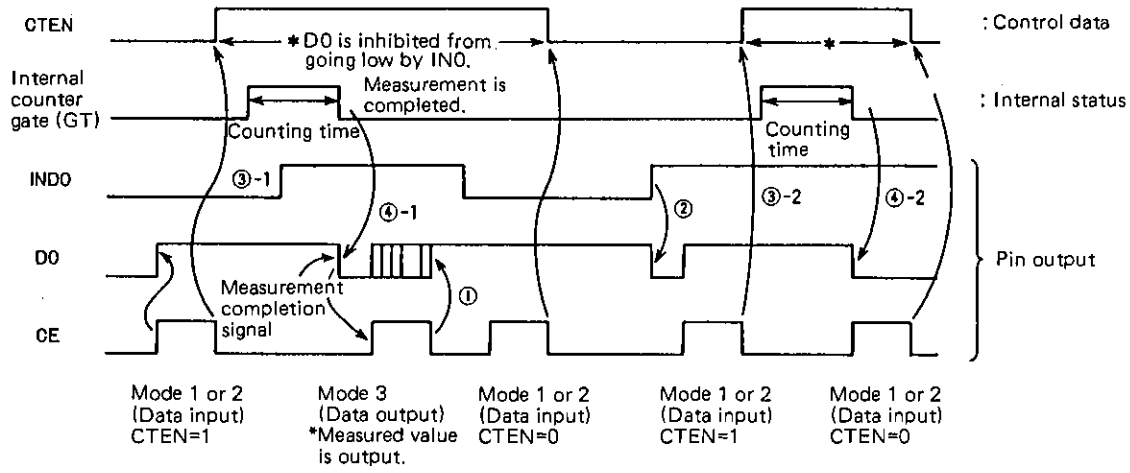
The DO pin is forcibly set high when the universal counter starts counting (CTEN=1), and automatically goes low after the measurement is finished (i.e., after 120 or 60msec, or a signal input in 1- or 2-cycle). DO can, therefore, be used to check the measured value.

i) Universal counter is not used (CTEN=0) DO: Changes in external signals can be checked.



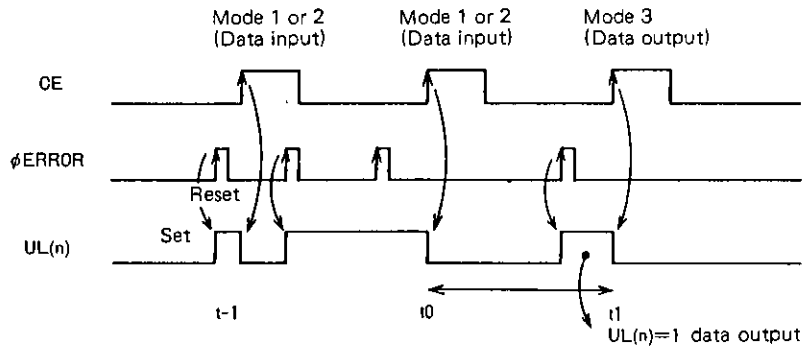
1) Select mode 3 to output data from DO. DO automatically goes high after outputting data (CE Low).
2) When IN0 changes, DO automatically goes low.
(i.e., changes in external signals input to IN0 can be checked).

ii) Universal counter is used DO: Completion of counting by universal counter can be checked.



3) While CTEN=1, DO is inhibited from going low by IN0, and is automatically set high.
4) When the measurement with the universal counter is finished, DO automatically goes low (i.e., the completion of measurement can be checked).

PLL Unclock Detector



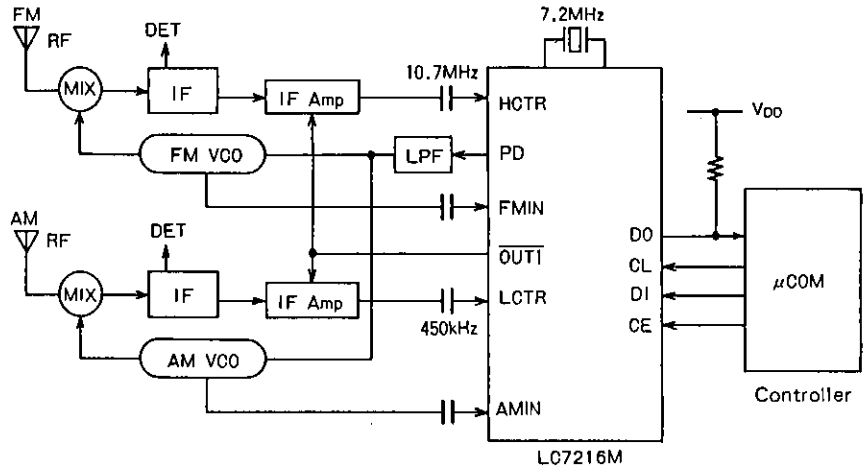
Internal data UL(n) is set/reset on the positive transition of φERROR signal/CE signal, respectively. In mode 3 (data output), φERROR data UL(n) after the previous positive transition of CE signal is read.
In the example shown above, data for the period of t_0 to t_1 is read.

		UL(n) 3210
φERROR<0.55μs	⟶	0000
0.55μs≦φERROR<1.11μs	⟶	1000
1.11μs≦φERROR<2.22μs	⟶	1001
2.22μs≦φERROR<3.33μs	⟶	1011
3.33μs≦φERROR	⟶	1111

When φERROR mode than shown below occurs, each of UL3 to UL0 is set to "1".
UL0:1.11μs .
UL1:2.22μs .
UL2:3.33μs .
UL3:0.55μs .
φERROR:Phase difference (Crystal 7.2MHz)

Sample Application System

• FM/AM (IF counting is carried out.)



Note 1) The capacitance of the coupling capacitors for the FMIN, AMIN, HCTR and LCTR pins should be set between 50 and 100pF (it may be 1000 pF if LCTR is selected at 100kHz or less).

Note 2) Place the coupling capacitor near the pin.

Note 3) The IF signals measurement should be done after the IF-IC SD (station detect) signals are activated.

1) FM: For 100kHz step
When FM RF = 90MHz (IF=+10.7MHz),
FM VCO=100.7MHz
Select PLL fref=50kHz
DV=1, SP=* (FMIN)
Set N=1007
When N is the number of frequency divisions on the programmable divider (decimal).

2) AM: For 10kHz step
When AM RF=1000kHz (IF=+450kHz),
AM VCO=1450kHz
Select PLL fref=10kHz
DV=0, SP=0 (AMIN: Low speed)
Set N=145
Where N is the number of frequency divisions on the programmable divider (decimal).

*: Don't care