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Ordering number: EN ※3941B

CMOS LSI

No. ※3941B

LC7441N, 7441NE

Picture-in-picture Controller for TVs and VCRs

Preliminary

Overview

The LC7441N, 7441NE are picture-in-picture (PIP) system controller ICs for use in NTSC, PAL or multi-system (both NTSC and PAL) TVs and VCRs. The LC7441 PIP system configuration requires discrete LC7480 A/D converter and memory ICs.

The LC7441 system controller IC provides nested-picture main-screen/sub-screen video signal control. Single or multiple (2) sub-screens occupying 11.11% (one-third height, one-third width) of the main-screen can be constructed and controlled. Features include still/active display, white/color frame, fixed/variable (screen) positioning, and wipe function for gradual sub-screen display and erasure. Sub-screen horizontal resolution is achieved by 248 6-bit, 64-level samples.

The LC7441 construction includes A/D interface, vertical (VERT) filter, memory controller, odd-field decision circuits, read/write PLLs and D/A converters.

The LC7441 operates from a 5 V supply and is available in 64-pin DIPs and 64-pin QIPs.

Features

- NTSC, PAL and multi-system compatibility
- TV and VCR signals
- Forms component-based PIP controller system.
- One or two (nested) sub-screens occupying 11.11% of main-screen
- Still and active video display control
- White and colored screen frames
- Fixed and variable screen positioning
- Gradual sub-screen display and erasure (wipe) function
- A/D interface, vertical (VERT) filter, memory controller
- Three D/A converters
- 5 V supply
- 64-pin DIP and 64-pin QIP

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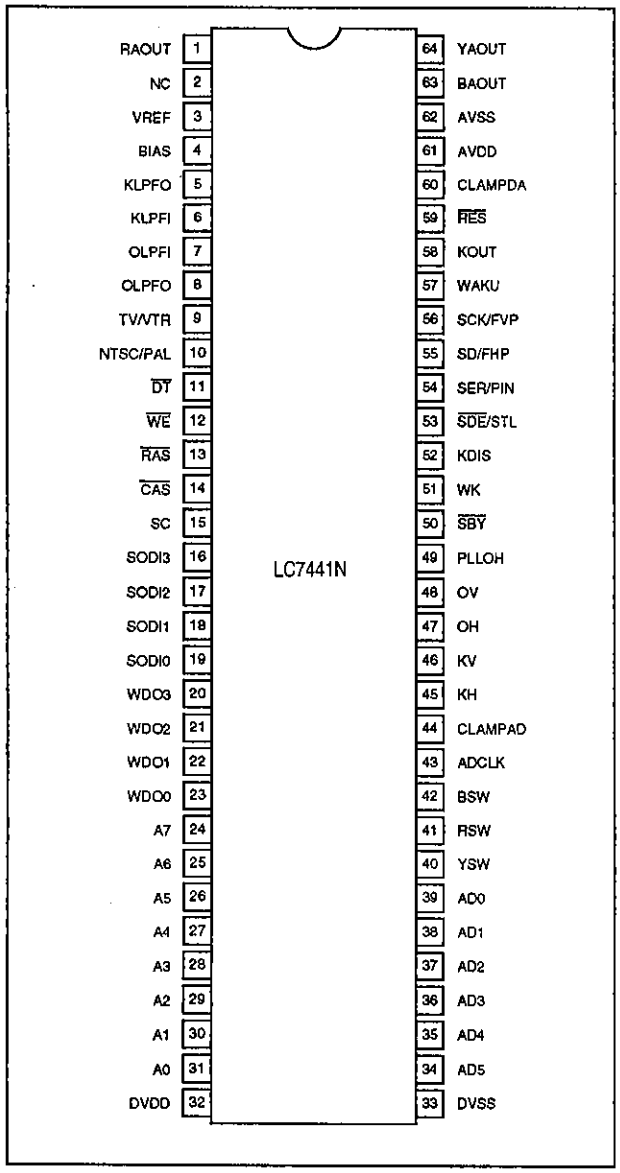
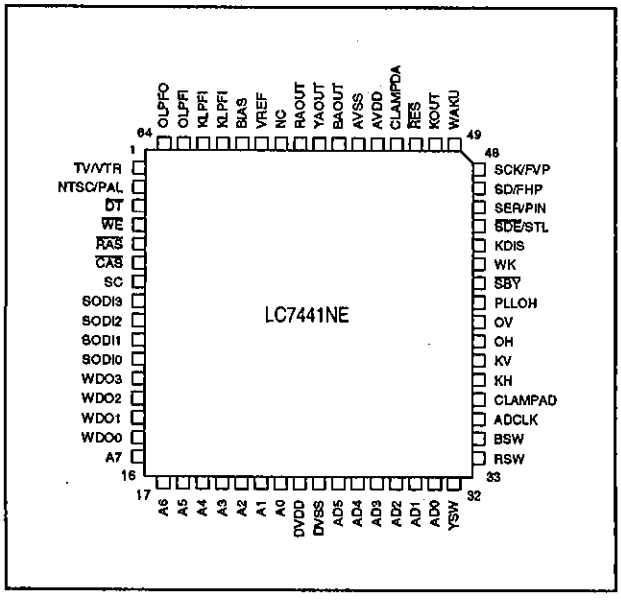
Pin Assignments

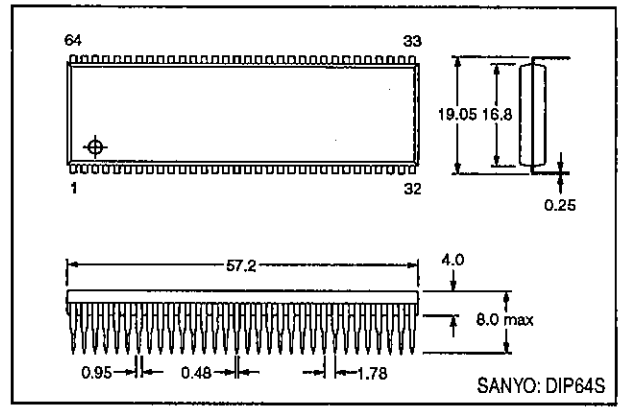




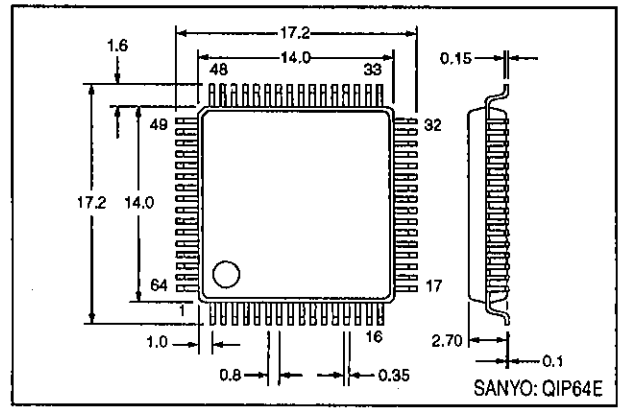
Package Dimensions

Unit: mm

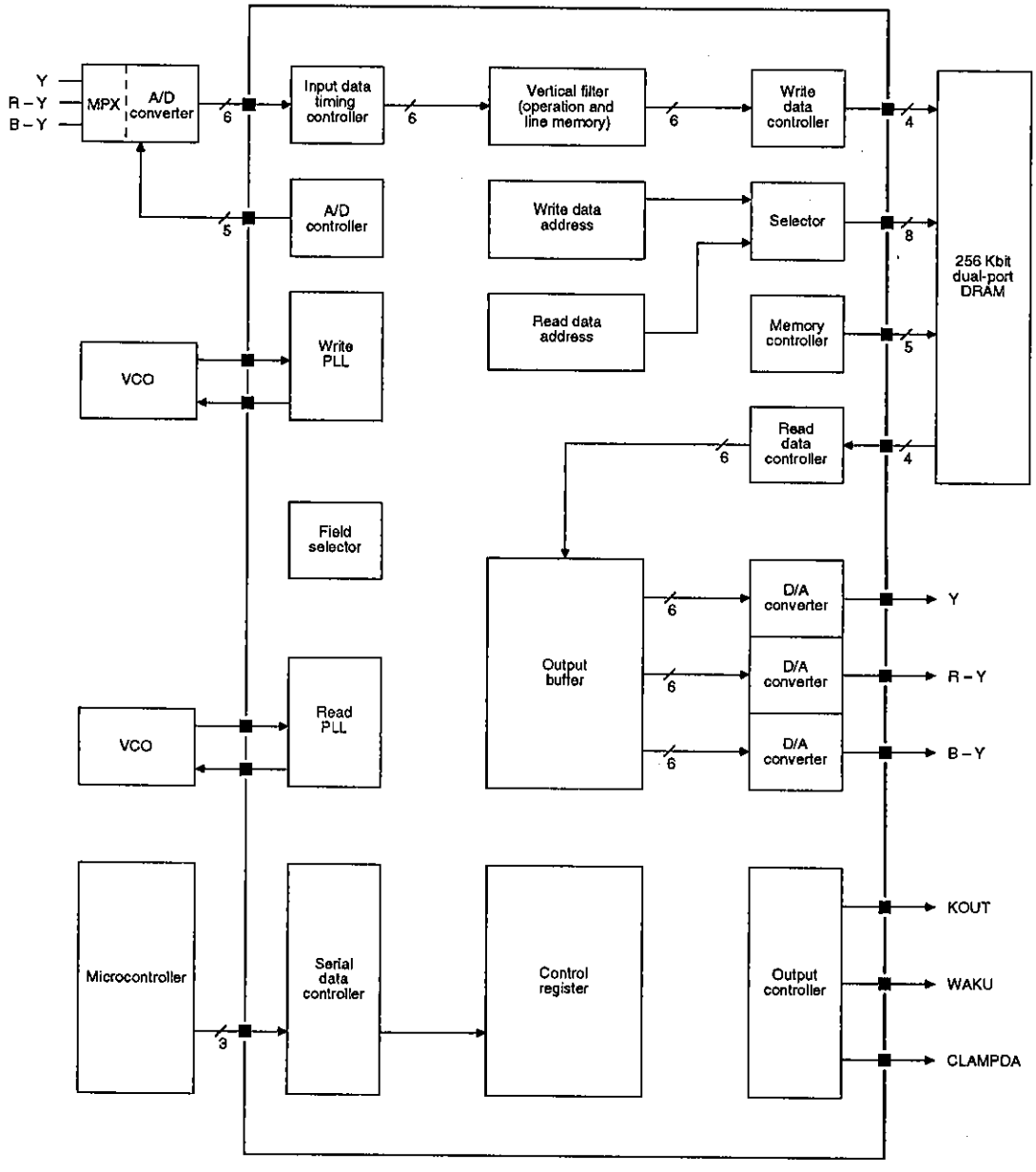
3071-DIP64S (LC7441N)



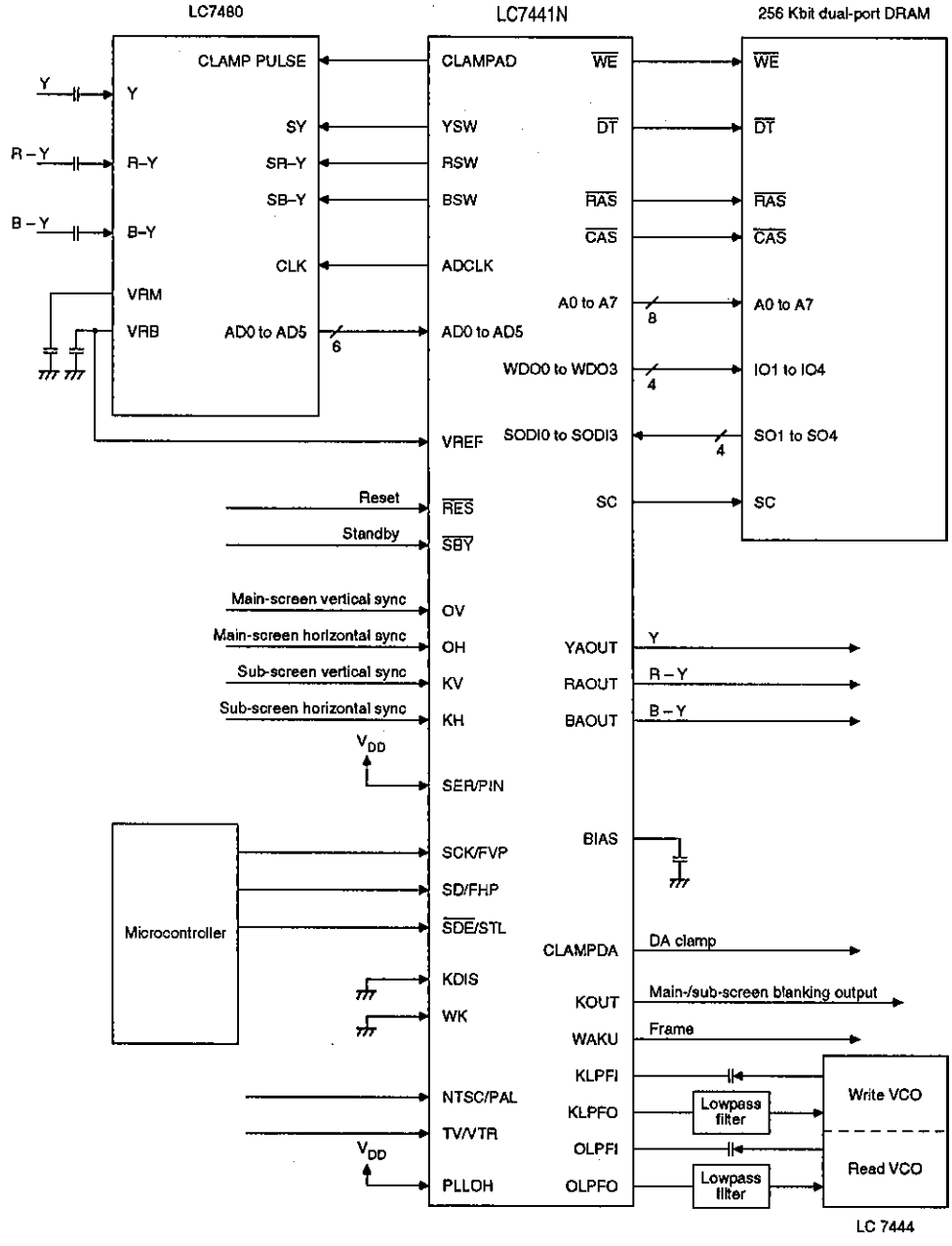
3159-QIP64E (LC7441NE)



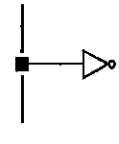
Block Diagram

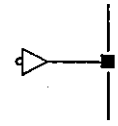
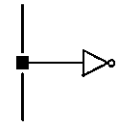
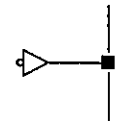
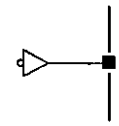
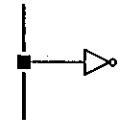
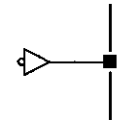


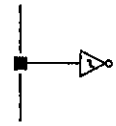
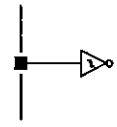
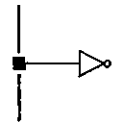
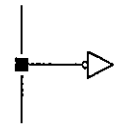
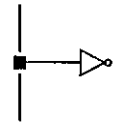
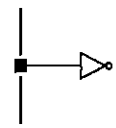
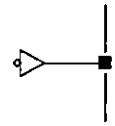
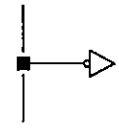
PIP System Diagram

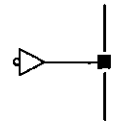
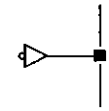
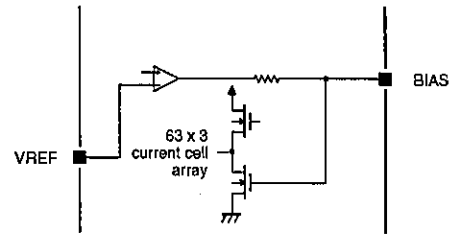
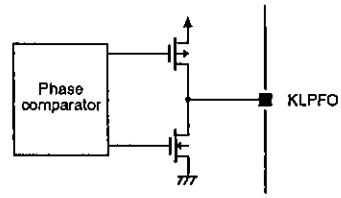
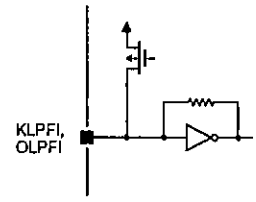
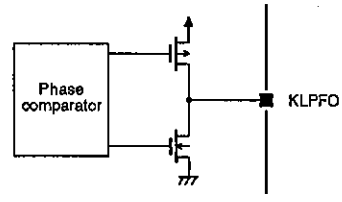


Pin Functions

Number		Name	Equivalent circuit	Function
QIP	DIP			
1	9	TV/VTR		TV/VCR select, CMOS input
2	10	NTSC/PAL		NTSC/PAL select, CMOS input

Number		Name	Equivalent circuit	Function
QIP	DIP			
3	11	$\overline{DT}$		Dual-port memory control outputs
4	12	$\overline{WE}$		
5	13	$\overline{RAS}$		
6	14	$\overline{CAS}$		
7	15	SC		
8	16	SODI3		4-bit, dual-port memory serial output data, TTL inputs
9	17	SODI2		
10	18	SODI1		
11	19	SODI0		
12	20	WDO3		4-bit, dual-port memory input data output lines
13	21	WDO2		
14	22	WDO1		
15	23	WDO0		
16	24	A7		8-bit, dual-port memory address output lines. The msb is A7, and the lsb, A0.
17	25	A6		
18	26	A5		
19	27	A4		
20	28	A3		
21	29	A2		
22	30	A1		
23	31	A0		
24	32	DVDD		5 V digital supply
25	33	DVSS		Digital ground
26	34	AD5		6-bit, sampled digital data TTL inputs. The msb is AD5, and the lsb, AD0.
27	35	AD4		
28	36	AD3		
29	37	AD2		
30	38	AD1		
31	39	AD0		
32	40	YSW		A/D interface Y-select output
33	41	RSW		A/D interface R – Y select output
34	42	BSW		A/D interface B – Y select output
35	43	ADCLK		Sampling-clock output
36	44	CLAMPAD		A/D conversion clamp pulse output
37	45	KH		Sub-screen horizontal sync input

Number		Name	Equivalent circuit	Function
QIP	DIP			
38	46	KV		Sub-screen vertical sync, Schmitt-trigger input
39	47	OH		Main-screen horizontal sync input
40	48	OV		Main-screen vertical sync, Schmitt-trigger input
41	49	PLLOH		Read-PLL horizontal sync signal select, CMOS input
42	50	$\overline{SBY}$		Active-LOW standby mode set, CMOS input
43	51	WK		Sub-screen frame ON/OFF select, CMOS input
44	52	KDIS		Sub-screen display ON/OFF select, CMOS input
45	53	$\overline{SDE}$/STL		Serial data enable and still picture select, CMOS input
46	54	SER/PIN		Serial data and pin data select, CMOS input
47	55	SD/FHP		Serial data and sub-screen horizontal position select, CMOS input
48	56	SCK/FVP		Serial data clock and sub-screen vertical position select, CMOS input
49	57	WAKU		Frame output
50	58	KOUT		Main-screen/sub-screen switch, blanking signal output
51	59	$\overline{RES}$		Active-LOW reset, CMOS input

Number		Name	Equivalent circuit	Function
QIP	DIP			
52	60	CLAMPDA		D/A converter clamp-pulse output
53	61	AVDD		5 V analog supply
54	62	AVSS		Analog ground
55	63	BAOUT		B – Y D/A converter output
56	64	YAOUT		Y D/A converter output
57	1	RAOUT		R – Y D/A converter output
58	2	NC		No connection
59	3	VREF		D/A converters reference voltage input
60	4	BIAS		D/A converters bias capacitor connection
61	5	KLPFO		Sub-screen horizontal sync PLL charge-pump, tristate output
62	6	KLPFI		Sub-screen horizontal sync PLL VCO clock input
63	7	OLPFI		Sub-screen horizontal sync PLL VCO clock input
64	8	OLPFO		Main-screen horizontal sync PLL charge-pump, tristate output

Specifications

Absolute Maximum Ratings

$V_{DD} = DV_{DD} = AV_{DD}$, $V_{SS} = DV_{SS} = AV_{SS} = 0$ V

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Input voltage range	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage range	V_O	−0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	500	mW
Operating temperature range	T_{opr}	−10 to 70	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Allowable Operating Ranges

$V_{DD} = DV_{DD} = AV_{DD}$, $T_a = 25$ °C

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

Electrical Characteristics

$V_{DD} = DV_{DD} = AV_{DD} = 5$ V ±10%, $V_{SS} = 0$ V, $T_a = 23$ to 27 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Digital supply current	I_{DDD}	$V_{\overline{RES}} = V_{\overline{SBY}} = V_{DD}$, $f_{OV} = f_{KV} = 60$ Hz, $f_{OH} = f_{KH} = 15$ kHz, $f_{KLPFI} = f_{OLPFI} = 20$ MHz	–	20	–	mA
Analog supply current	I_{DDA}	$V_{\overline{RES}} = V_{\overline{SBY}} = V_{DD}$, $f_{OV} = f_{KV} = 60$ Hz, $f_{OH} = f_{KH} = 15$ kHz, $f_{KLPFI} = f_{OLPFI} = 20$ MHz	–	20	–	mA
Standby supply current	I_{DDO}	$V_{\overline{RES}} = V_{\overline{SBY}} = V_{SS}$	–	–	10	µA
Input leakage current	I_{OFF}		−1	–	1	µA
TTL LOW-level input voltage	V_{IL1}		–	–	0.6	V
CMOS LOW-level input voltage	V_{IL2}		–	–	$0.3V_{DD}$	V
TTL HIGH-level input voltage	V_{IH1}		2.2	–	–	V
CMOS HIGH-level input voltage	V_{IH2}		$0.7V_{DD}$	–	–	V
Reference voltage	V_{REF}		–	$AV_{DD} - 1$	AV_{DD}	V
KLPFI and OLPFI input voltage	V_I	22 MHz sine wave, capacitive coupling	1	–	–	V_{p-p}
KLPFO and OLPFO output leakage current	I_{OZ}	$V_I = V_{DD}$ or V_{SS}	−0.1	0.01	0.1	µA
LOW-level output voltage for all outputs except KLPFO and OLPFO	V_{OL1}	$I_{OL} = 4$ mA	–	–	0.4	V
KLPFO and OLPFO LOW-level output voltage	V_{OL2}	$I_{OL} = 1$ mA	–	–	1	V

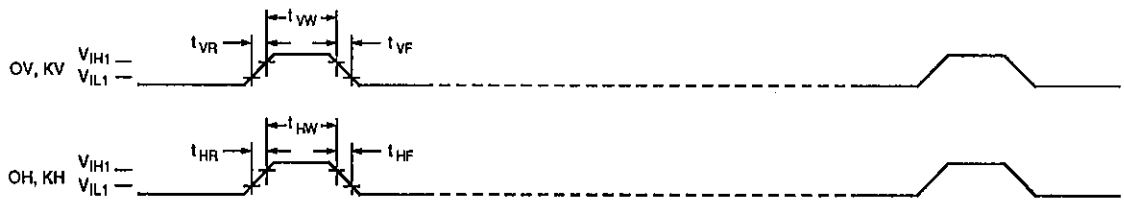
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
HIGH-level output voltage for all outputs except KLPFO and OLPFO	V_{OH1}	I_{OH} = –0.8 mA	2.4	–	–	V
KLPFO and OLPFO HIGH-level output voltage	V_{OH2}	I_{OH} = –1 mA	V_{DD} – 1	–	–	V
KLPFI and OLPFI pull-up current	I_{PV}	V_{RES} = V_{SBY} = V_{SS}	–	50	–	µA
YAOUT, RAOUT and BAOUT output impedance	R_{DA}		–	150	–	Ω
Phase compensating capacitance	C_{BS}		–	1	–	µF

Timing Characteristics

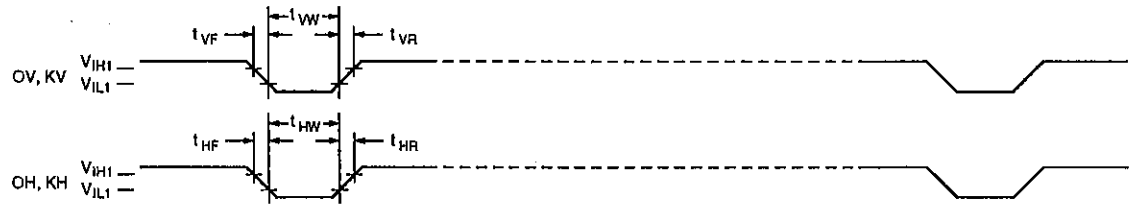
V_{DD} = DV_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = 0 V, T_a = 23 to 27 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
KV and OV pulsewidth	t_{VW}		1	–	–	µs
KV and OV rise time	t_{VR}		–	–	50	ns
KV and OV fall time	t_{VF}		–	–	50	ns
KH and OH pulsewidth	t_{HW}		1	–	–	µs
KH and OH rise time	t_{HR}		–	–	50	ns
KH and OH fall time	t_{HF}		–	–	50	ns
SCK pulsewidth	t_{SCW}		200	–	–	ns
SCK rise time	t_{SCR}		50	–	–	ns
SCK fall time	t_{SCF}		50	–	–	ns
SCK period	t_{SCI}		2	–	–	µs
SD to SCK setup time	t_{DSU}		100	–	–	ns
SCK to SD hold time	t_{DH}		30	–	–	ns
$\overline{SDE}$ pulsewidth	t_{CW}		200	–	–	ns
$\overline{SDE}$ rise time	t_{CR}		50	–	–	ns
$\overline{SDE}$ fall time	t_{CF}		50	–	–	ns
$\overline{SDE}$ to SCK setup time	t_{CSU}		200	–	–	ns
SCK to $\overline{SDE}$ hold time	t_{CH}		200	–	–	ns

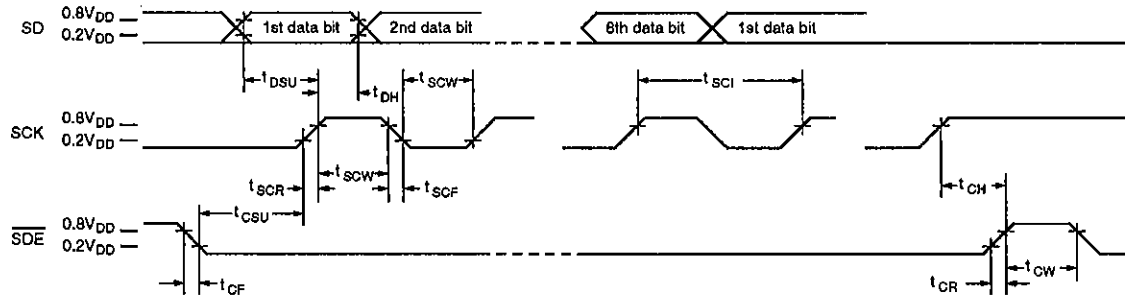
VCR sync pulse



Television sync pulse



Serial interface



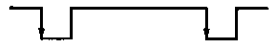
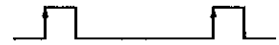
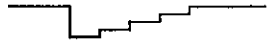
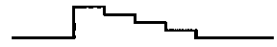
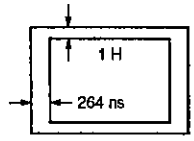
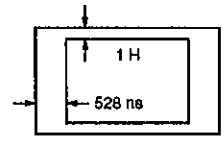
Functional Description

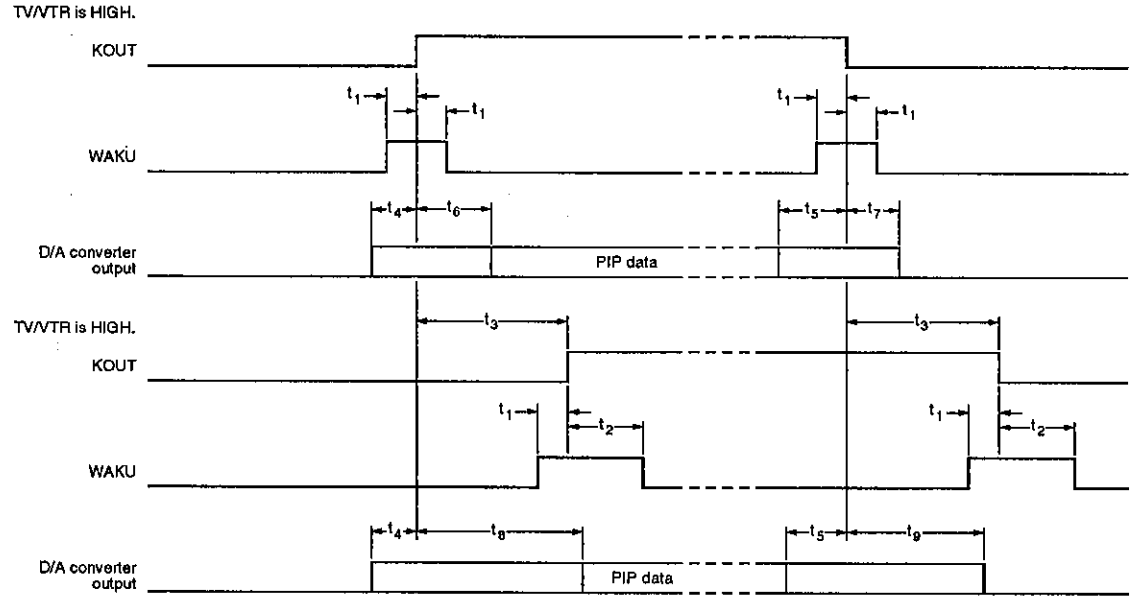
NTSC/PAL

NTSC/PAL should be tied HIGH for NTSC, and LOW, for PAL.

TV/VTR

TV/VTR should be tied HIGH for television mode, and LOW, for VCR mode. The differences between the two modes are shown in the following table and figure.

Parameter	Television (TV/VTR is HIGH)	VCR (TV/VTR is LOW)
Horizontal and vertical sync polarity	Negative 	Positive 
Y-signal D/A converter output polarity	–Y 	Y 
WAKU output vertical frame		
KOUT, WAKU and D/A converter output timing	Output simultaneously	KOUT and WAKU delayed 528 ns



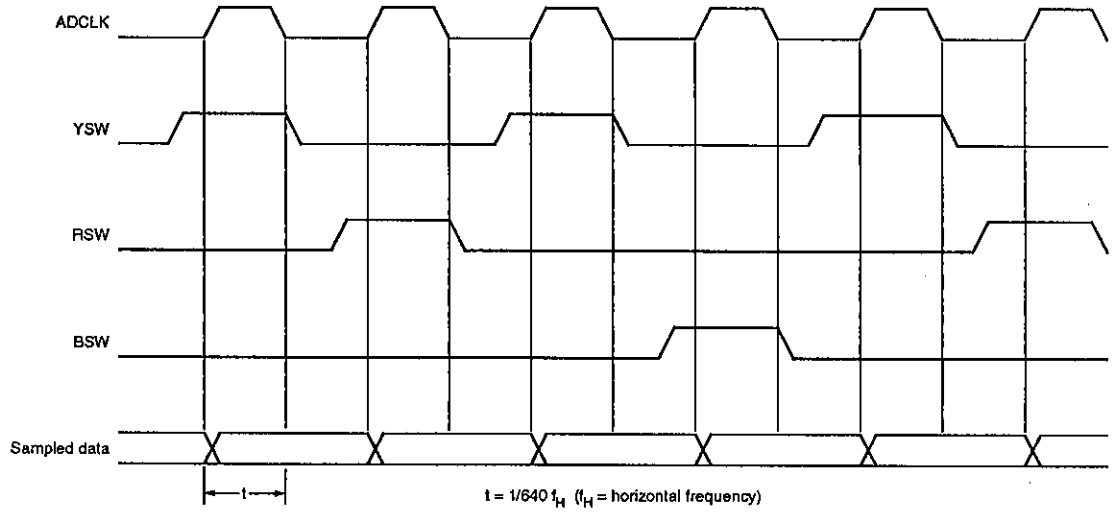
Note

The shaded D/A converter outputs indicate frame data. t_1 = 132 ns, t_2 = 396 ns, t_3 = 528 ns, t_4 = 176 ns, t_5 = 308 ns, t_6 = 352 ns, t_7 = 220 ns, t_8 = 616 ns and t_9 = 484 ns

A/D Converter Interface

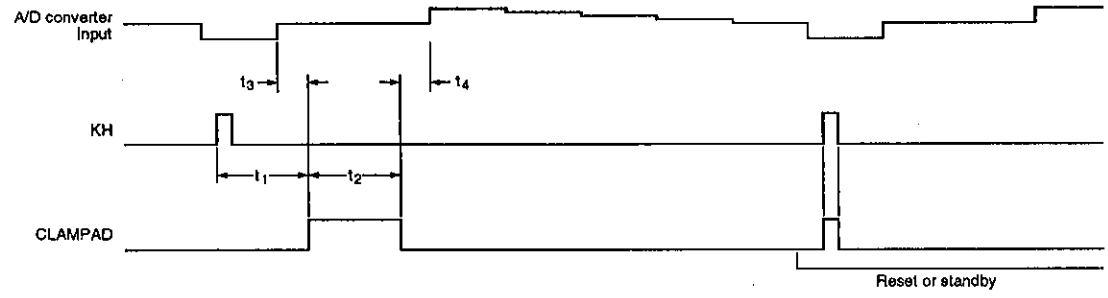
The PIP controller interfaces with an LC7480 multiplexing A/D converter using the AD0 to AD5 and VREF inputs and CLAMPAD, YSW, RSW, BSW and ADCLK outputs. The LC7480 converts the Y, R – Y and B – Y video signals into 6-bit digital data which is input to the PIP on AD0 to AD5. YSW, RSW and BSW control the LC7480 input multiplexer. The conversion sequence is Y, R – Y, Y, B – Y, as shown in the following figure. The conversion frequencies are shown in the following table.

The LC7441 and LC7480 should be mounted as closely as possible and care taken with the PCB layout because of the high signal frequencies.



System	Conversion frequency (MHz)			
	Total (f_T = 320f_H)	Y (f_{TY} = 160f_H)	R – Y (f_{TR} = 80f_H)	B – Y (f_{TB} = 80f_H)
NTSC (f_H = 15,734 Hz)	5.035	2.517	1.258	1.258
PAL (f_H = 15,625 Hz)	5.000	2.500	1.250	1.250

The CLAMPAD output pulse follows the KH input pulse. CLAMPAD should be HIGH during the horizontal blanking period as shown in the following figure. Note that when KH is HIGH during reset or standby, CLAMPAD is HIGH.



Note

t_1 = 5.6 µs, t_2 = 2.4 µs, t_3 > 0 µs and t_4 > 0.5 µs

On-chip D/A Converters

The normal D/A converter clock frequencies and the clock frequencies when the RAR (Revise Aspect Ratio) register is HIGH are shown in tables 1 and 2, respectively.

Table 1. D/A converter clock frequency

System	Clock frequency (MHz)		
	Y (f_{CY} = 480f_H)	R – Y (f_{CR} = 240f_H)	B – Y (f_{CB} = 240f_H)
NTSC (f_H = 15,734 Hz)	7.552	3.776	3.776
PAL (f_H = 15,625 Hz)	7.500	3.750	3.750

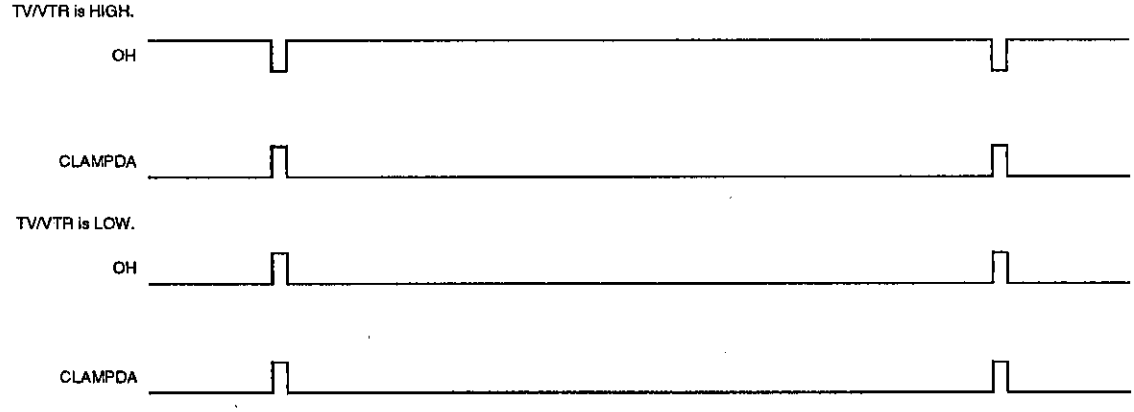
Table 2. Changing clock frequency with RAR

RAR register	NTSC/PAL Input	Y	R – Y	B – Y
LOW	×	480f_H	240f_H	240f_H
HIGH	LOW	416f_H	208f_H	208f_H
HIGH	HIGH	565f_H	283f_H	283f_H

Note

× = don't care

CLAMPDA is HIGH during main-screen horizontal sync pulses, as shown in the following figure.



The D/A converter data when the sub-screen is not displayed are shown, msb first, in the following table. Note that when TV/VTR is HIGH, the Y signal is output as –Y, and when LOW, as Y.

Output	D/A converter data	
	TV/VTR is HIGH	TV/VTR is LOW
YAOUT	111111	000000
RAOUT	100000	100000
BAOUT	100000	100000

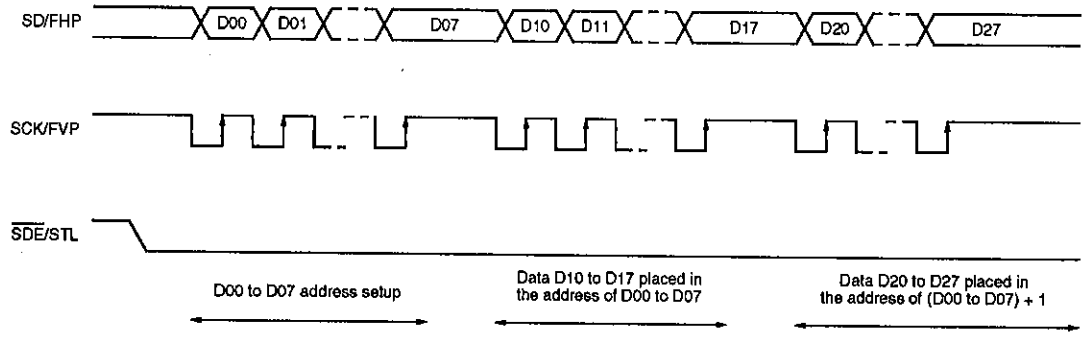
Dual-function Inputs

Input logic levels select sub-screen display parameters when SER/PIN is LOW, and serial data and input logic levels, when SER/PIN is HIGH, as shown in the following table.

Pin	SER/PIN	
	LOW	HIGH
SCK/FVP	Sub-screen vertical position select	Serial data clock
SD/FHP	Sub-screen horizontal position select	Serial data
$\overline{\text{SDE}}$/STL	Still/active display select	Serial data enable
KDIS	Sub-screen ON/OFF select	Initial sub-screen ON/OFF selection when controller is reset
WK	Sub-screen frame ON/OFF select	Initial sub-screen frame ON/OFF selection when controller is reset

Serial Data Interface

When SER/PIN is HIGH, SD/FHP, SCK/FVP and $\overline{\text{SDE}}$/STL function as the serial-interface data, clock and data-enable inputs, respectively, as shown in the following figure. After $\overline{\text{SDE}}$/STL goes LOW, data bits D00 to D07 are the internal register address, and D10 to D17, the register data. After the data has been received, the address is automatically incremented, and D20 to D27 are the data for the next register. After $\overline{\text{SDE}}$/STL goes from LOW to HIGH to LOW, address selection re-occurs.



Internal Registers

The internal control registers are shown in the following table. Note that the lower four bits of the address byte determine the register address, and the upper four bits are ignored.

Address	Bit position							
	7	6	5	4	3	2	1	0
0H	SBY	WKVAR	FILD	KOUT	POSVAR	STL	FVPR	FHPR
1H	SBY	PRI	KOUT2	KOUT1	STL2	STL1	FVPR	FHPR
8H	VWIPE	HWIPE	VP5	VP4	VP3	VP2	VP1	VP0
9H	RAR	MUL	HP5	HP4	HP3	HP2	HP1	HP0
AH	WK2	WK1	YWK5	YWK4	YWK3	YWK2	YWK1	YWK0
BH	WKVAR2	WKVAR1	RWK5	RWK4	RWK3	RWK2	RWK1	RWK0
CH	VDFS1	VDFS0	BWK5	BWK4	BWK3	BWK2	BWK1	BWK0

Reset and Standby Modes

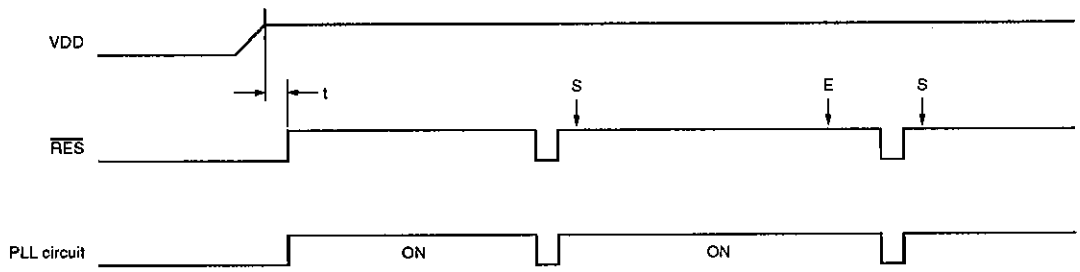
The controller is reset by holding $\overline{RES}$ LOW and put in standby mode by either holding $\overline{SBY}$ LOW or setting the SBY register HIGH. The PLLs are stopped and the internal registers set as shown in the following table. Note that the input levels are used to determine some initial register values. For example, if KDIS is LOW when $\overline{RES}$ is brought LOW, then the KOUT, KOUT1 and KOUT2 registers are set LOW.

Register	Reset	Standby
SBY	LOW	–
WKVAR, WKVAR1, WKVAR2	LOW	–
FILD	LOW	–
KOUT, KOUT1, KOUT2	KDIS	KDIS
POSVAR	LOW	–
STL, STL1, STL2	$\overline{SDE}$/STL	$\overline{SDE}$/STL
FVPR	SCK/FVP	SCK/FVP
FHPR	SD/FHP	SD/FHP
PRI	HIGH	–

Register	Reset	Standby
VWIPE	LOW	–
HWIPE	LOW	–
VP0 to VP5	–	–
HP0 to HP5	–	–
WK1, WK2	WK	–
VDFS1	LOW	–
VDFS0	HIGH	–
YWK0 to YWK5	–	–
RWK0 to RWK5	–	–
BWK0 to BWK5	–	–
MUL, RAR	LOW	–

Note
– Register unchanged

At power-up, hold $\overline{RES}$ LOW for several microseconds after the power supply stabilizes as shown in the following figure. Note that S and E represent the start and the end of PIP controller operation, respectively.



Register data can be written when the controller is in standby mode, but memory data is lost because the PLLs are stopped and the memory is not refreshed.

Dual-port RAM Interface

The dual-port RAM interface comprises the SODI0 to SODI3 inputs and A0 to A7, WDO0 to WDO3, $\overline{WE}$, $\overline{DT}$, $\overline{RAS}$, $\overline{CAS}$ and SC outputs.

The LC7441 and the dual-port RAM should be mounted as closely as possible and care taken with the PCB layout because of the high speed of memory accesses.

The data read, memory refresh and data transfer waveforms are shown in figures 1, 2 and 3, respectively. Note that when RAR is HIGH, $t = 1/1696f_H$ if NTSC/PAL is also HIGH, and $t = 1248f_H$ if NTSC/PAL is LOW.

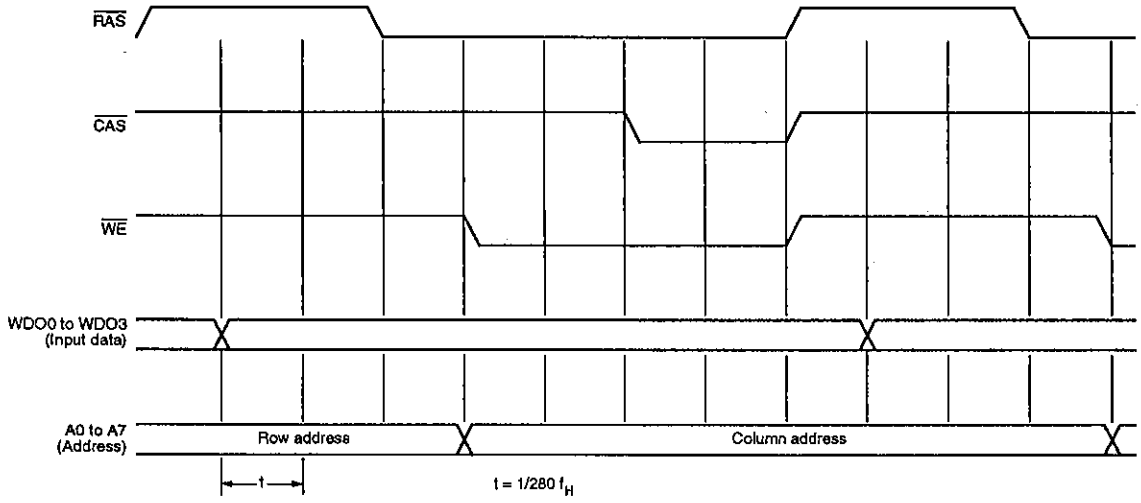


Figure 1. Data read

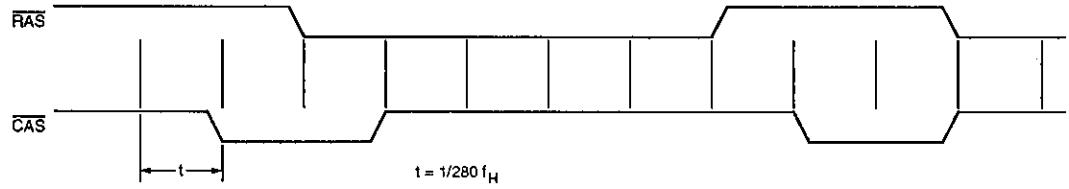


Figure 2. $\overline{CAS}$ before $\overline{RAS}$ memory refresh

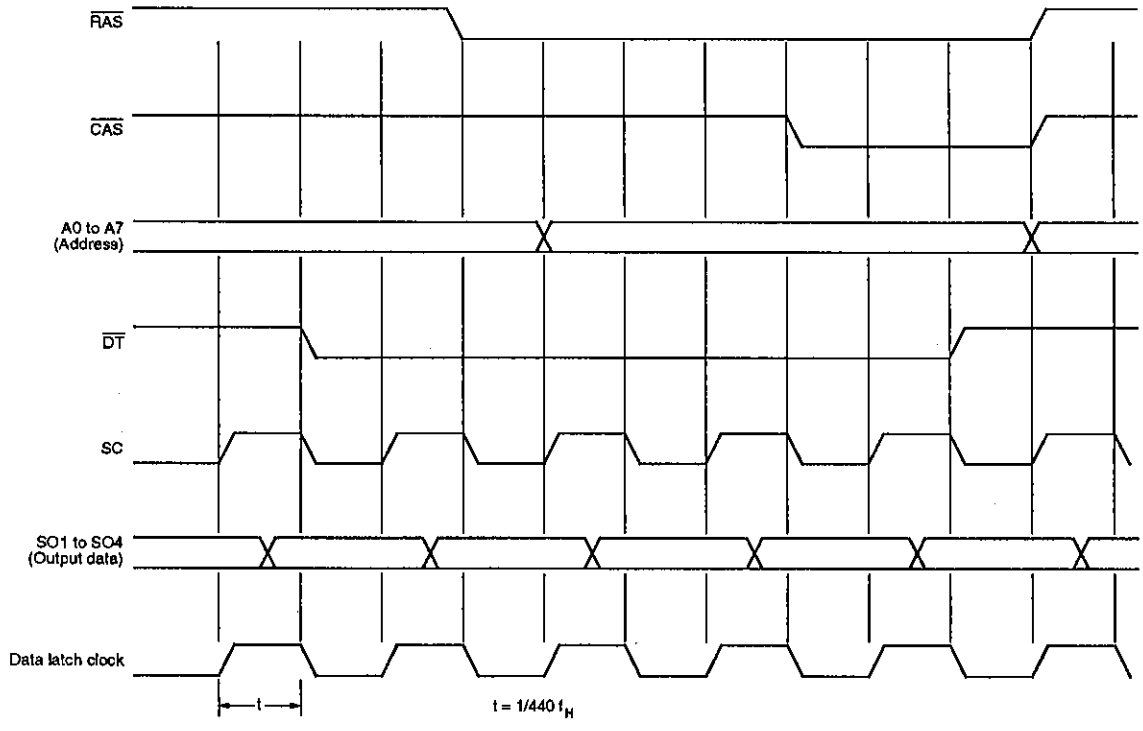


Figure 3. Data transfer

Memory Write Range

The horizontal memory-write range is 252 dots comprising 126, 63 and 63 dots of Y, R – Y and B – Y data, respectively. The NTSC and PAL vertical memory-write ranges are 80 and 85 horizontal lines, respectively, as shown in figures 4 and 5, respectively.

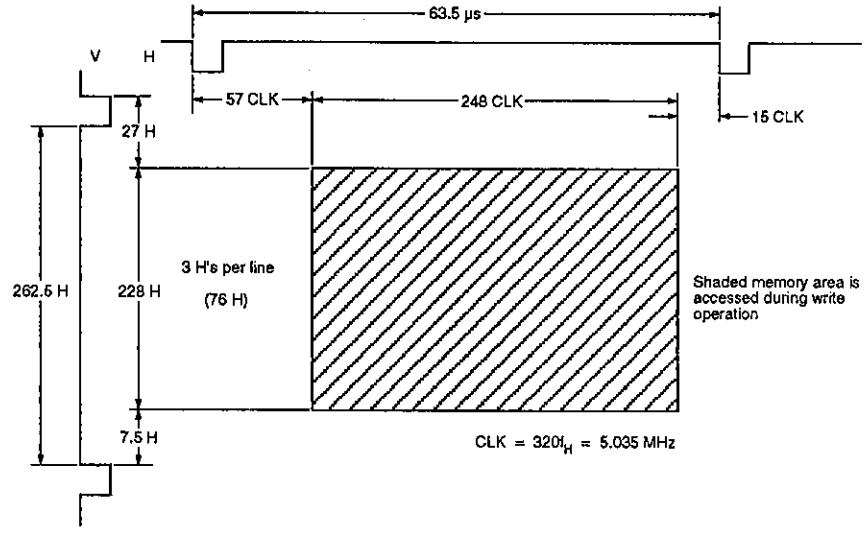


Figure 4. NTSC memory write range

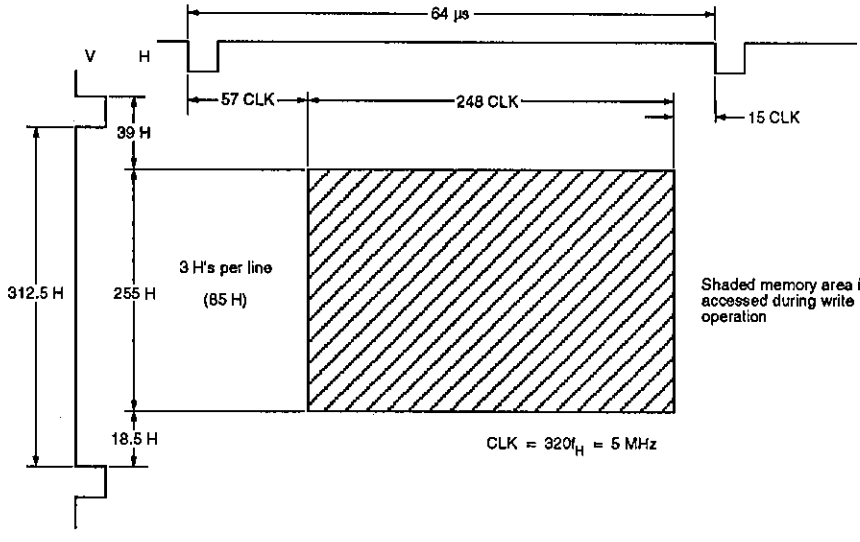


Figure 5. PAL memory write range

Memory Readout Range

The horizontal memory-readout range is 244 dots comprising 122, 61 and 61 dots of Y, R – Y and B – Y data, respectively. The NTSC and PAL vertical memory readout ranges are 77 and 83 horizontal lines, respectively, as shown in figures 6 and 7, respectively.

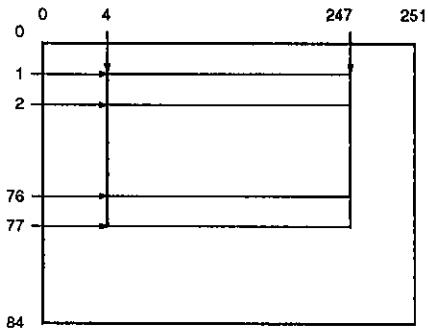


Figure 6. NTSC memory readout range

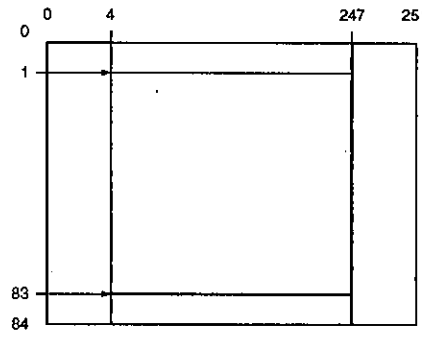


Figure 7. PAL memory readout range

Sync Signals

The PCB layout should not allow noise to be induced in the OH, OV, KH and KV signals from the sync-separator IC because this can cause screen distortion. The sub-screen display should be turned off when the sync signals become unstable because the display can become distorted. The OH and KH input signals should lag the video horizontal sync signals by 1 µs as shown in the following figure.

Note
$t_w > 1$ µs

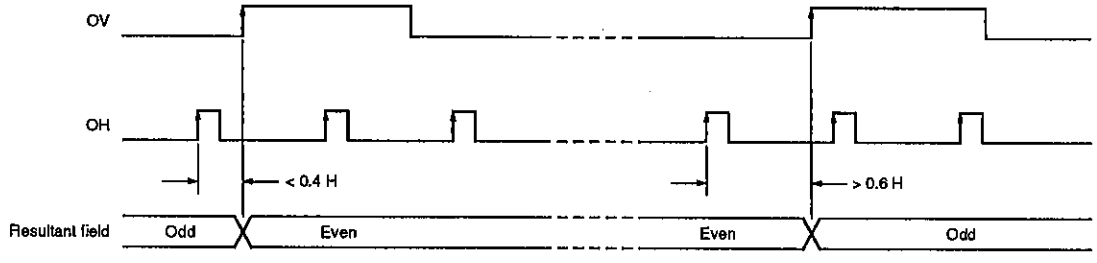
PLLOH

The read-PLL locks to the main-screen horizontal sync frequency when PLLOH is HIGH, and to the sub-screen horizontal sync frequency, when PLLOH is LOW. Using a PLL clock to generate the horizontal sync signal and determine the sub-screen display position results in an error-free display.

PLLOH is normally held HIGH. However, when OH is unstable, PLLOH should be held LOW, otherwise the PLL clock becomes unstable and the sub-screen flickers.

Odd-field Decision Circuits

The OH/OV and KH/KV odd-field decision circuits measure the phase difference between the horizontal and vertical sync pulses as shown in the following figure. When the field is odd, a single output horizontal sync pulse is blanked during the vertical sync pulse period, and when even, two are blanked. The phase difference is measured between the falling edges of the sync pulses when TV/VTR is HIGH, and between the rising edges, when TV/VTR is LOW.



Operating Information

The LC7441 operates under input pin control when SER/PIN is LOW, and under serial control, when SER/PIN is HIGH. It can display one sub-screen when under input pin control, and either one or two sub-screens, when under serial control.

Single- or Dual-screen Operation Under Serial Control

Writing register data to address 0 selects single-screen mode, and writing data to address 1, dual-screen mode. The registers selecting single-screen parameters are VWIPE, HWIPE and the address 0 registers. The registers selecting dual-screen parameters are WKVAR1, WKVAR2 and the address 1 registers.

Sub-screen ON/OFF

Pin control

The sub-screen is ON when the KDIS input is HIGH, and OFF, when LOW.

Serial control, single screen

The sub-screen is ON when KOUT is HIGH, and OFF, when LOW.

Serial control, dual screen

Sub-screen 1 is ON when KOUT1 is HIGH, and OFF, when LOW. Sub-screen 2 is ON when KOUT2 is HIGH, and OFF, when LOW.

Sub-screen Position

The sub-screen position can be fixed or variable. The four fixed positions are shown in figure 8, and the variable position, which is determined by the VP0 to VP5 and HP0 to HP5 registers as follows, in figure 9.

$$VP = ((VP0 \text{ to } VP5) + 1) \times 5H + 3H$$

$$HP = ((HP0 \text{ to } HP5) + 6) \times \frac{1}{60f_H}$$

Note that variable positions outside the main-screen area are ignored.

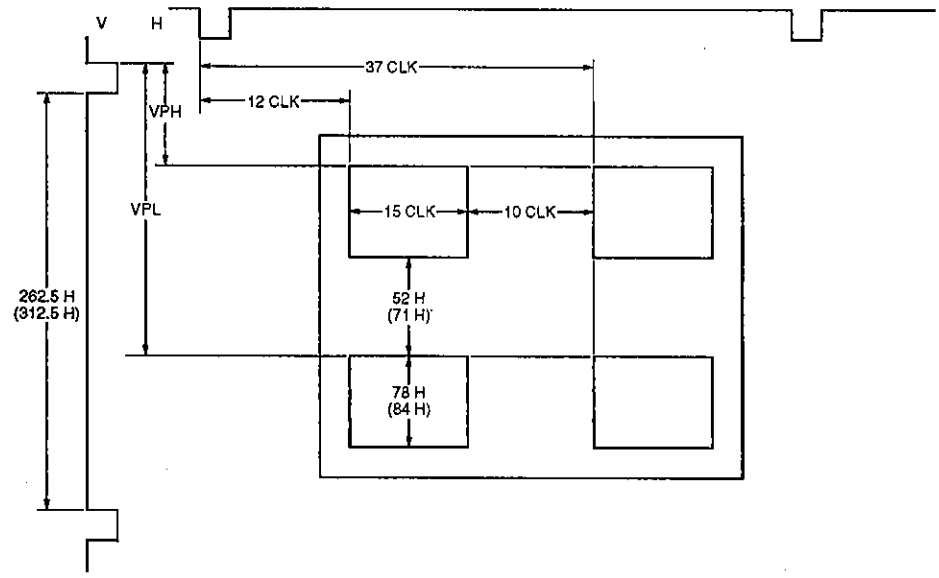


Figure 8. Sub-screen positions

Note
Figures in brackets apply to PAL displays.

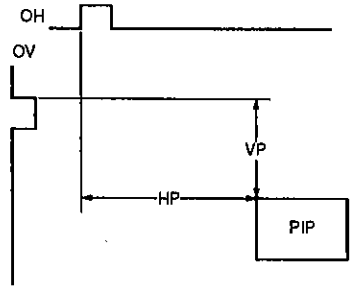


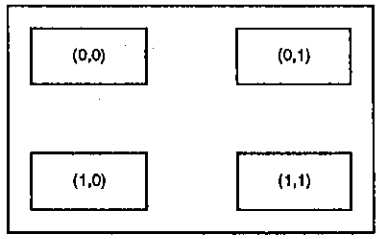
Figure 9. Variable screen position

RAR register	NTSC/PAL input	Read-VCO frequency	CLK frequency
LOW	LOW	$1,440f_H$	$60f_H$
LOW	HIGH	$1,440f_H$	$60f_H$
HIGH	LOW	$1,248f_H$	$52f_H$
HIGH	HIGH	$1,696f_H$	$70.7f_H$

Note
Normal write-VCO frequency is $1280f_H$.

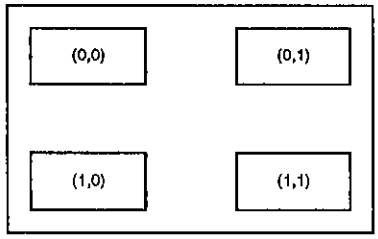
Pin control

The sub-screen position is determined by the SCK/FVP and SD/FHP input levels as shown in the following figure. (SCK/FVP, SD/FHP)



Serial control, single screen

The sub-screen position is variable when POSVAR is HIGH, and fixed, when LOW. The fixed screen position is determined by FVPR and FHPR at address 0 as shown in the following figure.



Serial control, dual screen

The screen 1 position is fixed, and is determined by FVPR and FHPR at address 1. The screen 2 position is variable, and is determined by VP0 to VP5 and HP0 to HP5.

Sub-screen Frame

The sub-screen, or screens, can have no frame, a white frame or a colored frame. The D/A converter registers YWK0 to YWK5, RWK0 to RWK5 and BWK0 to BWK5 are used to set the frame color. The white frame corresponds to YWK, RWK and BWK data values of 110000, 100000 and 100000, respectively.

Pin control

The frame, which is always white, is ON when the WK input is HIGH, and OFF, when LOW.

Serial control, single screen

The frame is ON when the WK input is HIGH, and OFF, when LOW. The frame color is set using the frame-color registers when WKVAR is HIGH, and white, when LOW. When register FILD is HIGH, the field screen is displayed; when LOW, the frame screen is displayed.

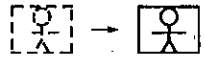
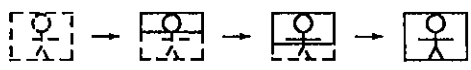
Serial control, dual-screen

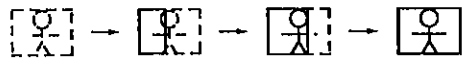
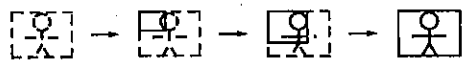
The screen 1 frame is ON when WK1 is HIGH, and OFF, when LOW. The screen 2 frame is ON when WK2 is HIGH, and OFF, when LOW.

The screen 1 frame color is set using the frame-color registers when WKVAR1 is HIGH, and white, when LOW. The screen 2 frame color is set using the frame-color registers when WKVAR2 is HIGH, and white, when LOW.

Wipe Function

The wipe function allows gradual display or erasure of the sub-screen when in serial control, single-screen mode. Wipe direction is set using the VWIPE and HWIPE registers as shown in the following table. When wiping is OFF, the sub-screen turns ON and OFF instantaneously, otherwise screen display and erasure occurs in 64 stages over approximately one second. Note that screen erasure is in the reverse sequence to display.

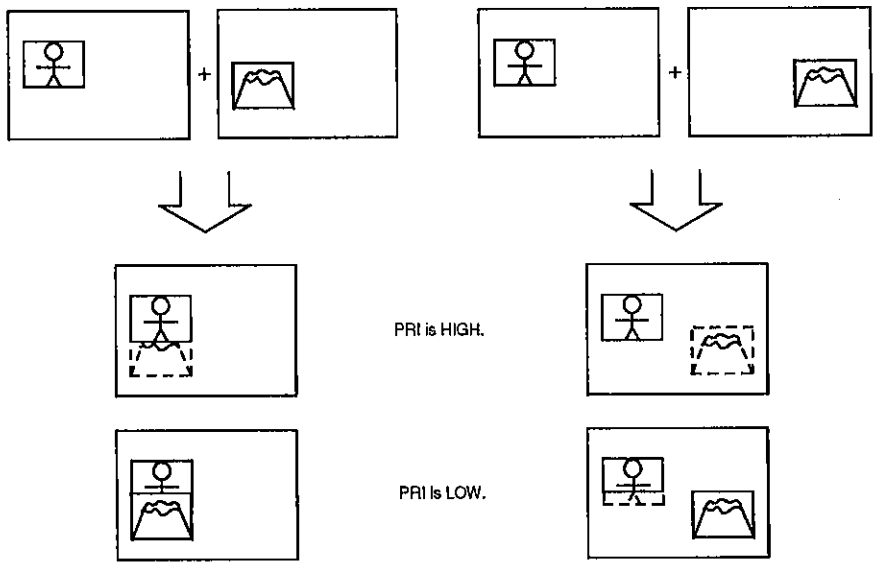
VWIPE	HWIPE	Operation
LOW	LOW	 Wipe off
HIGH	LOW	

VWIPE	HWIPE	Operation
LOW	HIGH	
HIGH	HIGH	

Dual-screen Priority

When the dual screens overlap vertically, the priority of screen display is determined by the PRI register. The higher screen has priority when PRI is HIGH, and the lower screen, when LOW as shown in the following figure.

When the higher screen has priority, the lower screen is OFF, and when the lower screen has priority, the higher screen display ends at the first overlapped screen line. Note that prioritized display occurs even if the screens do not superimpose and that side-by-side sub-screens cannot be displayed.



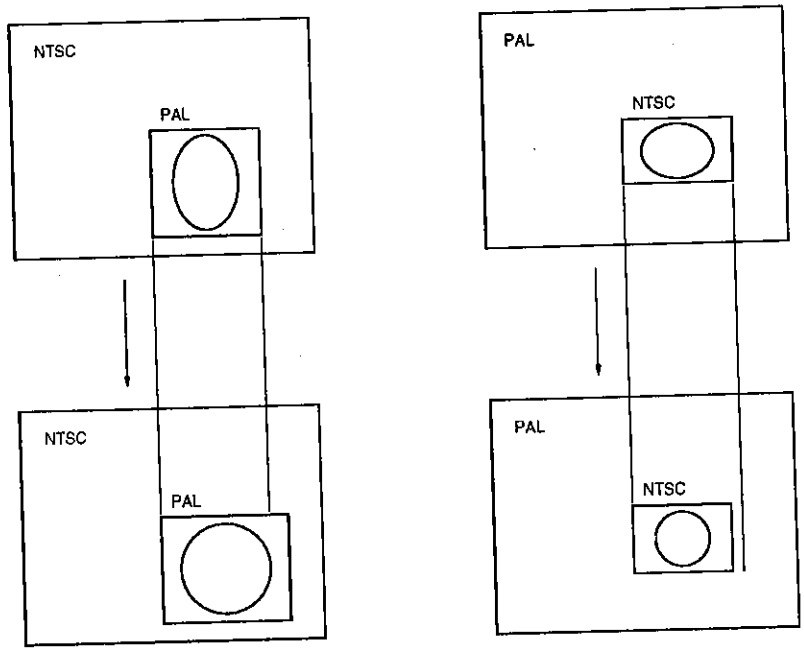
Note
The dotted areas do not display.

Multi-system Display

Multi-system mode is selected when the MUL register is HIGH, and single-system mode, when LOW. In multi-system mode, the fixed vertical positions correspond to the main-screen system, and in single-system mode, to the sub-screen system, as shown in the following table.

MUL register	NTSC/PAL Input	VPH	VPL
LOW	LOW	48H	198H
LOW	HIGH	43H	158H
HIGH	LOW	43H	158H
HIGH	HIGH	48H	198H

A PAL sub-screen expands vertically in a multi-system display and an NTSC sub-screen contracts because the two systems use a different number of scan lines. These changes in the sub-screen aspect ratios are corrected using the RAR (Revise Aspect Ratio) register, as shown in the following figure. When RAR is HIGH, the horizontal clock frequency is adjusted to correct the aspect ratio.



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