

Ordering number : EN4453A

CMOS IC



LC74760, 74760M

On-Screen Display IC

Overview

The LC74760 and LC74760M are on-screen display CMOS ICs that superimpose text and low-level graphics onto a TV screen (video signal) under microprocessor control. The display characters have a 12 by 18 dot structure, and 128 characters are provided. The display area consists of 12 lines of 24 characters each.

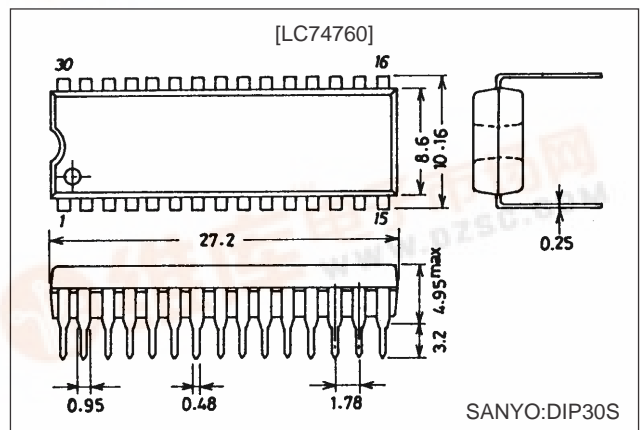
Features

- Display structure: 12 lines by 24 characters (up to 288 characters)
- Number of displayed characters: Up to 288 characters
- Character configuration: 12 (W) by 18 (H) dot structure
- Character sizes: Three sizes (normal, double, and triple sizes)
- Display starting positions: 64 horizontal and 64 vertical locations
- Reverse video function: Characters can be inverted on a per character basis.
- Flashing types: Two types with periods of 0.5 and 1.0 second on a per character basis (duty fixed at 50%)
- Background color: One of eight colors (when internal synchronization used)
- External control input: Serial data input in 8-bit units
- Built-in horizontal/vertical sync separation circuit, AFC circuit, and synchronization detector
- Video output: Composite video signal output in NTSC, PAL, PAL-M, PAL-N, PAL60, NTSC4.43, or SECAM format

Package Dimensions

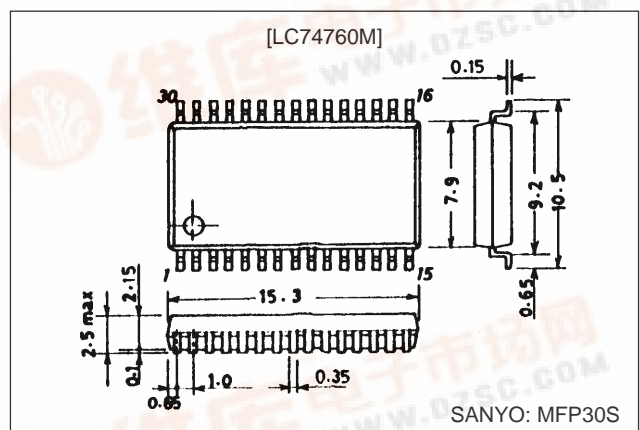
unit: mm

3061-DIP30S



unit: mm

3073A-MFP30S



LC74760, 74760M

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V _{DD} max	V _{DD1} , V _{DD2} pins	V _{SS} - 0.3 to V _{SS} + 7.0	V
Maximum input voltage	V _{IN} max	All input pins	V _{SS} - 0.3 to V _{DD} + 0.3	V
Maximum output voltage	V _{OUT} max	HSYNC _{OUT} , VSYNC _{OUT} , SYNC _{DET} pins	V _{SS} - 0.3 to V _{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta = -30 to +70°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V _{DD1}	V _{DD1} pin	4.5	5.0	5.5	V
	V _{DD2}	V _{DD2} pin	4.5	5.0	1.27 V _{DD1}	V
Input high level voltage	V _{IH1}	R _{ST} , CS, SIN, SCLK pins	0.8 V _{DD1}		V _{DD1} + 0.3	V
	V _{IH2}	SECAM, 525/625, NTSC/PAL, 3.58/4.43 pins	0.7 V _{DD1}		V _{DD1} + 0.3	V
Input low level voltage	V _{IL1}	R _{ST} , CS, SIN, SCLK	V _{SS} - 0.3		0.2 V _{DD1}	V
	V _{IL2}	SECAM, 525/625, NTSC/PAL, 3.58/4.43 pins	V _{SS} - 0.3		0.3 V _{DD1}	V
Input voltage	V _{IN}	FC, AMP _{IN} pins	V _{SS} - 0.3		V _{DD1} + 0.3	V
Composite video signal input voltage	V _{IN1}	CV _{IN} pins		2 V _{PP}		V
	V _{IN2}	CV _{CR} pins		2 V _{PP}		V
	V _{IN3}	SYNC _{IN} pins		2 V _{PP}	2.5 V _{PP}	V
Oscillator frequency	F _{OSC1}	Xtal _{IN1} , Xtal _{OUT1} pins; 4fsc: NTSC		14.318		MHz
		Xtal _{IN2} , Xtal _{OUT2} pins; 4fsc: PAL		17.734		MHz
	F _{OSC2}	Xtal _{IN2} , Xtal _{OUT2} pins; 4fsc: PAL-M		14.302		MHz
		Xtal _{IN2} , Xtal _{OUT2} pins; 4fsc: PAL-N		14.328		MHz

Electrical Characteristics at Ta = -30 to +70°C, with V_{DD1} = V_{DD2} = 5 V unless otherwise specified

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output off leakage current	I _{leak1}	CV _{OUT} pin			10	μA
Input off leakage current	I _{leak2}	CV _{IN} , CV _{CR} pins			10	μA
Output high level voltage	V _{OH}	HSYNC _{OUT} , VSYNC _{OUT} , SYNC _{DET} , SECAM, 525/625, NTSC/PAL, 3.58/4.43, AMP _{OUT} , PD _{OUT} pins; V _{DD1} = 4.5 V, I _{OH} = -1.0 mA	3.5			V
Output low level voltage	V _{OL}	HSYNC _{OUT} , VSYNC _{OUT} , SYNC _{DET} , SECAM, 525/625, NTSC/PAL, 3.58/4.43, AMP _{OUT} , PD _{OUT} pins; V _{DD1} = 4.5 V, I _{OL} = 1.0 mA			1.0	V
Input current	I _{IH}	R _{ST} , CS, SIN, SCLK, SECAM, 525/625, NTSC/PAL, 3.58/4.43 pins; V _{IN} = V _{DD1}			1	μA
	I _{IL}	SECAM, 525/625, NTSC/PAL, 3.58/4.43 pin; V _{IN} = V _{SS1}	-1			μA
Oscillator frequency	F _{OSC3}	VCO _{IN} , VCO _{OUT} pins; FC = 1/2 V _{DD1}		14.12		MHz
Operating current dissipation	I _{DD1}	V _{DD1} pin; All outputs open, Xtal: 4fsc			15	mA
	I _{DD2}	V _{DD2} pin; V _{DD2} = 5.0 V			20	mA

Timing Characteristics at Ta = -30 to +70°C, V_{DD} = 5 ± 0.5 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Minimum input pulse width	t _{W(SCLK)}	SCLK pin	200			ns
	t _{W(CS)}	CS pin (during periods when CS is high)	1			μs
Data setup time	t _{SU(CS)}	CS pin	200			ns
	t _{SU(SIN)}	SIN pin	200			ns
Data hold time	t _{H(CS)}	CS pin	2			μs
	t _{H(SIN)}	SIN pin	200			ns
One word write time	t _{word}	Write time for 8 bits of data	4.2			μs
	t _{wt}	RAM data write time	1			μs

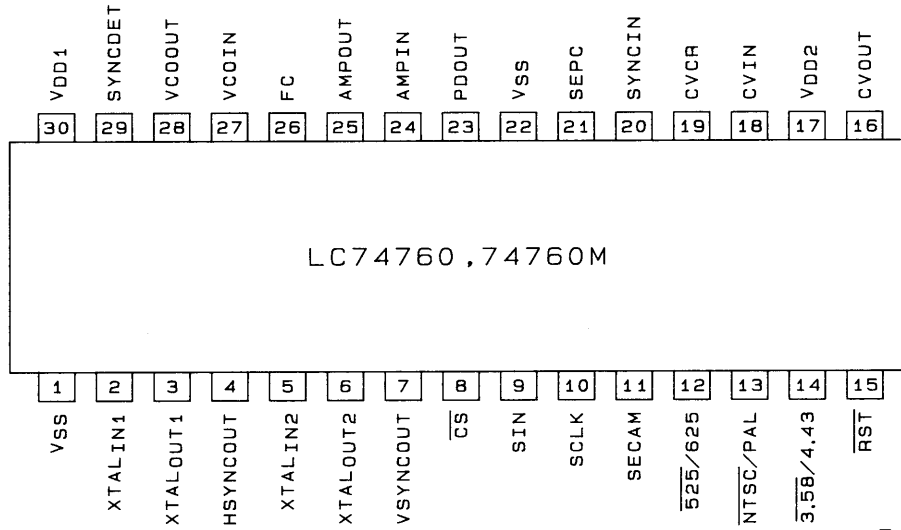
LC74760, 74760M

Pin Functions

Pin No.	Symbol	Function	Description
1	V _{SS}	Ground	Ground connection
2	Xtal _{IN1}	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal. (For an NTSC crystal oscillator 4fsc = 14.318 MHz.)
3	Xtal _{OUT1}		
4	HSYNC _{OUT}	Horizontal synchronization output	Outputs the horizontal synchronization signal (AFC). The polarity can be selected with a metal switch.
5	Xtal _{IN2}	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal. (For a PAL crystal oscillator 4fsc = 17.734 MHz.)
6	Xtal _{OUT2}		
7	VSYNC _{OUT}	Vertical synchronization output	Outputs the vertical synchronization signal. The polarity can be selected with a metal switch.
8	$\overline{\text{CS}}$	Enable input	Enables/disables serial data input. Serial data is enabled when this pin is low. Pull-up resistor built in (hysteresis input).
9	SIN	Data input	Serial data input. Pull-up resistor built in (hysteresis input).
10	SCLK	Clock input	Clock input for serial data input. Pull-up resistor built in (hysteresis input).
11	SECAM	SECAM mode switch input	Switches between SECAM and other modes. Low = other modes, high = SECAM mode
12	$\overline{525/625}$	525/625 switch input	Switches between 525 scan lines and 625 scan lines. Low = 525 lines, high = 625 lines
13	$\overline{\text{NTSC/PAL}}$	NTSC/PAL switch input	Switches the color mode between NTSC and PAL. Low = NTSC, high = PAL
14	$\overline{3.58/4.43}$	3.58/4.43 switch input	Switch FSC between 3.58 MHz and 4.43 MHz. Low = 3.58, high = 4.43
15	$\overline{\text{RST}}$	Reset input	System reset input pin, low is active (reset). Pull-up resistor built in (hysteresis input).
16	CV _{OUT}	Video signal output	Composite video output
17	V _{DD2}	Power supply connection	Power supply connection for composite video signal level generation
18	CV _{IN}	Video signal input	Composite video input
19	CV _{CR}	Video signal input	SECAM chroma signal input
20	SYNC _{IN}	Sync separator circuit input	Built-in sync separator circuit video signal input
21	SEP _C	Sync separator circuit	Built-in sync separator circuit (AMP out)
22	V _{SS}	Ground	Ground connection
23	PD _{OUT}	Control voltage output	AFC control voltage output
24	AMP _{IN}	AFC filter connection	Filter connection
25	AMP _{OUT}		
26	FC	Control voltage input	AFC control voltage input
27	VCO _{IN}	LC oscillator connection	VCO LC oscillator circuit coil and capacitor connection
28	VCO _{OUT}		
29	SYNC _{DET}	External synchronization signal detection output	Outputs the exclusive NOR of the horizontal synchronization signal (AFC) and CSYNC (sync separator).
30	V _{DD1}	Power supply connection	Power supply connection (+5 V: digital system power supply)

LC74760, 74760M

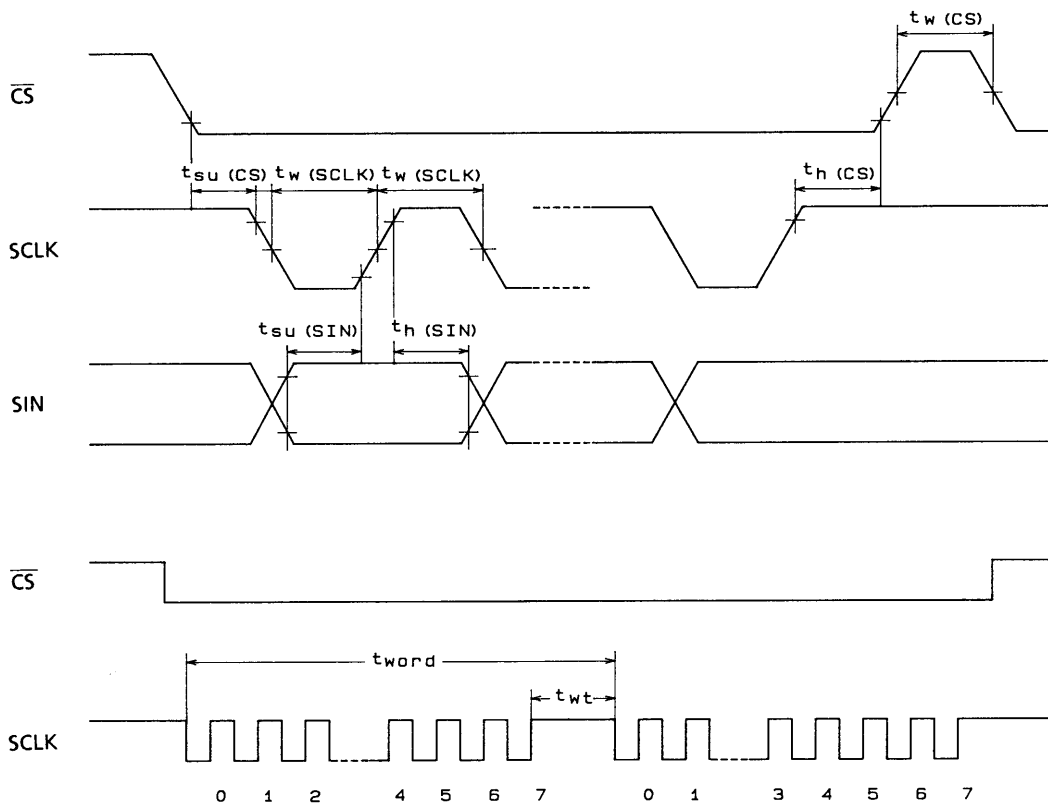
Pin Assignment



Top view

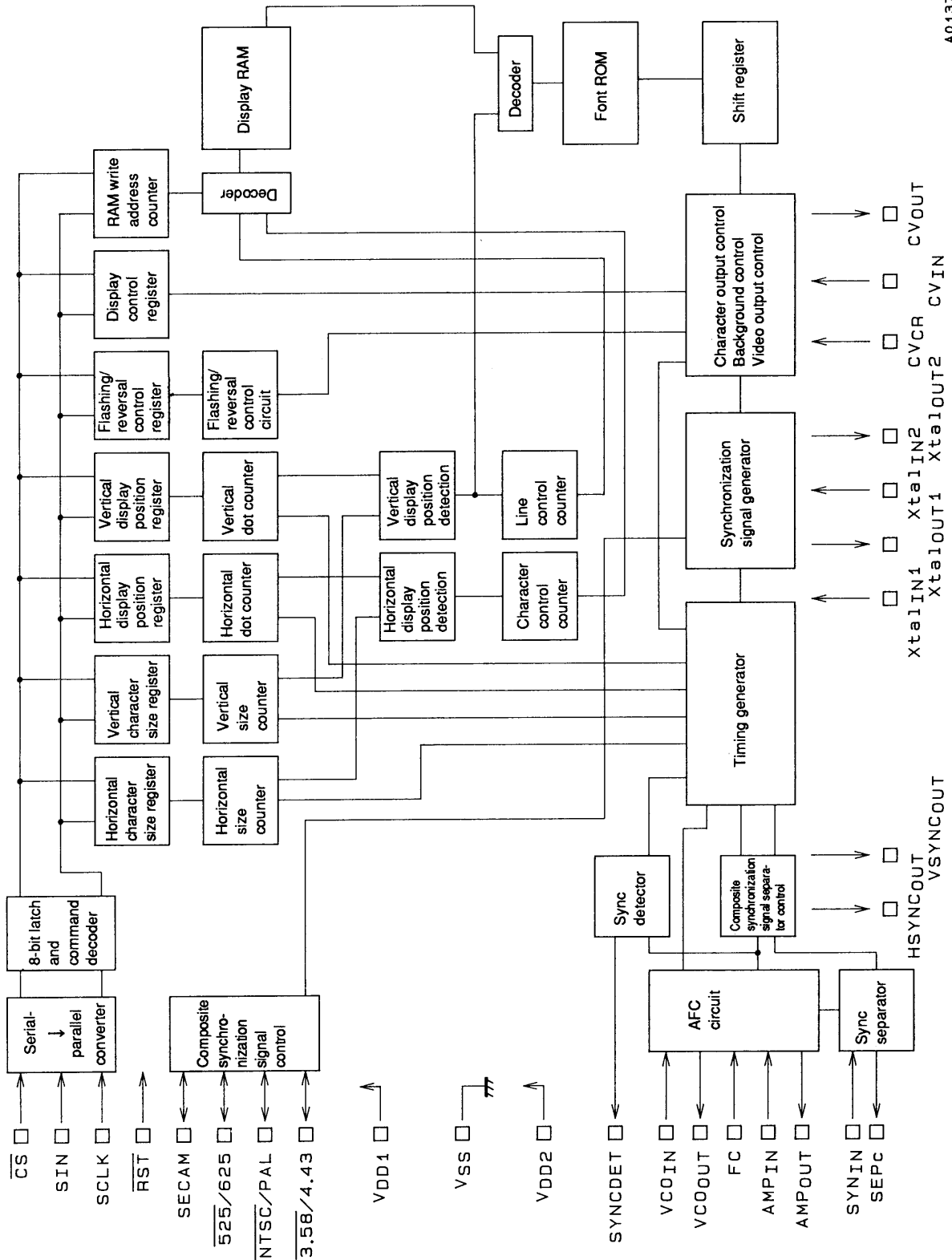
A01374

Serial Data Input Timing



A01375

System Block Diagram



LC74760, 74760M

Display Control Commands

Display control commands are input in an 8-bit serial format. Commands consist of a command identification code in the first byte and data in the second and following bytes. The following commands are supported.

- 1 COMMAND0: Display memory (VRAM) write address setting command
- 2 COMMAND1: Display character data write command
- 3 COMMAND2: Vertical display start position and character size (lines 1 and 2) setting command
- 4 COMMAND3: Horizontal display start position and character size (lines 9 and 11) setting command
- 5 COMMAND4: Display control setting command 1
- 6 COMMAND5: Display control setting command 2
- 7 COMMAND6: Display control setting command 3
- 8 COMMAND7: Display control setting command 4

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Write address	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Character write	1	0	0	1	0	0	at2	at1	0	c6	c5	c4	c3	c2	c1	c0
COMMAND2 Vertical display start position	1	0	1	0	SZ 21	SZ 20	SZ 11	SZ 10	0	0	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Horizontal display start position	1	0	1	1	SZ B1	SZ B0	SZ 91	SZ 90	0	0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control 1	1	1	0	0	RST	RAM	OSC	RND	0	I/N	BLK 1	BLK 0	BK 1	ATS	0	DSP
COMMAND5 Display control 2	1	1	0	1	PH 2	PH 1	PH 0	I/E	0	TST	CHAL	BLK	RSL 1	RSL 0	0	0
COMMAND6 Display control 3	1	1	1	0	MOD 3	MOD 2	MOD 1	MOD 0	0	0	0	0	IOS	BCL 1	BCL 0	CB
COMMAND7 Display control 4	1	1	1	1	0	0	0	LINS	0	0	LIN 5	LIN 4	LIN 3	LIN 2	LIN 1	LIN 0

Once the command identification code in the first byte is written, it is stored internally until the first byte of the following command is written. However, when the display character data write command (COMMAND1) is written, the system becomes locked in display character data write mode, and the first byte cannot be overwritten.

When the \overline{CS} pin is set high the command state is set to COMMAND0, i.e., display memory write address setting mode.

1 COMMAND0: Display Memory Write Address Setting Mode

First data byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 0 identification code: sets the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (from 0 to B (hexadecimal))	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

LC74760, 74760M

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory character address (from 0 to 17 (hexadecimal))	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

2 COMMAND1: Display Character Data Write Command

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 1 identification code: sets the display memory write address.	When this command is entered, the chip locks in display character write mode until the CS pin is set high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	at2	0	Turns character attribute 2 off.	Specifies highlight or flashing.
		1	Turns character attribute 2 on.	
0	at1	0	Turns character attribute 1 off.	Specifies reverse video.
		1	Turns character attribute 1 on.	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Character code (from 00 to 7F (hexadecimal))	
6	c6	0		
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

LC74760, 74760M

3 COMMAND2: Vertical Display Position Setting Command

First byte

DA0 to DA7	Register name	Register content			Note									
		State	Function											
7	—	1	The command 2 identification code: sets the vertical display position.											
6	—	0												
5	—	1												
4	—	0												
3	SZ21	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZ20 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZ21 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZ20 \	0	1	SZ21 /	Normal size	Double size		Triple size	Normal size	Character size for the second line
		SZ20 \	0	1										
SZ21 /	Normal size	Double size												
	Triple size	Normal size												
1														
2	SZ20	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZ20 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZ21 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZ20 \	0	1	SZ21 /	Normal size	Double size		Triple size	Normal size	
		SZ20 \	0	1										
SZ21 /	Normal size	Double size												
	Triple size	Normal size												
1														
1	SZ11	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZ10 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZ11 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZ10 \	0	1	SZ11 /	Normal size	Double size		Triple size	Normal size	Character size for the first line
		SZ10 \	0	1										
SZ11 /	Normal size	Double size												
	Triple size	Normal size												
1														
0	SZ10	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZ10 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZ11 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZ10 \	0	1	SZ11 /	Normal size	Double size		Triple size	Normal size	
		SZ10 \	0	1										
SZ11 /	Normal size	Double size												
	Triple size	Normal size												
1														

Second byte

DA0 to DA7	Register name	Register content			Note
		State	Function		
7	—	0	Second byte identification code		
6	—	0			
5	VP5 (MSB)	0	The vertical display start position is given by $VS = H \times \left(\sum_{n=0}^5 2^n VP_n \right)$ where H is the horizontal synchronization pulse period.		The six bits VP0 to VP5 specify the vertical display start position. The weight of the lsb is $1 \times H$.
		1			
4	VP4	0			
		1			
3	VP3	0			
		1			
2	VP2	0			
		1			
1	VP1	0			
		1			
0	VP0 (LSB)	0			
		1			

The diagram shows a vertical synchronization pulse (VSYNC) and a horizontal synchronization pulse (HSYNC). A vertical display area is defined by the VSYNC pulse, with a height labeled VS. Within this area, a character display area is shown with a horizontal width labeled HS. The HSYNC pulse is shown as a horizontal line above the display area.

Note: When the chip is reset by the \overline{RST} pin, the register states (bits) are all cleared to 0.

4 COMMAND3: Horizontal Display Position Setting Command

First byte

DA0 to DA7	Register name	Register content			Note									
		State	Function											
7	—	1	The command 3 identification code: sets the horizontal display position.											
6	—	0												
5	—	1												
4	—	1												
3	SZB1	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZB0 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZB1 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZB0 \	0	1	SZB1 /	Normal size	Double size		Triple size	Normal size	The character size for the eleventh line.
		SZB0 \	0	1										
SZB1 /	Normal size	Double size												
	Triple size	Normal size												
1														
2	SZB0	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZB0 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZB1 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZB0 \	0	1	SZB1 /	Normal size	Double size		Triple size	Normal size	
		SZB0 \	0	1										
SZB1 /	Normal size	Double size												
	Triple size	Normal size												
1														
1	SZ91	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZ90 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZ91 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZ90 \	0	1	SZ91 /	Normal size	Double size		Triple size	Normal size	The character size for the ninth line.
		SZ90 \	0	1										
SZ91 /	Normal size	Double size												
	Triple size	Normal size												
1														
0	SZ90	0	<table border="1" style="display: inline-table;"> <tr> <td style="text-align: center;">SZ90 \</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">SZ91 /</td> <td>Normal size</td> <td>Double size</td> </tr> <tr> <td></td> <td>Triple size</td> <td>Normal size</td> </tr> </table>		SZ90 \	0	1	SZ91 /	Normal size	Double size		Triple size	Normal size	
		SZ90 \	0	1										
SZ91 /	Normal size	Double size												
	Triple size	Normal size												
1														

LC74760, 74760M

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	HP5 (MSB)	0	<p>The horizontal display start position is given by</p> $HS = T_c \times \left(\sum_{n=0}^5 2^n \cdot HP_n \right)$ <p>where T_c is the period of the OSCIN and OSCOUT oscillator in operating mode.</p>	<p>The six bits HP0 to HP5 specify the vertical display start position. The weight of the lsb is $1 \times T_c$.</p>
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

5 COMMAND4: Display Control Setting Command 1

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 4 identification code: sets display control parameters.	
6	—	1		
5	—	0		
4	—	0		
3	RST _{SYS}	0		This reset occurs when the \overline{CS} pin goes low, and the reset state cleared when the \overline{CS} pin goes high.
		1	Resets all registers. (Clears all registers to 0.)	
2	RAM _{ERS}	0		The RAM erase function requires at least 500 μ s. It is executed on DSPOFF.
		1	Erases display RAM. (Sets display RAM to 7F (hexadecimal).)	
1	OSC _{STP}	0	Continues crystal oscillator operation.	Only valid with character display off if external synchronization is used.
		1	Stops the crystal oscillator.	
0	RND _{SEL}	0	Turns off rounding.	Only valid for double and triple size characters.
		1	Turns on rounding.	

LC74760, 74760M

Second byte

DA0 to DA7	Register name	Register content			Note										
		State	Function												
7	—	0	Second byte identification code												
6	INT/NON	0	Interlaced		Switches between interlaced and non-interlaced display.										
		1	Non-interlaced												
5	BLK1	0	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="text-align: center;">BLK0 \ BLK1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Blanking off</td> <td>Character size blanking</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Frame size blanking</td> <td>Total area blanking</td> </tr> </table>		BLK0 \ BLK1	0	1	0	Blanking off	Character size blanking	1	Frame size blanking	Total area blanking	Changes the blanking size.	
		BLK0 \ BLK1			0	1									
0	Blanking off	Character size blanking													
1	Frame size blanking	Total area blanking													
1															
4	BLK0	0													
		1													
3	BK1	0	Flashing period about 0.5 s		Sets the flashing period.										
		1	Flashing period about 1 s												
2	ATS	0	Highlight function		Selects at2.										
		1	Flashing function												
1	—	0													
0	DSPON	0	Character display off		Turns character output on and off.										
		1	Character display on												

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

6 COMMAND5: Display Control Setting Command 2

First byte

DA0 to DA7	Register name	Register content					Note																																																									
		State	Function																																																													
7	—	1	The command 5 identification code: sets display control parameters.																																																													
6	—	1																																																														
5	—	0																																																														
4	—	1																																																														
3	PH2	0	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <th rowspan="2">PHASE 2</th> <th rowspan="2">PHASE 1</th> <th rowspan="2">PHASE 0</th> <th colspan="2">Background color (phase)</th> </tr> <tr> <th>NTSC</th> <th>PAL</th> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>$\pi/2$</td> <td>$\pm\pi/2$</td> </tr> <tr> <td rowspan="2">0</td> <td rowspan="2">0</td> <td rowspan="2">1</td> <td>In phase</td> <td>In phase</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>$3\pi/2$</td> <td>$\mp\pi/2$</td> </tr> <tr> <td rowspan="2">1</td> <td rowspan="2">0</td> <td rowspan="2">1</td> <td>0</td> <td>1</td> <td>1</td> <td>π</td> <td>$\pm\pi$</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>$3\pi/4$</td> <td>$\pm 3\pi/4$</td> </tr> <tr> <td rowspan="2">1</td> <td rowspan="2">PH0</td> <td rowspan="2">0</td> <td>1</td> <td>0</td> <td>1</td> <td>$\pi/4$</td> <td>$\pm\pi/4$</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>$7\pi/4$</td> <td>$\mp\pi/4$</td> </tr> <tr> <td rowspan="2">1</td> <td rowspan="2">1</td> <td rowspan="2">1</td> <td>1</td> <td>1</td> <td>1</td> <td>$5\pi/4$</td> <td>$\mp 3\pi/4$</td> </tr> </table>				PHASE 2	PHASE 1	PHASE 0	Background color (phase)		NTSC	PAL	0	0	0	$\pi/2$	$\pm\pi/2$	0	0	1	In phase	In phase	0	1	0	$3\pi/2$	$\mp\pi/2$	1	0	1	0	1	1	π	$\pm\pi$	1	0	0	$3\pi/4$	$\pm 3\pi/4$	1	PH0	0	1	0	1	$\pi/4$	$\pm\pi/4$	1	1	0	$7\pi/4$	$\mp\pi/4$	1	1	1	1	1	1	$5\pi/4$	$\mp 3\pi/4$	Sets the phase of the background color for color burst.sz	
		PHASE 2								PHASE 1	PHASE 0	Background color (phase)																																																				
NTSC	PAL																																																															
0	0	0	$\pi/2$	$\pm\pi/2$																																																												
0	0	1	In phase	In phase																																																												
			0	1	0	$3\pi/2$	$\mp\pi/2$																																																									
1	0	1	0	1	1	π	$\pm\pi$																																																									
			1	0	0	$3\pi/4$	$\pm 3\pi/4$																																																									
1	PH0	0	1	0	1	$\pi/4$	$\pm\pi/4$																																																									
			1	1	0	$7\pi/4$	$\mp\pi/4$																																																									
1	1	1	1	1	1	$5\pi/4$	$\mp 3\pi/4$																																																									
			1																																																													
0	INT/EXT	0	External synchronization mode				Switches between internal and external synchronization.																																																									
		1	Internal synchronization mode																																																													

LC74760, 74760M

Second byte

DA0 to DA7	Register name	Register content				Note	
		State	Function				
7	—	0	Second byte identification code				
6	TST	0	Normal operation			Test mode should not be used. This bit should always be zero.	
		1	Test mode				
5	CHAL	0	Sets the character intensity level to about 95 IRE (bright white).			Switches the character intensity level.	
		1	Sets the character intensity level to about 75 IRE (white with a touch of grey).				
4	BKL	0	Sets the blanking intensity level to about 5 IRE (a deep black as a frame level).			Switches the blanking intensity level.	
		1	Sets the blanking intensity level to about 15 IRE (a dark grey as a frame level).				
3	RSL1	0	RSL1	RSL0	Intensity level	Amplitude	Switches the background intensity level.
		1	0	0	About 15 IRE	About 60 IRE	
2	RSL0	0	0	1	About 30 IRE	About 60 IRE	
		1	1	0	About 45 IRE	About 60 IRE	
1	—	0	1	1	About 60 IRE	About 69 IRE	
		0	—	—	—	—	
0	—	0					

Note: When the chip is reset by the $\overline{\text{RST}}$ pin, the register states (bits) are all cleared to 0.

7 COMMAND6: Display Control Setting Command 3

First byte

DA0 to DA7	Register name	Register content				Note
		State	Function			
7	—	1	The command 6 identification code: sets display control parameters.			
6	—	1				
5	—	1				
4	—	0				
3	MOD3	0	Sets Fsc to 3.58 MHz.			The logical or of this bit and the Fsc switching input pin (pin 14) is used.
		1	Sets Fsc to 4.43 MHz.			
2	MOD2	0	Sets the color mode to NTSC.			The logical or of this bit and the color mode switching input pin (pin 13) is used.
		1	Sets the color mode to PAL.			
1	MOD1	0	Sets the number of scan lines to 525 lines.			The logical or of this bit and the scan line count switching input pin (pin 12) is used.
		1	Sets the number of scan lines to 625 lines.			
0	MOD0	0	Sets the mode to a mode other than SECAM.			The logical or of this bit and the mode switching input pin (pin 11) is used.
		1	Sets the mode to SECAM mode.			

LC74760, 74760M

Second byte

DA0 to DA7	Register name	Register content			Note	
		State	Function			
7	—	0	Second byte identification code			
6	—	0				
5	—	0				
4	—	0				
3	IOS	0	Sets the mode setting pin to be an input pin.		Switches the input/output direction of the mode setting pins. (11 pin to 14 pin)	
		1	Sets the mode setting pin to be an output pin.			
2	BCOL1	0	BCOL1	BCOL0	Background color	Determines whether a background color is displayed. (Only valid in internal synchronization mode.)
		1	0	0	Background color displayed	
			0	1	No background color (about 15 IRE)	
1	BCOL0	0	1	0	No background color (about 25 IRE)	
		1	1	1	Illegal value	
0	CBOFF	0	Outputs a color burst signal.		Only valid when either BCOL0 is 1 or BCOL1 is 1.	
		1	Stops the output of color burst signals.			

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

8 COMMAND7: Display Control Setting Command 4

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 7 identification code: sets display control parameters.	
6	—	1		
5	—	1		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	LINS	0	Selects the lower 6 bits (bits 0 to 5)	Selects the upper or lower six bits when halftone output line mode is specified.
		1	Selects the upper 6 bits (bits 6 to B)	

Second byte

DA0 to DA7	Register name	Register content		Note	
		State	Function		
7	—	0	Second byte identification code		
6	—	0			
5	LIN5	0	Turns off (low) sixth line halftone output.		Used for the line 12 setting when LINS is high.
		1	Turns on (high) sixth line halftone output.		
4	LIN4	0	Turns off (low) fifth line halftone output.		Used for the line 11 setting when LINS is high.
		1	Turns on (high) fifth line halftone output.		
3	LIN3	0	Turns off (low) fourth line halftone output.		Used for the line 10 setting when LINS is high.
		1	Turns on (high) fourth line halftone output.		
2	LIN2	0	Turns off (low) third line halftone output.		Used for the line 9 setting when LINS is high.
		1	Turns on (high) third line halftone output.		
1	LIN1	0	Turns off (low) second line halftone output.		Used for the line 8 setting when LINS is high.
		1	Turns on (high) second line halftone output.		
0	LIN0	0	Turns off (low) first line halftone output.		Used for the line 7 setting when LINS is high.
		1	Turns on (high) first line halftone output.		

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

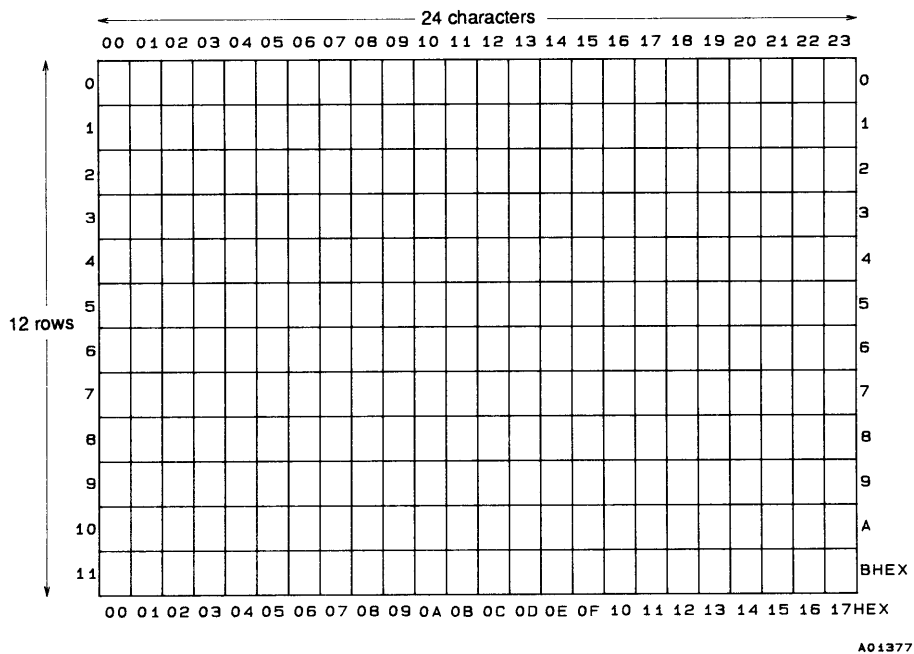
LC74760, 74760M

Display Configuration

The display consists of 12 rows of 24 characters each. Up to 288 characters can be displayed unless enlarged characters are displayed. Display memory addresses are expressed as a row address in the range 0 to B (hexadecimal) and a column address in the range 0 to 17 (hexadecimal).

Display Configuration and Display Memory Addresses

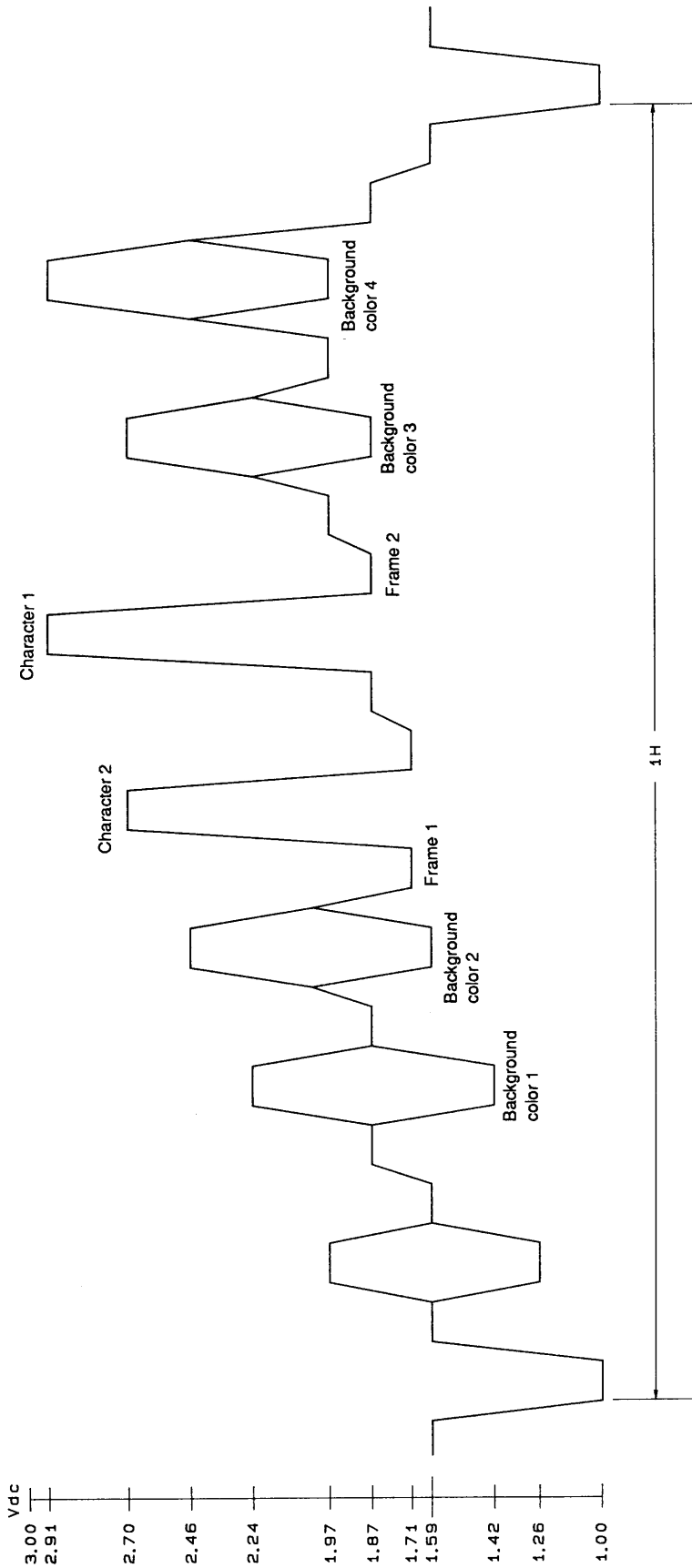
24 characters by 12 rows



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of January, 1996. Specifications and information herein are subject to change without notice.

Composite Video Signal Output Levels (internally generated levels)



A0137B

Output level	Output voltage (VDC)
Frame level 1	1.713
Pedestal level	1.597
Background low level 1	1.428
Burst low level	1.263
Sync level	1.000

Output level	Output voltage (VDC)
Character level 1	2.914
Character level 2	2.702
Background high level 2	2.460
Background high level 1	2.244
Burst high level	1.971
Frame level 2	1.873