Ordering number : EN5663

CMOS IC

LC83026E

Digital Signal Processor for Karaoke Systems

Overview

The LC83026E provides the audio signal processing required in karaoke systems, including pitch shift, microphone echo, voice muting, and simple surround simulation. It is a special-purpose DSP that implements karaoke processing with the addition of a single external 256-Kb DRAM. The LC83026E includes on-chip A/D and D/A converters and supports both digital and analog inputs and outputs. Its functions and characteristics can be modified to match the needs of the end product by sending coefficient data from the microcontroller over a serial interface.

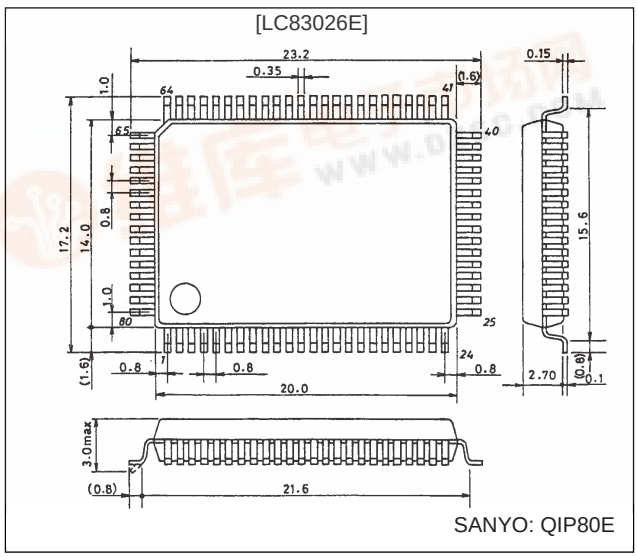
Features

- Application features
  - — Pitch shift
    The LC83026E supports pitch shifting of ±15 quarter tone steps, or ±1 octave in scale tone units as specified by command data. This pitch shifting can be applied either to the music track or to the microphone input. It is also possible to set up pitch shifting of ±1 octave in arbitrary steps by setting coefficient values.
  - — Microphone echo
    The LC83026E can apply echo processing to the input signal from the microphone A/D converter. The echo coefficients, including amount of echo and delay time, can be set.
  - — Voice muting
    The LC83026E provides attenuation of monaural components in the music signal. This allows CDs that include vocals to be used for karaoke. The voice muting function is turned on or off by command data transferred over the serial interface.
  - — Simple surround
    The LC83026E implements a simple surround simulation function by adding delay components to the music signal. The LC83026E includes six sets of simple surround coefficients as preset data, and these can be selected and switched using command data transferred over the serial interface. User-original surround effects can be implemented by setting coefficients, but the algorithm is fixed.
  - — Versatile input mixing
    The LC83026E supports hybrid mixing of digital music inputs and analog music inputs for both the left and right channels to support the processing of a wide range of disks.
- Audio inputs and outputs
  - — Inputs: Digital One system (stereo)
    A/D converters Three channels
  - — Outputs: Digital One system (stereo)
    D/A converters Two channels
  - — A/D converters
    Second-order delta-sigma modulation
    Three channels
  - — D/A converters
    2× oversampling digital filters + third-order noise shaper system Two channels
- Master clock: 768fs
- External memory: Up to two 256K (64K × 4 bits) external DRAMs can be used.
- Microcontroller input: Synchronous 8-bit serial data
- Power-supply voltage: 5V single-voltage supply
- Package: QFP80E

Package Dimensions

unit: mm

3174-QFP80E



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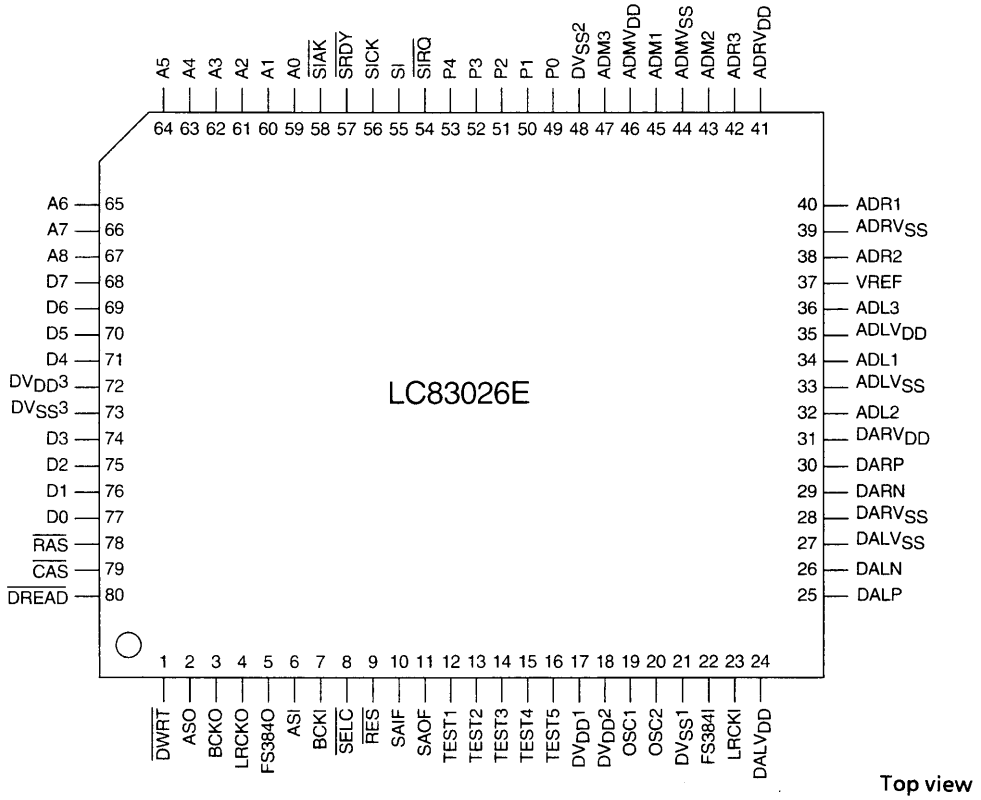
Pin Assignment



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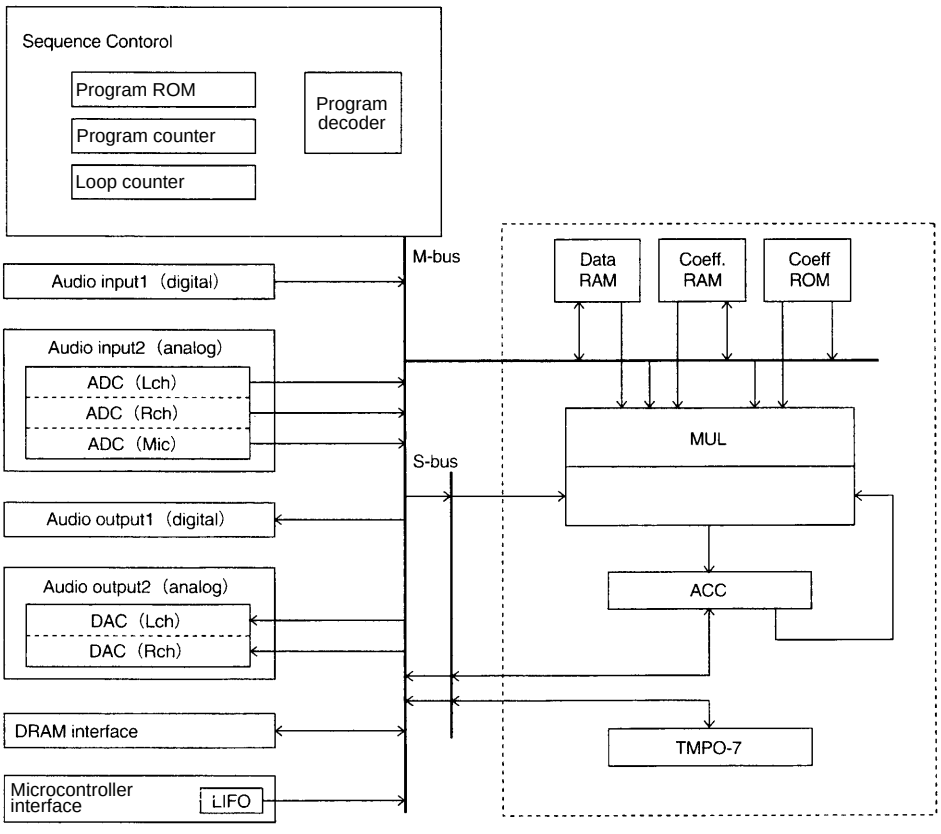
Block Diagram



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Pin Functions

Pin		Pin No.	I/O	Function
Control pins	OSC1	19	I	Crystal oscillator connection (768fs)
	OSC2	20	O	Crystal oscillator connection (768fs)
	FS384I	22	I	384fs input
	$\overline{\text{SELC}}$	8	I	Audio clock source switching (High: external, low: internal)
	SAIF	10	I	Digital audio input mode switching (Low: backward packing, high: forward packing)
	SAOF	11	I	Digital audio output mode switching (Low: 48fs, high 64fs)
	$\overline{\text{RES}}$	9	I	Reset
	TEST5 to 1	16 to 12	I	Test (Must be connected to ground during normal operation.)
	P0	49	I	Coefficient transfer mode control
	P2 to P1	51, 50	I	Initial operating mode control (A high level should be applied for normal operation.)
	P3	52	O	Microphone signal input level: Yes (low output)/No (high output) output
	P4	53	O	Music signal input level: Yes (low output)/No (high output) output
External memory interface	$\overline{\text{RAS}}$	78	O	$\overline{\text{RAS}}$ signal output
	$\overline{\text{CAS}}$	79	O	$\overline{\text{CAS}}$ signal output
	$\overline{\text{DREAD}}$	80	O	External memory read signal output
	$\overline{\text{DWRT}}$	1	O	External memory write signal output
	A8 to A0	67 to 59	O	Address output
	D7 to D0	68 to 71, 74 to 77	I/O	Data input and output (Normally only D0 to D3 are used)
Audio interface	LRCKI	23	I	ASI L/R clock input (1fs)
	LRCKO	4	O	ASO L/R clock output (1fs)
	BCKI	7	I	ASI bit clock input (32fs or higher)
	BCKO	3	O	ASO bit clock output (48fs or 64fs)
	FS384O	5	O	ASO 384fs output
	ASI	6	I	Digital audio data input (16-bits, MSB first)
	ASO	2	O	Digital audio data output (16-bits, MSB first, backward packed)
	ADL1	34	I	A/D converter input (left channel)
	ADL2	32	O	A/D converter output (left channel)
	ADL3	36	O	A/D converter output (left channel)
	ADR1	40	I	A/D converter input (right channel)
	ADR2	38	O	A/D converter output (right channel)
	ADR3	42	O	A/D converter output (right channel)
	ADM1	45	I	A/D converter input (microphone)
	ADM2	43	O	A/D converter output (microphone)
	ADM3	47	O	A/D converter output (microphone)
	DALP	25	O	D/A converter output (left channel)
	DALN	26	O	D/A converter output (left channel)
	DARP	30	O	D/A converter output (right channel)
	DARN	29	O	D/A converter output (right channel)
Microcontroller interface	$\overline{\text{SIRQ}}$	54	I	Input for the serial input request signal
	$\overline{\text{SIAK}}$	58	O	Output that indicates that a serial input is in progress
	SI	55	I	Serial data input from the control microcontroller (8-bit serial input)
	SICK	56	I	SI pin transfer clock input
	$\overline{\text{SRDY}}$	57	I	Ready signal input (from the control microcontroller) that indicates the completion of a serial data input.

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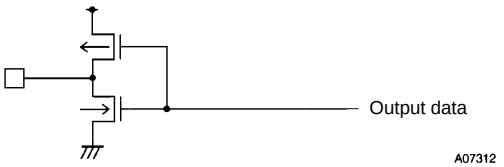
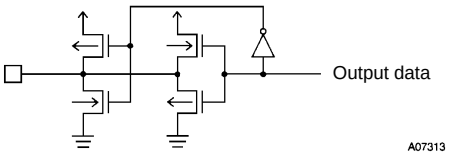
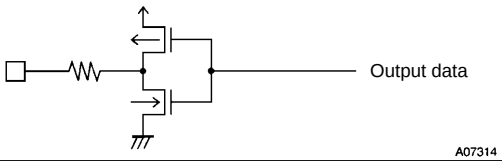
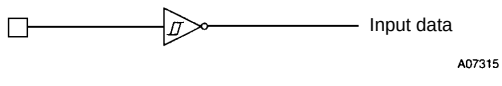
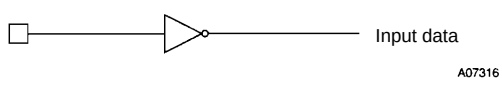
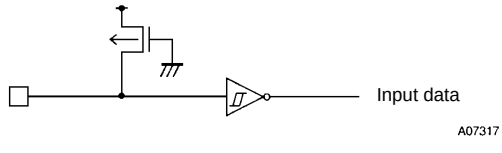
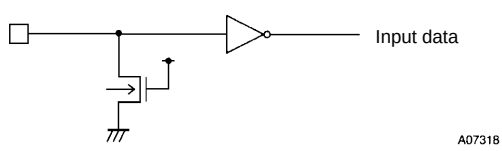
	Pin	Pin No.	I/O	Function
Power supply	$DV_{DD}1$ to 3	17, 18, 72	—	Digital block V_{DD} (Must be connected to +5 V.)
				<Make connections as short as possible so that no potential differences occur between any of the V_{DD} pins.>
	$DV_{SS}1$ to 3	21, 48, 73	—	Digital block V_{SS} (Must be connected to ground.)
				<Make connections as short as possible so that no potential differences occur between any of the V_{SS} pins.>
	$ADLV_{DD}$	35	—	A/D converter V_{DD} (left channel) (Connect to +5 V.)
	$ADRV_{DD}$	41	—	A/D converter V_{DD} (right channel) (Connect to +5 V.)
	$ADMV_{DD}$	46	—	A/D converter V_{DD} (microphone) (Connect to +5 V.)
	$DALV_{DD}$	24	—	D/A converter V_{DD} (left channel) (Connect to +5 V.)
	$DARV_{DD}$	31	—	D/A converter V_{DD} (right channel) (Connect to +5 V.)
	$ADLV_{SS}$	33	—	A/D converter V_{SS} (left channel) (Connect to ground.)
	$ADRV_{SS}$	39	—	A/D converter V_{SS} (right channel) (Connect to ground.)
	$ADMV_{SS}$	44	—	A/D converter V_{SS} (microphone) (Connect to ground.)
	$DALV_{SS}$	27	—	D/A converter V_{SS} (left channel) (Connect to ground.)
	$DARV_{SS}$	28	—	D/A converter V_{SS} (right channel) (Connect to ground.)

Design the wiring so that potential differences do not occur between the analog system V_{DD} pins and either other analog system V_{DD} pins or the digital system V_{DD} pins.

Design the wiring so that potential differences do not occur between the analog system V_{SS} pins and either other analog system V_{SS} pins or the digital system V_{SS} pins.

Pin Circuits

Pins	Specifications	Circuit
ASO, LRCKO, BCKO, $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$, FS384O, A0 to A8	TTL output	
P3, P4, $\overline{SIAK}$	CMOS intermediate current output	
ADL2, ADL3, ADM2, ADM3, ADR2, ADR3	Analog output	
DALP, DALN, DARP, DARN		
SI, SICK, $\overline{SIRQ}$, $\overline{SRDY}$, (OSC1)	Schmitt input	
FS384I, BCKI, ASI, LRCKI	Low Schmitt input	
TEST1 to TEST5	Normal input	
$\overline{RES}$	Input with built-in pull-up resistor	
$\overline{SELC}$, SAIF, SAOF	Input with built-in pull-down resistor	

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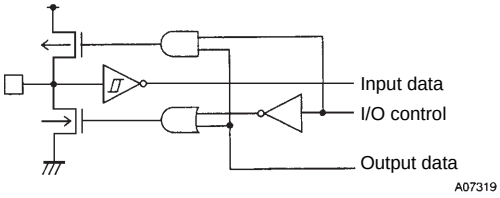
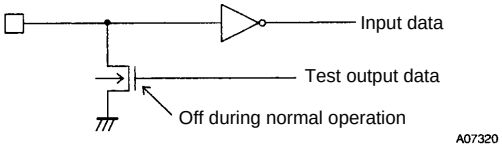
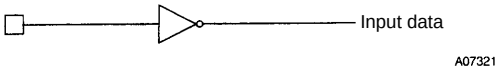
Pins	Specifications	Circuit
D0 to D7	CMOS intermediate current output Low Schmitt input	
P0 to P2	N-channel open drain intermediate current output Normal input	
ADL1, ADR1, ADM1	Analog input	

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit	Notes
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V	
Input voltage	V_{IN}		–0.3 to V_{DD} +0.3	V	
Output voltage	V_O1	OSC2 output	Values up to the oscillator voltage are allowable.	V	
	V_O2	Outputs other than OSC2	–0.3 to V_{DD} +0.3	V	
Peak output current	$I_{OP}1$	Audio interface, external RAM interface	–2 to +4	mA	1
	$I_{OP}2$	Microcontroller interface, P3, P4	–2 to +10	mA	2
Average output current	$I_{OA}1$	Audio interface, external RAM interface: Per pin	–2 to +4	mA	1
	$I_{OA}2$	Microcontroller interface, P3, P4: Per pin	–2 to +10	mA	2
	$\Sigma I_{OA}1$	FS384O, LRCKO, BCKO, ASO : Total	–10 to +10	mA	
	$\Sigma I_{OA}2$	$\overline{DWRT}$, $\overline{DREAD}$, $\overline{RAS}$, $\overline{CAS}$, A0 to A8, D0 to D7, $\overline{SIAK}$, P3, P4 : Total	–10 to +10	mA	
Allowable power dissipation	Pd max	Ta = –30 to +70°C	700	mW	
Operating temperature	Topr		–30 to +70	°C	
Storage temperature	Tstg		–40 to +125	°C	

Allowable Operating Ranges at Ta = –30 to +70°C, all V_{DD} = 4.75 to 5.25 V, all V_{SS} = 0 V unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit	Notes
			min	typ	max		
Operating supply voltage	V_{DD}		4.75		5.25	V	
Input high-level voltage	$V_{IH}1$	Audio interface and external RAM interface	2.4			V	4
	$V_{IH}2$	P0 to P2, $\overline{SELC}$, SAIF, SAOF, TEST1 to TEST5	0.7 V_{DD}			V	5
	$V_{IH}3$	$\overline{RES}$, OSC1, and the microcontroller interface	0.75 V_{DD}			V	6
Input low-level voltage	$V_{IL}1$	Audio interface and external RAM interface			0.8	V	4
	$V_{IL}2$	P0 to P2, $\overline{SELC}$, SAIF, SAOF, TEST1 to TEST5			0.3 V_{DD}	V	5
	$V_{IL}3$	$\overline{RES}$, OSC1, and the microcontroller interface			0.25 V_{DD}	V	6
Instruction cycle time	t_{CYC}		58		59.11	ns	

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Parameter	Symbol	Conditions	Ratings			Unit	Notes
			min	typ	max		
[External Clock Input Conditions]							
Frequency	f_{EXT}	Related to the FS384I pin. See Figure 1.	16.85		17.01	MHz	
Pulse width	f_{EXTH}	maximum: 44.1 kHz × 384 × 1.005	23			ns	
	f_{EXTL}	minimum: 44.1 kHz × 384 × 0.995	23			ns	
Rise time	t_{EXTR}				9	ns	
Fall time	t_{EXF}				9	ns	
[Self-Excited Oscillation Conditions(crystal oscillator)]							
Oscillator frequency	f_{OSC}	OSC1 and OSC2. See Figure 2. 44.1 kHz/48 kHz × 768 ±0.1%	33.84		40.55	MHz	
Oscillator stabilization period	t_{OSCS}	See Figure 3.			100	ms	
[Audio Data Input Conditions]							
Transfer bit clock period	t_{BCYC}	Related to BCKI. See Figure 4.	354			ns	
Transfer bit clock pulse width	t_{BCW}		100			ns	
Data setup time	t_S		70			ns	
Data hold time	t_H		70			ns	
[Serial I/O Clock Conditions]							
Serial clock period	t_{SCYC}	Related to the microcontroller interface. See Figure 5. (Related to SICK, SI, and $\overline{SRDY}$.)	480			ns	
Serial clock pulse width	t_{SCW}		200			ns	
Data setup time	t_{SS}		70			ns	
Data hold time	t_{SH}		70			ns	
$\overline{SRDY}$ hold time	t_{SYH}		200			ns	
$\overline{SRDY}$ pulse width	t_{SYW}		200			ns	
[DRAM Input Conditions]							
Input data setup time	t_{DSI}	Related to external DRAM data input. See Figure 6. (Related to $\overline{CAS}$ and D0 to D7.)	20			ns	
Input data hold time	t_{DHI}		0			ns	

Electrical Characteristics 1 at Ta = –30 to +70°C, all V_{DD} = 4.75 to 5.25 V, all V_{SS} = 0 V unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit	Notes
			min	typ	max		
Input high-level current	$I_{IH}1$	$\overline{SELC}$, SAIF, SAOF, $V_{IN} = V_{DD}$ (Input pins with pull-down resistors)		100	250	µA	8
	$I_{IH}2$	P0 to P2, $V_{IN} = V_{DD}$ (Nch transistor OFF)			10	µA	
	$I_{IH}3$	Other input-only pins			10	µA	
Input low-level current	$I_{IL}1$	$\overline{RES}$, $V_{IN} = V_{SS}$ (Input pins with pull-up resistors)	–250	–100		µA	8
	$I_{IL}2$	P0 to P2, $V_{IN} = V_{SS}$	–10			µA	
	$I_{IL}3$	Other input-only pins	–10			µA	
Output high-level voltage	$V_{OH}1$	I_{OH} = –0.4 mA	4.0	4.98		V	1, 8
	$V_{OH}2$	I_{OH} = –50 µA	V_{DD} –1.2	4.997		V	2,3,8
Output low-level voltage	$V_{OL}1$	I_{OL} = 2 mA		0.065	0.4	V	1, 8
	$V_{OL}2$	I_{OL} = 10 mA		0.32	1.5	V	2,3,8
Output off leakage current	I_{OFF}	$V_O = V_{SS}$, V_{DD}	–40		+40	µA	
Input and output capacitance	C_{IO}				10	pF	
[Audio Data Output Timing]							
Output data hold time	t_{OH}	BCK0 and ASO. See Figure 7.	–30			ns	7
Output data delay time	t_{OD}				50	ns	7

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Parameter	Symbol	Conditions	Ratings			Unit	Notes
			min	typ	max		
[External DRAM Access Timing]							
$\overline{RAS}$ high-level pulse width	t_{RP}	Output timing to the external DRAM. See Figure 8.	80			ns	7
$\overline{RAS}$ low-level pulse width	t_{RAS}		700			ns	7
$\overline{CAS}$ high-level pulse width	t_{CP}		50			ns	7
$\overline{CAS}$ low-level pulse width	t_{CAS}		95			ns	7
$\overline{CAS}$ cycle time	t_{PC}		175			ns	7
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}		60			ns	7
$\overline{CAS}$ hold time	t_{CSH}		170			ns	7
$\overline{RAS}$ hold time	t_{RSH}		95			ns	7
$\overline{RAS}$ address setup time	t_{ASR}		60			ns	7
$\overline{RAS}$ address hold time	t_{RAH}		20			ns	7
$\overline{CAS}$ address setup time	t_{ASC}		30			ns	7
$\overline{CAS}$ address hold time	t_{CAH}		90			ns	7
$\overline{DWRT}$ pulse width	t_{WP}		95			ns	7
Write command setup time	t_{WCS}		12			ns	7
Write command hold time	t_{WCH}		65			ns	7
Output data setup time	t_{DSO}	Output timing to the external DRAM. See Figure 8.	30			ns	7
Output data hold time	t_{DHO}		100			ns	7
Crystal oscillator	C1	OSC1 and OSC2. See Figure 2.		13		pF	8
	C2			29		pF	8
	L			1.5		µH	8
Current drain	I_{DD}	For $V_{DD}1$, $V_{DD}2$, and $V_{DD}3$ when operating at 33.8688 MHz.		60	95	mA	9

Electrical Characteristics 2 at Ta = 25°C, all V_{DD} = 5.0 V, all V_{SS} = 0 V unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit	Notes
			min	typ	max		
[A/D Converter Block]							
Total harmonic distortion	A-THD	1 kHz, at 0 dB		0.05		%	10
Signal-to-noise ratio	A-S/N	1 kHz, at 0 dB	75	80		dB	10,11
Crosstalk	A-C · T	1 kHz, at 0 dB		–75		dB	10,11
[D/A Converter Block]							
Total harmonic distortion	D-THD	1 kHz, at 0 dB		0.01		%	10
Signal-to-noise ratio	D-S/N	1 kHz, at 0 dB		85		dB	10,11
Crosstalk	D-C · T	1 kHz, at 0 dB		–80		dB	10,11

Notes: 1. TTL output level pins: ASO, FS384O, BCKO, LRCKO, D0 to D7, A0 to A8, $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$

2. CMOS intermediate current output pins: P3, P4, SIAK

3. N-channel open drain intermediate current output pins: P0 to P2

4. Low Schmitt input pins: BCKI, ASI, LRCKI, D0 to D7, FS384I

5. Normal input pins: P0 to P2, TEST1 to TEST5, $\overline{SELC}$, SAIF, SAOF

6. Schmitt input pins: $\overline{RES}$, SI, SICK, $\overline{SIRQ}$, $\overline{SRDY}$, OSC1

7. When the load capacitance is 50 pF.

8. The values for the oscillator capacitors C1 and C2 include the line capacitances.

9. The typical values for the current drain are for V_{DD} = 5 V, room temperature, and typical samples.

10. Fs = 44.1 kHz and 20 kHz low-pass filter used. Measurement is with the external circuit structure and constants in the Sanyo evaluation board.

11. With the weight A filter used.

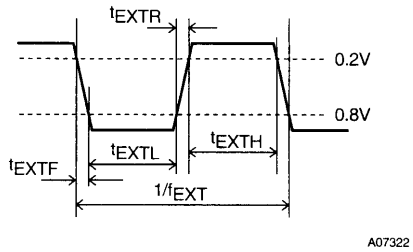


Figure 1 External Clock Input Waveform (FS384I)

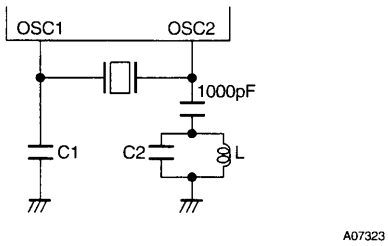


Figure 2 Crystal Oscillator Circuit

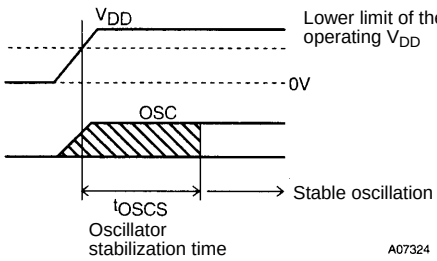


Figure 3 Oscillator Stabilization Time

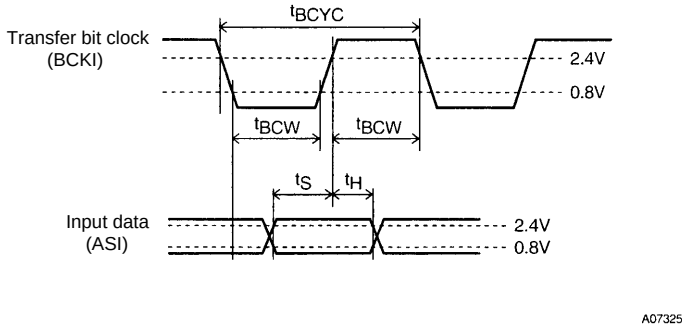


Figure 4 Audio Data Input Conditions

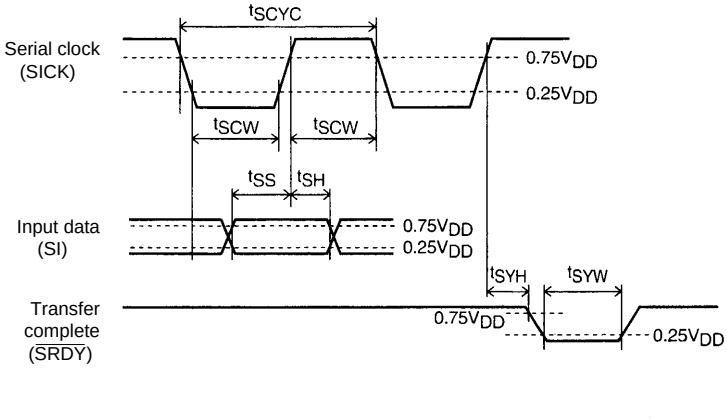


Figure 5 Microcontroller Interface

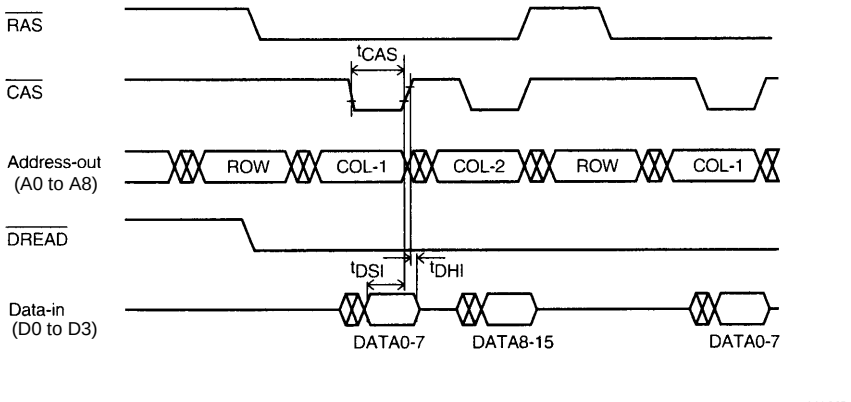


Figure 6 External DRAM Data Input Timing

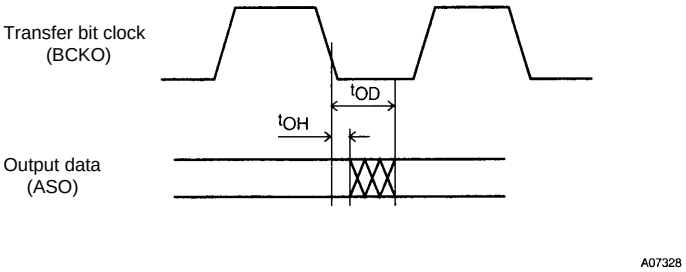


Figure 7 Audio Data Output Timing

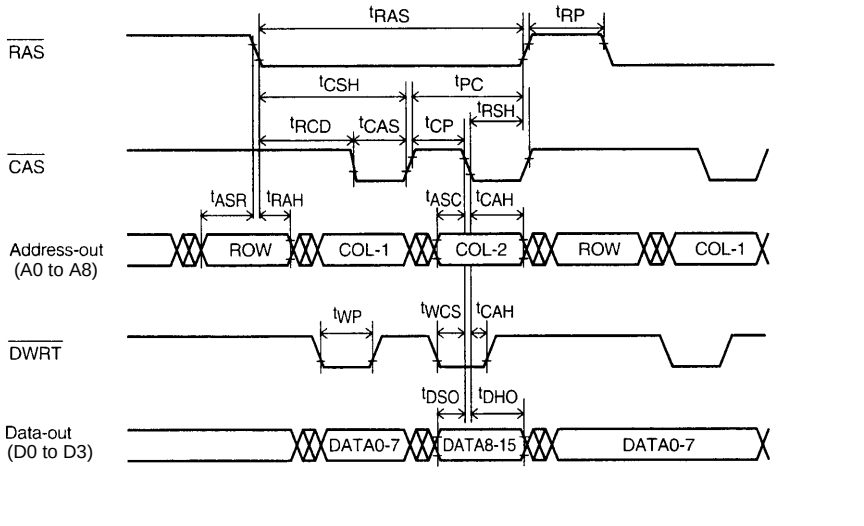
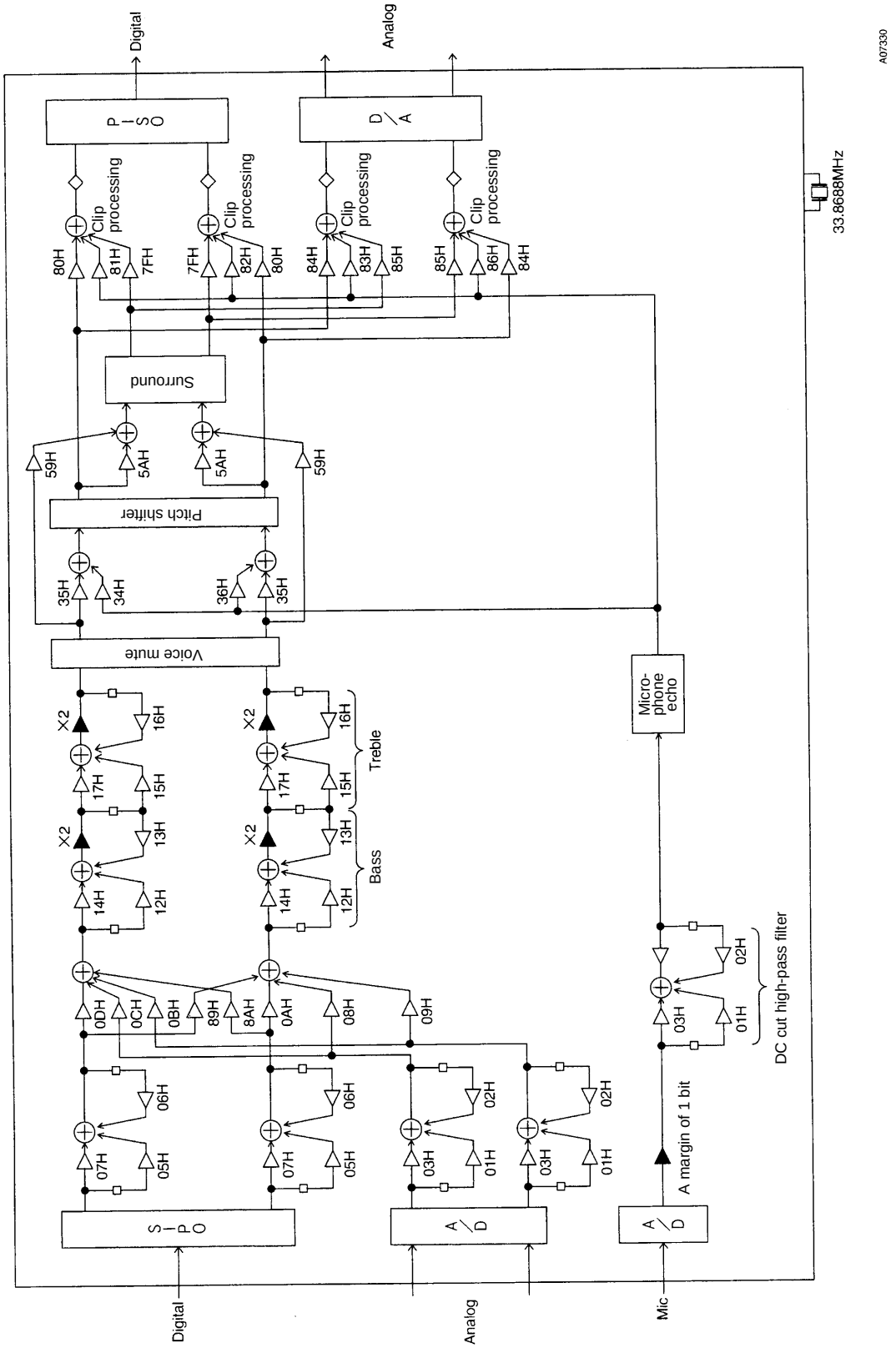


Figure 8 External DRAM Data Output Timing

Differences between the LC83025E and the LC83026E

Parameter	LC83025E	LC83026E
A/D converter block	Decimation filter improved	
	Input comparator improved	
	*: The V_{REF} pin was added in association with the improvements to the input comparator. The V_{REF} pin external capacitor must be located as close as possible to the LC83026E, and must be connected with lines that are as short as possible.	
D/A converter block	4 × oversampling filters used	2 × oversampling filters used
	Second-order noise shaping	Third-order noise shaping
	Single-pin output used.	Two-pin output operation
Reset time	One or more sampling period	Two or more sampling periods
When no digital input is provided (when the $\overline{SELC}$ pin is low)	The LRCKI and BCKI pins must be connected to the LRCKO and BCKO pins.	The LRCKI and BCKI pins must be connected to either V_{DD} or V_{SS}; they do not need to be connected to the LRCKO and BCKO pins.

Overall Signal Flow



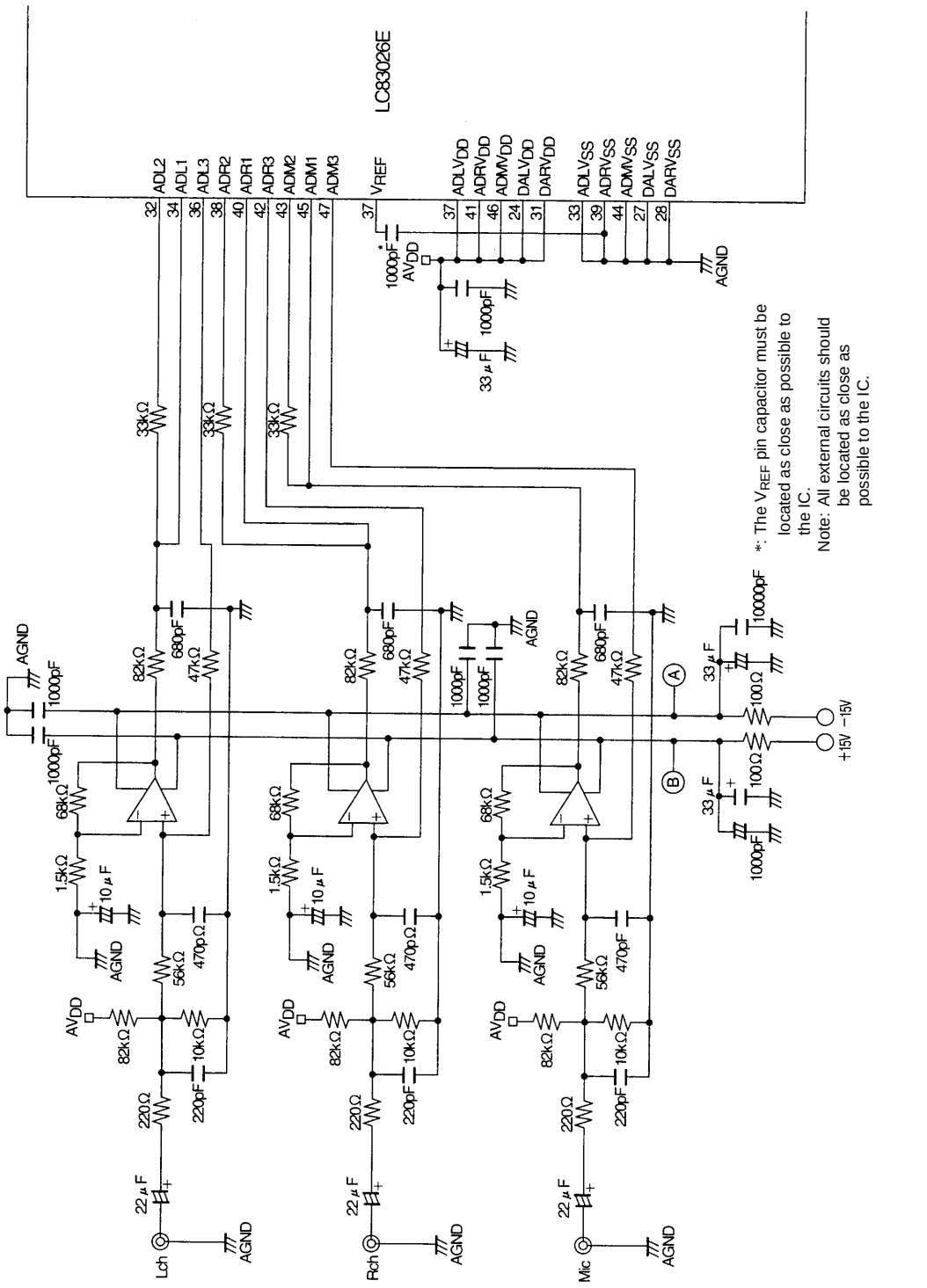


Figure 9 A/D Converter External Circuit Example

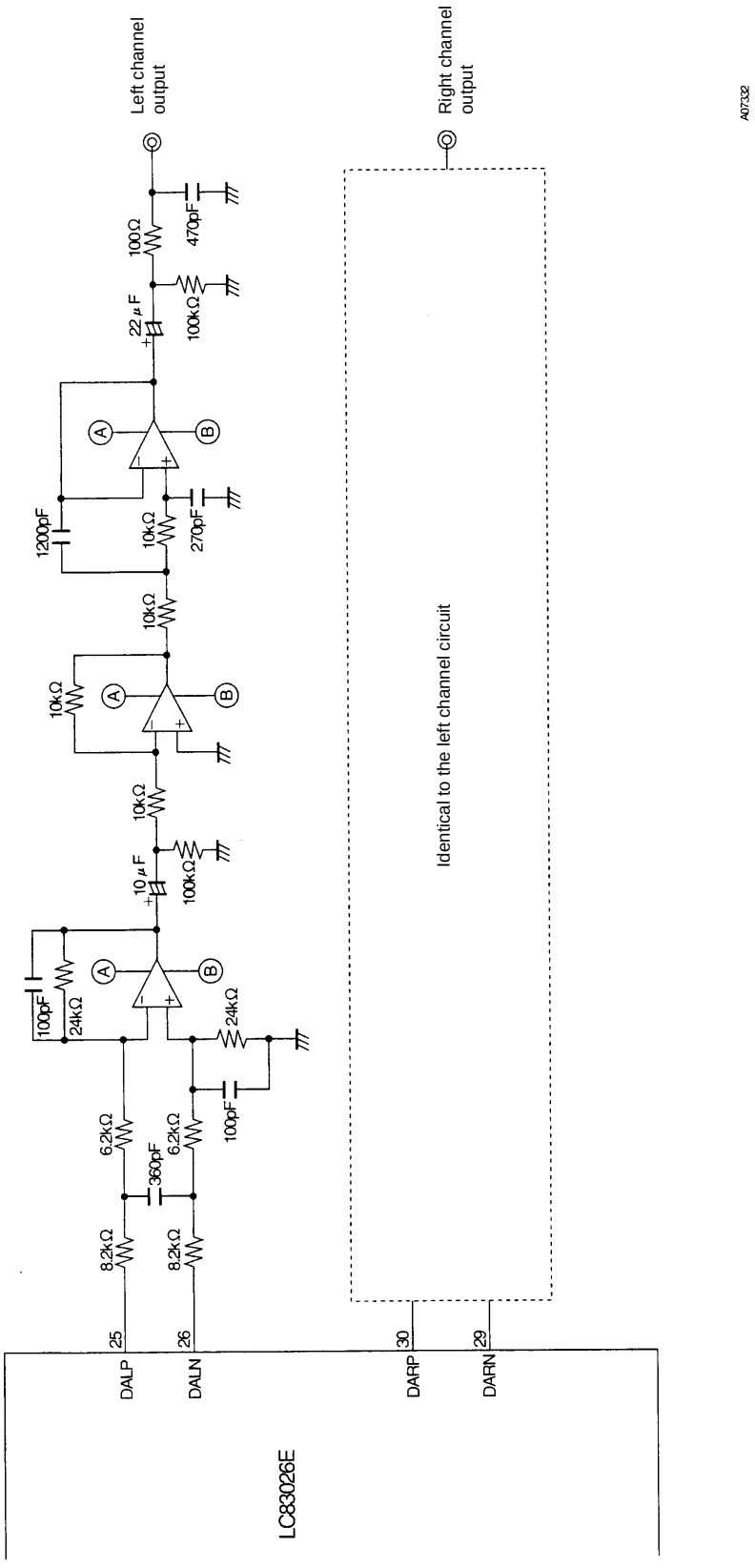
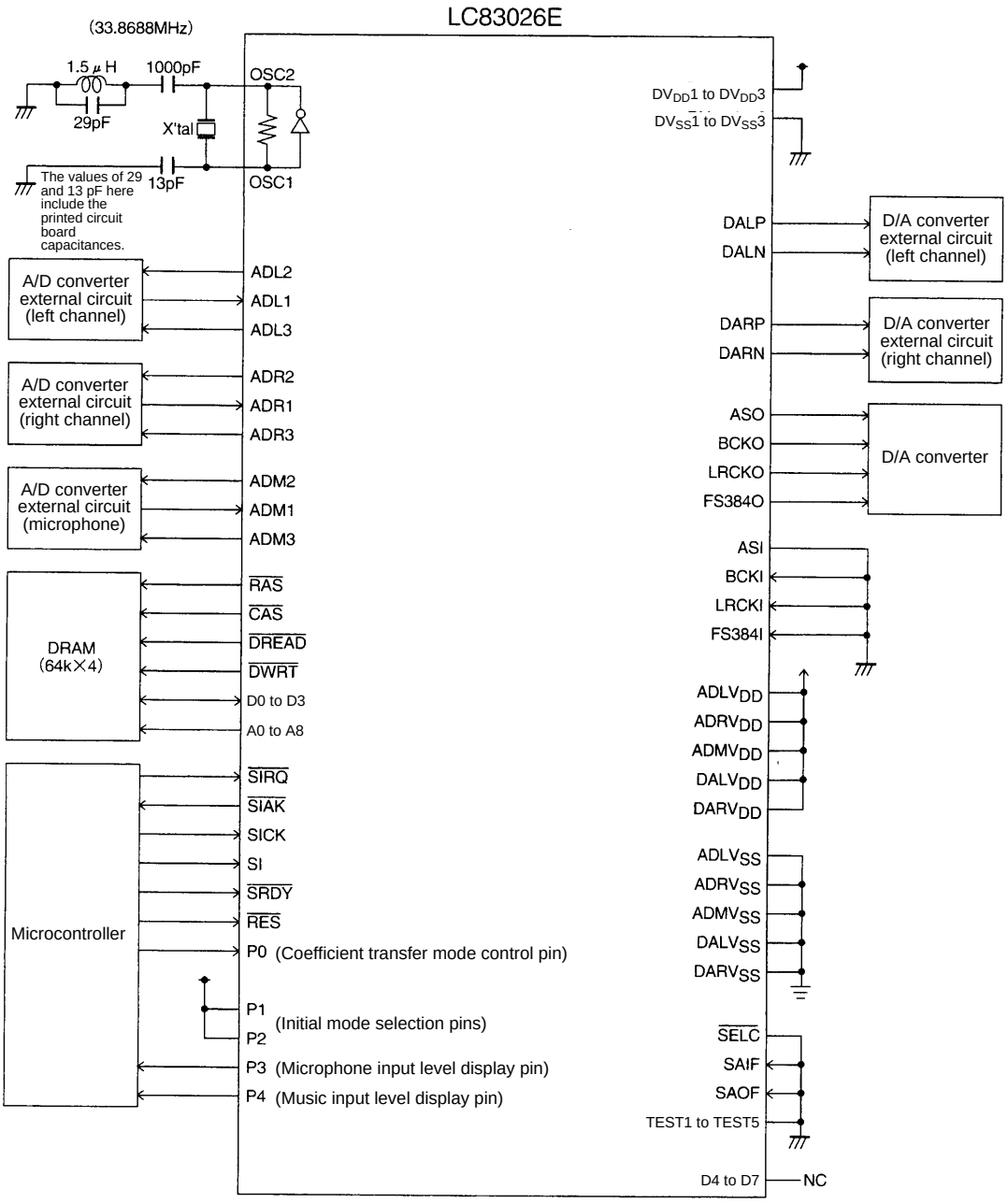


Figure 10 D/A Converter External Circuit Example

Application Circuit Example Outline (When digital input is not used)



Whether or not the digital inputs and/or analog outputs are used depends on the specifications of the application.
If any of these pins are not used, any unused input pins should be tied to high or low and any unused output pins should be left open.

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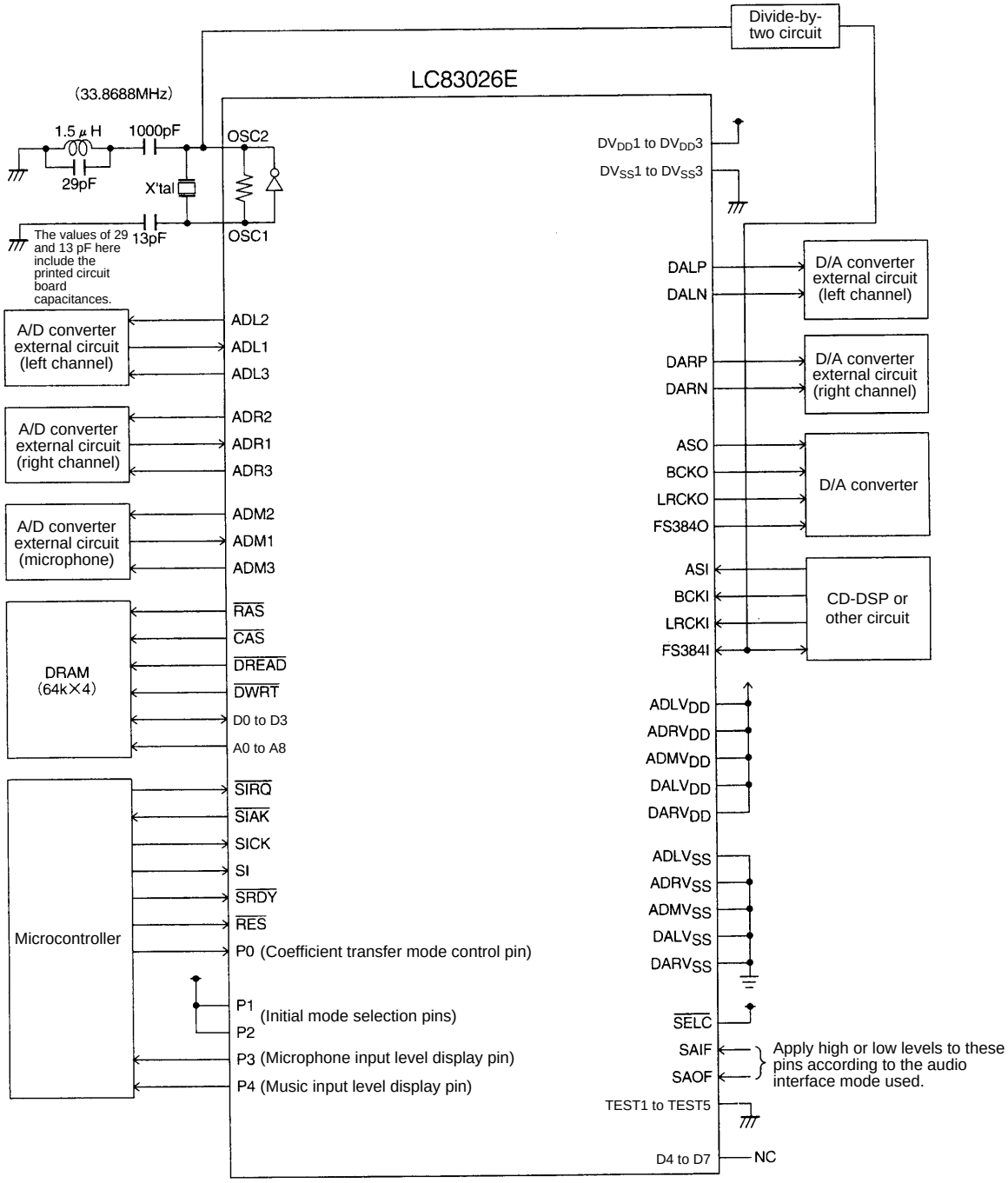
Application Circuit Example Outline (When digital input is used 1)



Whether or not the digital inputs and/or analog outputs are used depends on the specifications of the application.
If any of these pins are not used, any unused input pins should be tied to high or low and any unused output pins should be left open.

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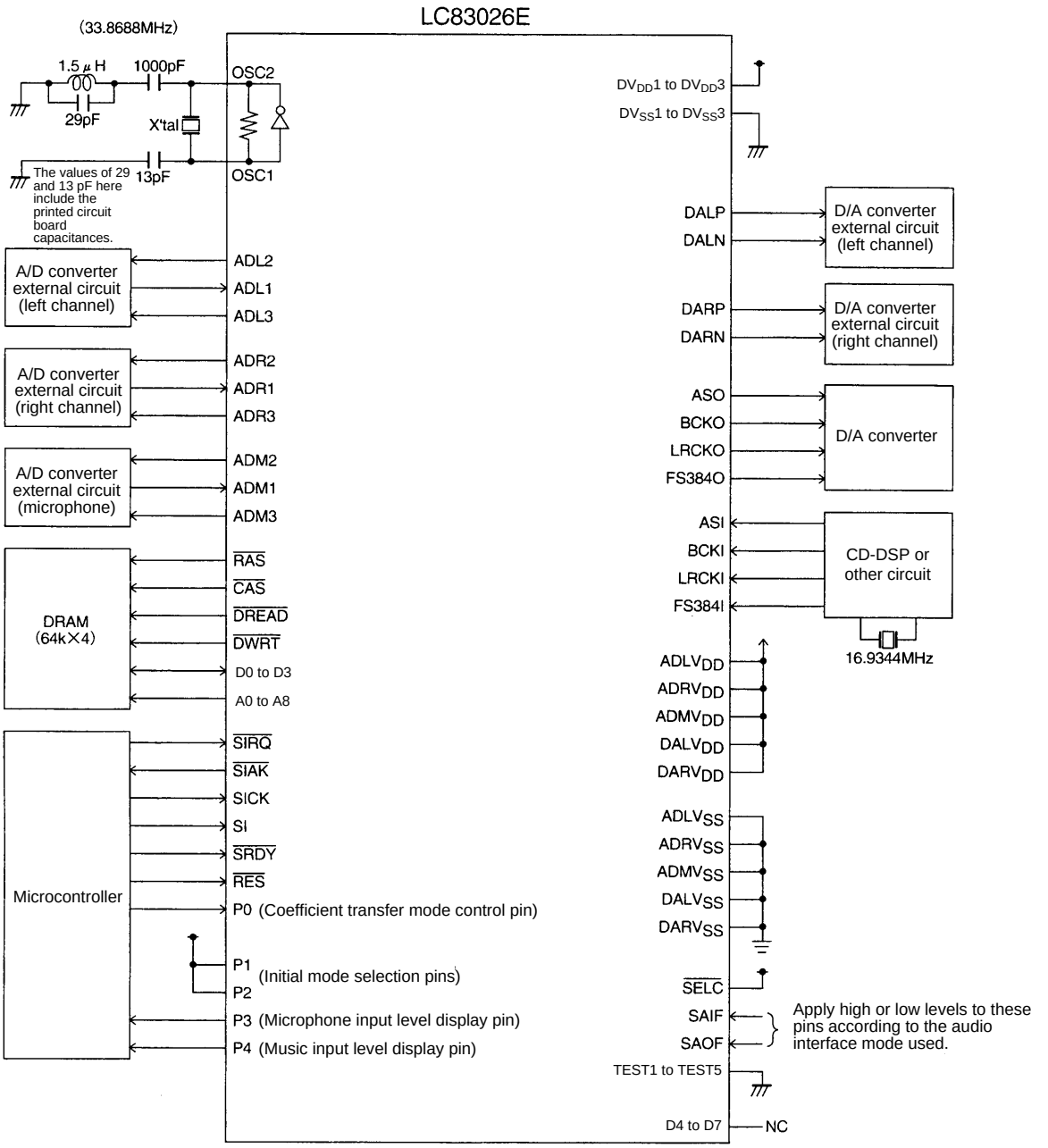
Application Circuit Example Outline (When digital input is used 2)



Whether or not the digital inputs and/or analog outputs are used depends on the specifications of the application.
If any of these pins are not used, any unused input pins should be tied to high or low and any unused output pins should be left open.

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