CMOS LSI

SANYO No.4454A

LC8390M

16bits A/D and D/A Converters for Digital Audio Systems

Overview

The LC8390M combines two-channel D/A and A/D converters in a single chip.

Features

- A/D Converter Block
  - — Quadratic ΔΣ modulation
  - — 16bit resolution
  - — Built-in aliasing noise prevention digital filter
  - — A/D converters for two channels built in (synchronized input when standard audio output is used)
  - — S/N = 80 dB, THD + N = 0.025% (typical, A-compensation filter used)
  - — Digital output: MSB first, forward packed, bit clock rates of 32, 48, and 64 Fs
  - — External integrator used.
- D/A Converter Block
  - — 16× oversampling quadratic noise shaper + PWM
  - — 16bits resolution
  - — D/A converters for two channels built in (synchronized output)
  - — S/N = 85 dB, THD + N = 0.03% (typical, A-compensation filter used)
  - — Digital input: MSB first, backward packed, bit clock rates of 32, 48, and 64 Fs
  - — Digital oversampling filters are not built in.
- Built-in double-buffering serial I/O circuits. (These circuits support both standard audio I/O and I/O with arbitrary timing.)
- Sampling frequencies of 48, 44.1, and 32 kHz
- Master clock: 512 Fs (24.576 MHz when fs = 48 kHz) or 384 Fs

  Notes: Only the A/D converters operate when 384 Fs is selected as the master clock. The D/A converters do not operate in this mode.

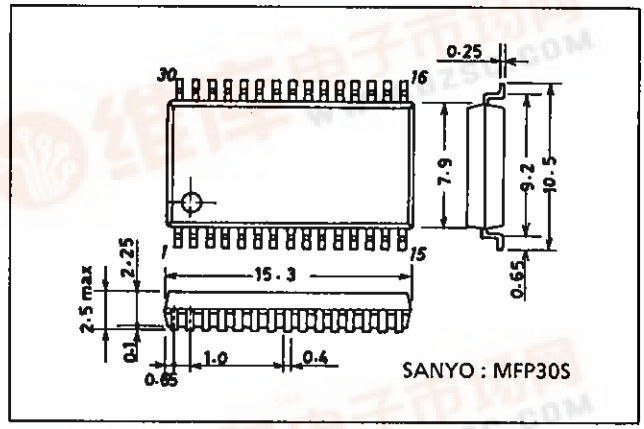
  Since the analog I/F and analog power supply pins are more susceptible to damage from static electricity than the other pins, extra care is required.

  Analog I/F pins: DZOUTL, ADL2, $ADLV_{SS}$, $ADLV_{DD}$, ADL3, DZOUTR, ADR2, $ADRV_{SS}$, $ADRV_{DD}$, ADR3, $DALV_{SS}$, PWML, $DALV_{DD}$, $DARV_{SS}$, PWMR, $DARV_{DD}$
- Package: 30-pin MFP
- Power supply: 5 V, single voltage, CMOS

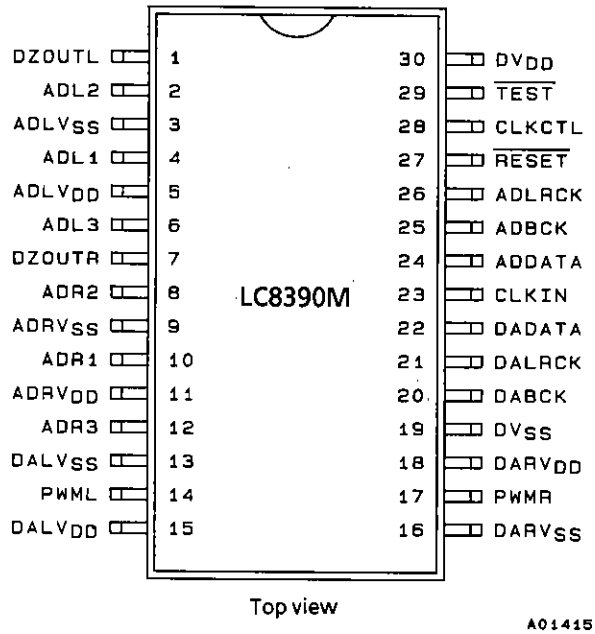
Package Dimensions

unit: mm

3073A-MFP30S



Pin Assignment



Top view

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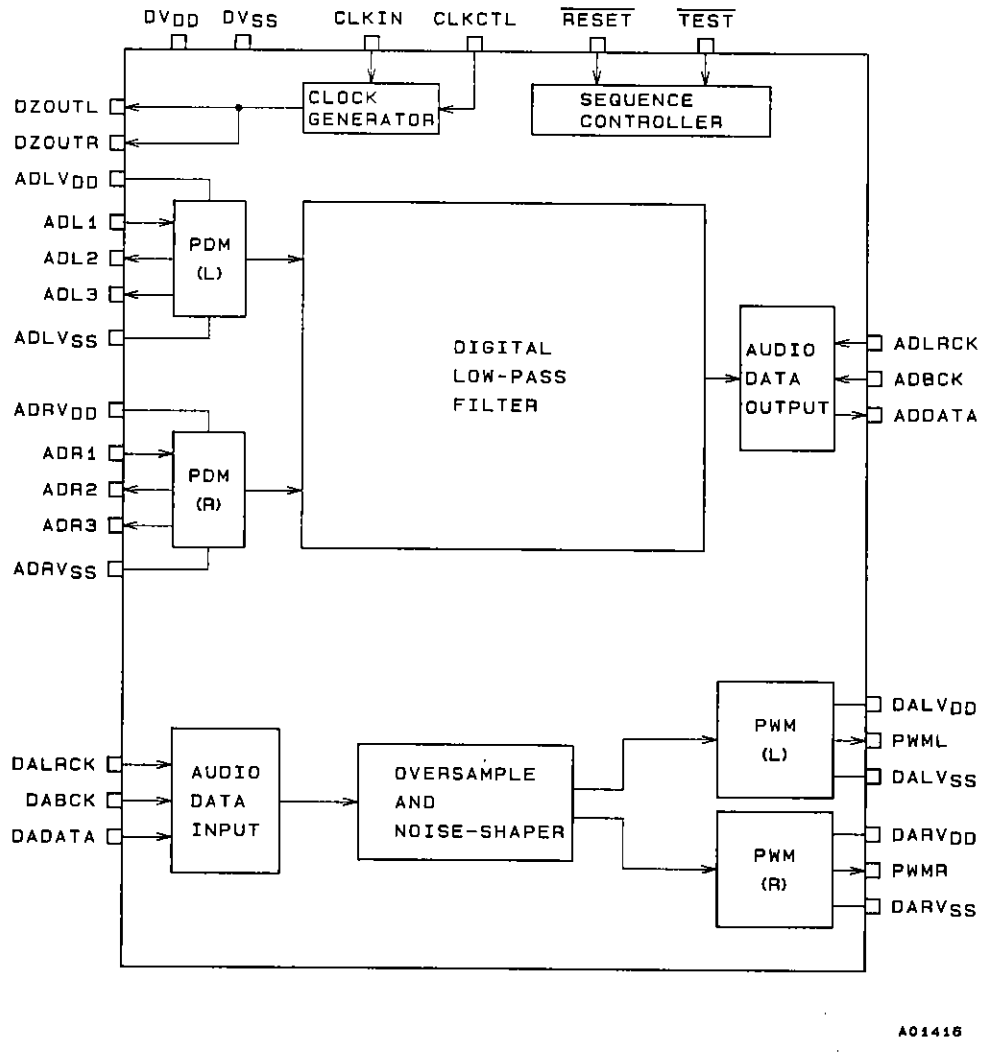
Block Diagram



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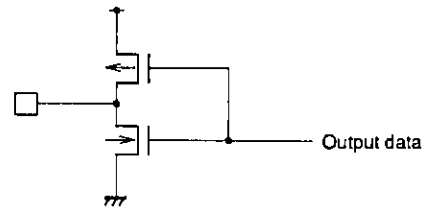
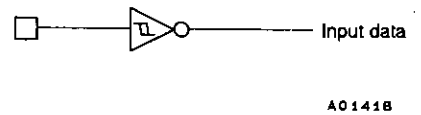
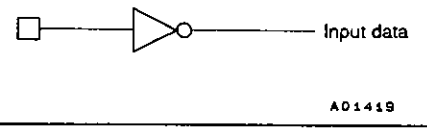
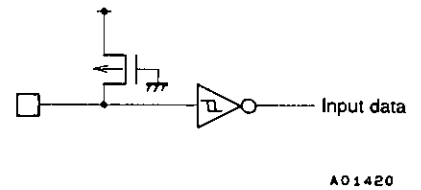
Pin Functions

Block	Pin No.	Pin	I/O	Function
A/D block	5	$ADLV_{DD}$	—	Analog left channel A/D power supply
	3	$ADLV_{SS}$	—	Analog left channel A/D ground
	4	ADL1	I	Left channel A/D audio input
	2	ADL2	O	Left channel A/D linear ΔΣ output
	6	ADL3	O	Left channel A/D quadratic ΔΣ output
	11	$ADRV_{DD}$	—	Analog right channel A/D power supply
	9	$ADRV_{SS}$	—	Analog right channel A/D ground
	10	ADR1	I	Right channel A/D audio input
	8	ADR2	O	Right channel A/D linear ΔΣ output
	12	ADR3	O	Right channel A/D quadratic ΔΣ output
	26	ADLRCK	I	A/D left and right channel clock input
	25	ADBCK	I	A/D bit clock input
	24	ADDATA	O	A/D data output
	1	DZOUTL	O	A/D dithering clock output
	7	DZOUTR	O	A/D dithering clock output
D/A block	15	$DALV_{DD}$	—	Analog left channel D/A power supply
	13	$DALV_{SS}$	—	Analog left channel D/A ground
	14	PWML	O	Left channel D/A PWM output
	18	$DARV_{DD}$	—	Analog right channel D/A power supply
	16	$DARV_{SS}$	—	Analog right channel D/A ground
	17	PWMR	O	Right channel D/A PWM output
	21	DALRCK	I	D/A left and right channel clock input
	20	DABCK	I	D/A bit clock input
	22	DADATA	I	D/A data input
Control and other pins	30	DV_{DD}	—	Digital system power supply
	19	DV_{SS}	—	Digital system ground
	23	CLKIN	I	Master clock input
	28	CLKCTL	I	Master clock selection (high: 512 Fs, low: 384 Fs)
	27	$\overline{RESET}$	I	Reset input
	29	$\overline{TEST}$	I	Test input. (This pin must be connected to DV_{DD} during normal operation.)

Pin Types

Specification	Circuit	Pin
TTL output		ADDATA
Analog output		PWML, PWMR
		ADL2, ADL3, DZOUTL, ADR2, ADR3, DZOUTR
Schmitt input		$\overline{\text{TEST}}$, CLKCTL, ADLRCK, ADBCK, CLKIN, DADATA, DALRCK, DABCK
Analog input		ADL1, ADR1
Built-in pull-up resistor input		$\overline{\text{RESET}}$

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +7.0	V
Maximum output voltage	V_O max		−0.3 to V_{DD} + 0.3	V
Maximum input voltage	V_{IN} max		−0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = −30 to +70°C	200	mW
Operating temperature	Topr		−30 to +70	°C
Storage temperature	Tstg		−40 to +125	°C

Allowable Operating Ranges
at Ta = –30 to 70°C, all V_{DD} = 4.75 to 5.5 V, all V_{SS} = 0 V unless otherwise specified

Parameter		Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Operating supply voltage		V_{DD}	All V_{DD} pins*2	4.75		5.5	V
Input high level voltage		V_{IH}	Schmitt inputs, built-in pull-up resistor inputs*1	0.75 V_{DD}			V
Input low level voltage		V_{IL}	Schmitt inputs, built-in pull-up resistor inputs*1			0.25 V_{DD}	V
External clock input conditions	Frequency	f_{EXT}	CLKIN: See figure 1.	12.16		24.83	MHz
	Pulse width	t_{EXTH} t_{EXTL}		16			ns
	Rise and fall times	t_{EXTR} t_{EXTF}				9	ns
$\overline{RESET}$ low level input pulse width		t_{RES}	$\overline{RESET}$: See figure 2.	15 cycles of the CLKIN input clock			
Transfer clock input conditions	Transfer bit clock period	t_{BCYC}	ADBCK, DABCK, ADLRCK, and DALRCK: See figures 3 and 4.	325			ns
	Transfer bit clock pulse width	t_{BCW}		100			ns
	Transfer bit clock setup time	t_{BCS}				70	ns
	Transfer bit clock hold time	t_{BCH}				70	ns
D/A converter data input conditions	Data setup time	t_{DS}	DABCK and DADATA: See figure 3.	70			ns
	Data hold time	t_{DH}		70			ns

Note 1: $\overline{TEST}$, CLKCTL, ADLRCK, ADBCK, CLKIN, DADATA, DALRCK, DABCK, $\overline{RESET}$
2: Apply the same voltage to the DV_{DD}, $ADLV_{DD}$, $ADRV_{DD}$, $DALV_{DD}$ and $DARV_{DD}$ pins.

Electrical Characteristics 1 at Ta = 25°C, all V_{DD} = 5.0 V, all V_{SS} = 0 V unless otherwise specified

Parameter		Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
A/D block	Total harmonic distortion	A-THD	At 1 kHz and 0 dB*		0.025		%
	Signal-to-noise ratio	A-S/N	At 1 kHz and 0 dB*		80		dB
	Crosstalk	A-C•T	At 1 kHz and 0 dB*		–78		dB
D/A block	Total harmonic distortion	D-THD	At 1 kHz and –1 dB*		0.03		%
	Signal-to-noise ratio	D-S/N	At 1 kHz and –1 dB*		85		dB
	Crosstalk	D-C•T	At 1 kHz and –1 dB*		–83		dB

Note: * A-compensation filter used, Fs = 48 kHz, and testing is performed using the Sanyo supplied evaluation board.

Electrical Characteristics 2
at Ta = –30 to 70°C, all V_{DD} = 4.75 to 5.5 V, all V_{SS} = 0 V unless otherwise specified

Parameter		Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Input low level current		I_{IL}	$\overline{RESET}$ (built-in pull-up resistor inputs): V_{IN} = V_{SS}	–250			μA
Output high level voltage		V_{OH}	ADDATA: I_{OH} = –0.4 mA	4.0			V
Output low level voltage		V_{OL}	ADDATA: I_{OL} = 2 mA			0.4	V
Input leakage current		I_{LK}	Schmitt inputs: V_{IN} = V_{SS}, V_{DD}	–10		+10	μA
Input and output capacitance		C_{IO}				10	pF
Data output timing	Data hold time	t_{OH}	ADDATA: See figure 5.	0			ns
	Data delay time	t_{OD}				50	ns
Current dissipation		I_{DD}	DV_{DD}		7	14	mA
			The sum of $ADLV_{DD}$, $ADRV_{DD}$, $DALV_{DD}$ and $DARV_{DD}$.		8	16	mA

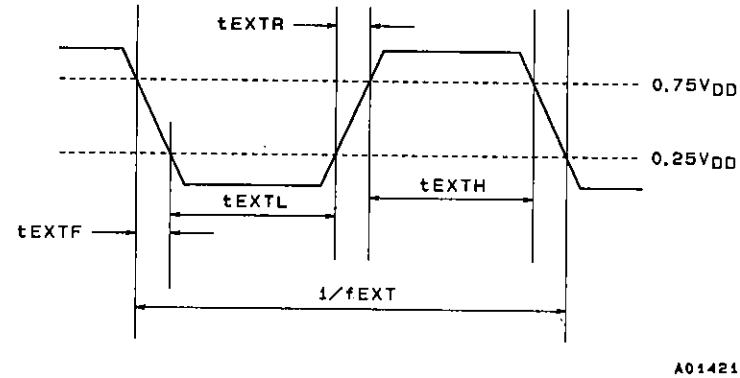


Figure 1 External Clock Input Waveform (CLKIN)

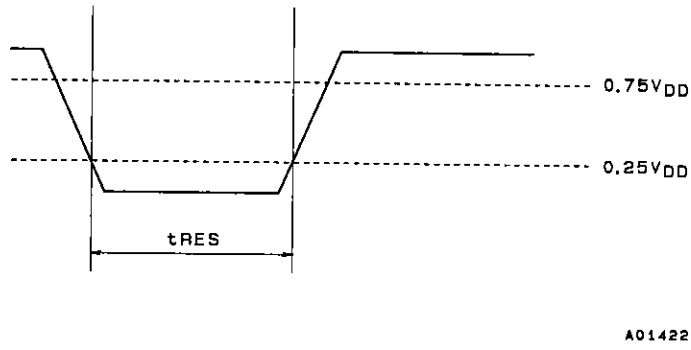


Figure 2 $\overline{\text{RESET}}$ Input Waveform

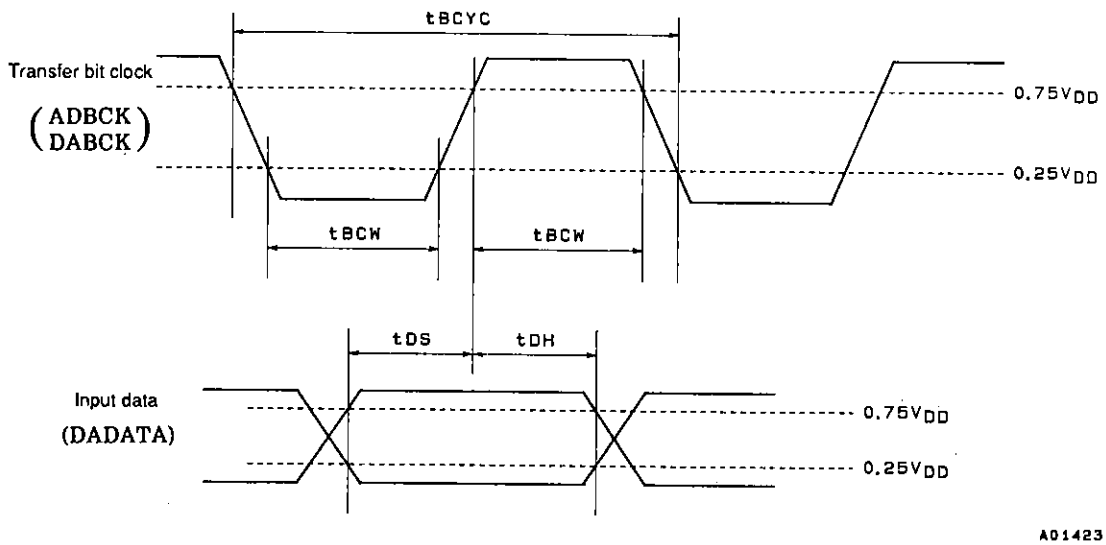


Figure 3 Audio Data Input Conditions

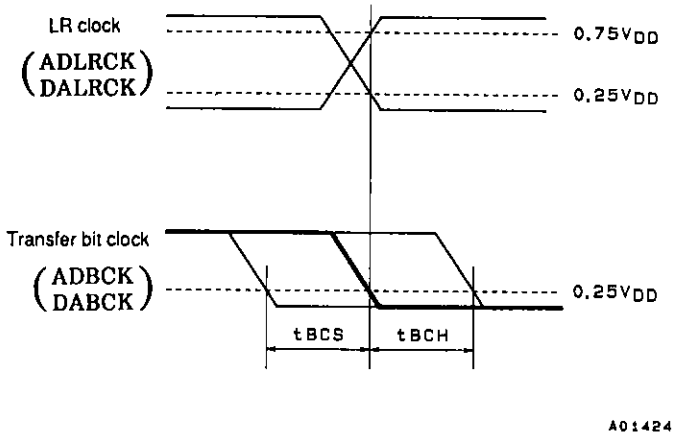


Figure 4 Audio Clock Input Conditions

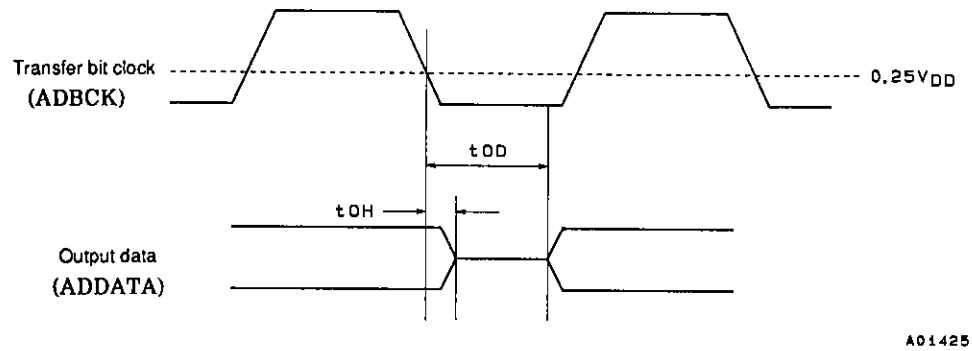


Figure 5 Audio Data Output Timing

Master Clock Setting

Set the CLKCTL pin to match the oscillator frequency as shown in the table below.

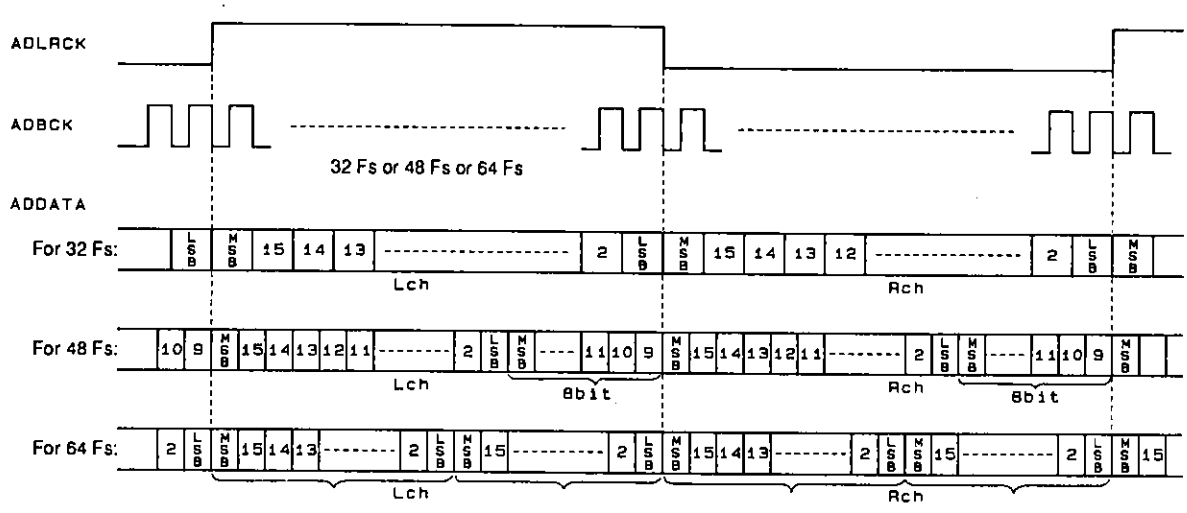
Oscillator frequency	CLKCTL
512 Fs	H
384 Fs	L

Only the A/D converters operate when 384 Fs is selected. The D/A converters do not operate in this mode.

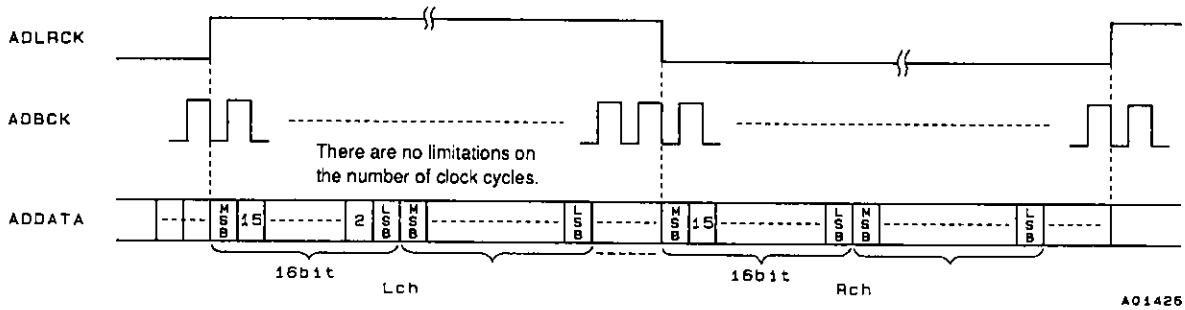
A/D Data Output Format

Always use the standard audio output mode when using this LSI in audio applications.

Standard Audio Output



Arbitrary Timing Output

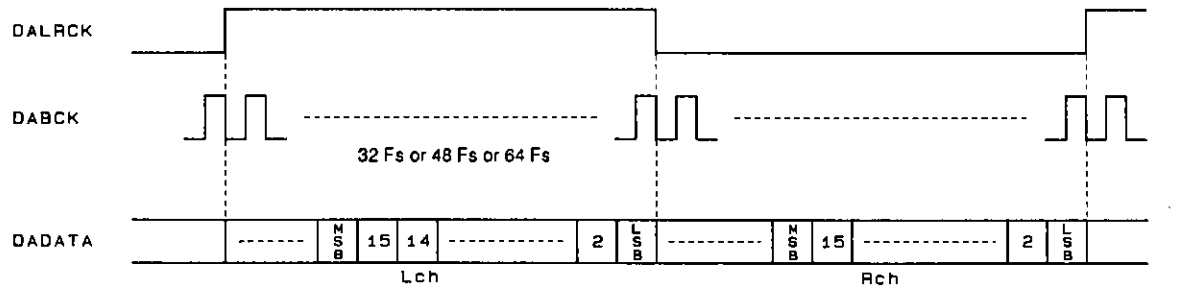


The output data pin (ADDATA) holds the left channel data when ADLRCK rises, and continues to output this value while ADLRCK remains high. Similarly, the right channel data is held when ADLRCK falls, and this value is output while ADLRCK remains low.

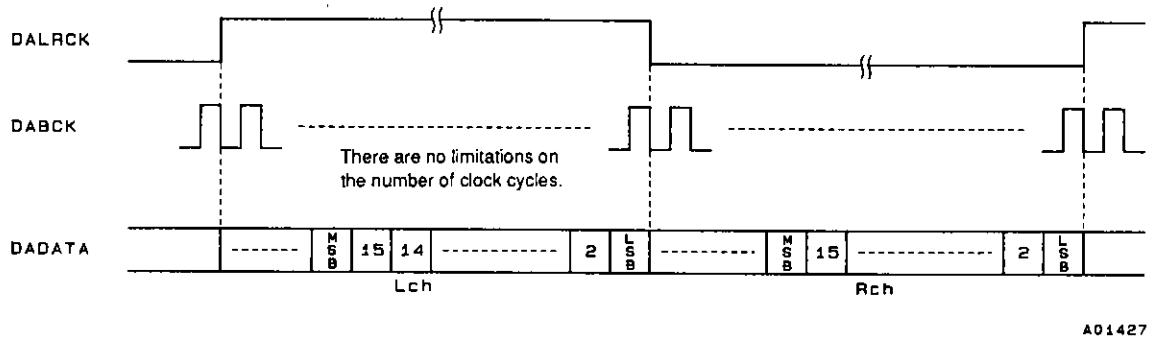
D/A Data Input Format

Always use the standard audio input mode when using this LSI in audio applications.

Standard Audio Input

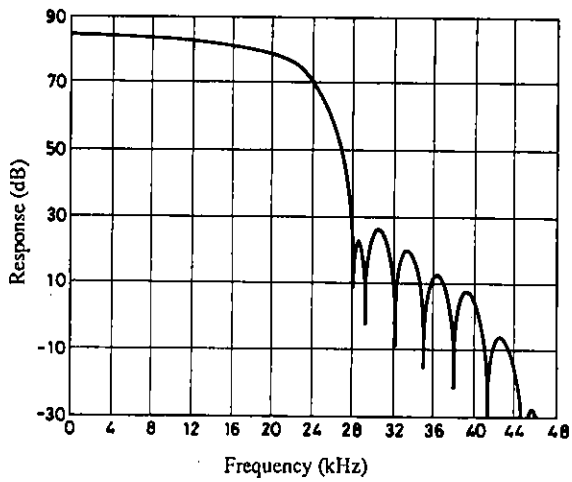


Arbitrary Timing Input



The previous 16 bits of input data are valid on the rise or fall of DALRCK.

A/D Digital Filter Frequency Response (theory values, fs = 48 kHz)



Operating Principles

1. A/D Converter Block

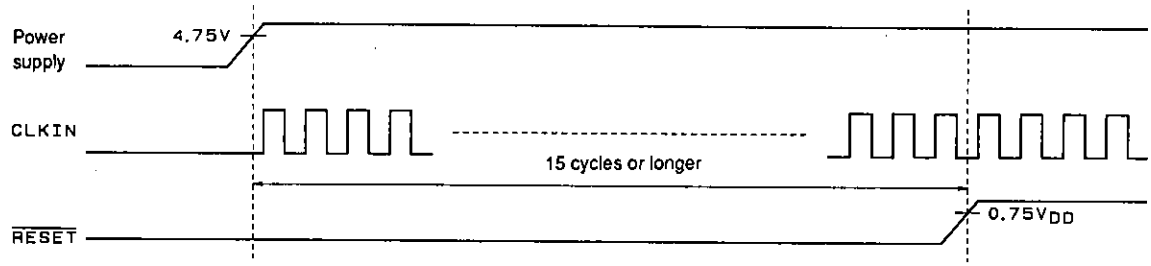
The A/D converter block in this IC is a 2-channel 16-bit A/D converter that uses a quadratic ΔΣ modulation technique. The circuit includes two built-in ΔΣ modulators (although an external integrator is used), and the analog input signals are simultaneously sampled at a 128× sampling rate. The oversampled data is decimated using a digital filter. The output data is serial signed 16-bit two's complement data. When standard audio output is used, simultaneously sampled data is output. When arbitrary timing is used, left channel data is output on the rise of ADLRCK, and right channel data is output on the fall of ADLRCK.

2. D/A Converter Block

The D/A converter block in this IC is a 2-channel 16-bit D/A converter that combines a quadratic noise shaper and PWM (pulse width modulation) techniques. Two PWM generators are built in, and quadratic noise shaping is applied to the data, which is oversampled by holding the previous value (note that digital filters are not built in), and output from the left and right channels at the same time. Input data is serial signed 16-bit two's complement data. Since digital oversampling filters are not built in, steep external low-pass filters (LPF) are required. Input data is acquired on the rising edge of DALRCK for both standard audio input and arbitrary timing input modes. Data is output from the PWM generators at the same time from the left and right channels.

3. Initialization

The LC8390M must be initialized after power is applied and when the sampling period changes. To initialize the LC8390M, once the power supply voltage has stabilized and CLKIN has been supplied, a low level must be input to the $\overline{\text{RESET}}$ pin for a period longer than 15 CLKIN cycles.



Design and Usage Notes

1. External Clock

The CLKIN must not be stopped during operation. If this clock is not supplied, overcurrents may occur since dynamic logic is used internally, and the LC8390M may function abnormally. This IC must synchronize its internal operating timing with the externally supplied ADLRCK and DALRCK. This synchronization is performed by resetting an internal counter. This reset is only performed a few times on the rising edges of ADLRCK and DALRCK following initialization by a $\overline{\text{RESET}}$ pin input. Therefore, the CLKIN, ADLRCK, ADBCK, DALRCK and DABCK clock inputs must be synchronized. However, CLKIN and other clocks do not have to be synchronized for arbitrary timing input and output. Clock jitter will degrade A/D and D/A converter precision in this IC. The wiring lines for the master clock must be kept as short as possible, and a crystal oscillator signal level clock should be used.

2. Power Supply and Ground

Use care in supplying power and ground to this IC. Separate the analog and digital blocks, and provide a separate ground plane for each. Connect the analog and digital grounds to points near the power supply on the PC board. While DV_{DD} is the power supply for the internal logic circuits, since DV_{DD} and the analog system V_{DD} supplies ($ADLV_{DD}$, $ADRV_{DD}$, $DALV_{DD}$ and $DARV_{DD}$) are connected together through the IC substrate with a few Ohms resistance, they should have identical voltages, and care should be exercised in handling the digital system power supply.

3. A/D Block DC Offset Adjustment

A DC offset component appears in the A/D block digital output due to manufacturing variations in the IC itself and in resistor values. When there is a DC offset, differences in the full scale level of the analog input are created. It is therefore necessary to adjust the DC offset adjustment point in the application circuit example (see the section "LC8390M Application Circuit Example") while monitoring the digital output, and to cut the DC component by performing HPF processing in the input processing block of the later stage DSP.

LC8390M Application Circuit Example