SAMSUNG ELECTRONICS

Data Sheet

Device Name : LCC3600A

Release Date : 2003. 03. 25 (Rev.000)

Samsung Electronics Co . , LTD.

INTRODUCTION

The LCC3600A is a Timing Controller for 240×320 260k-color Gate-IC-less TFT-LCD. This IC can make RGB data signals and control signals for a Source Driver and integrated Gate Driver circuits from input signals such as Data Enable, Main Clock and 6bits RGB data.

FEATURES

- Resolution : 240(Horizontal) × 320(Vertical)
- Generate Gate Clock and Gate Start signal for Integrated Gate Driver
- Generate signals for VCOM
- 6bits RGB Input data for 260K color display
- Function of Gate clock control
- Maximum Operating Frequency : 20MHz
- Operating Voltage : 3.0V ~ 3.6V
- Package : 64-ELP

BLOCK DIAGRAM

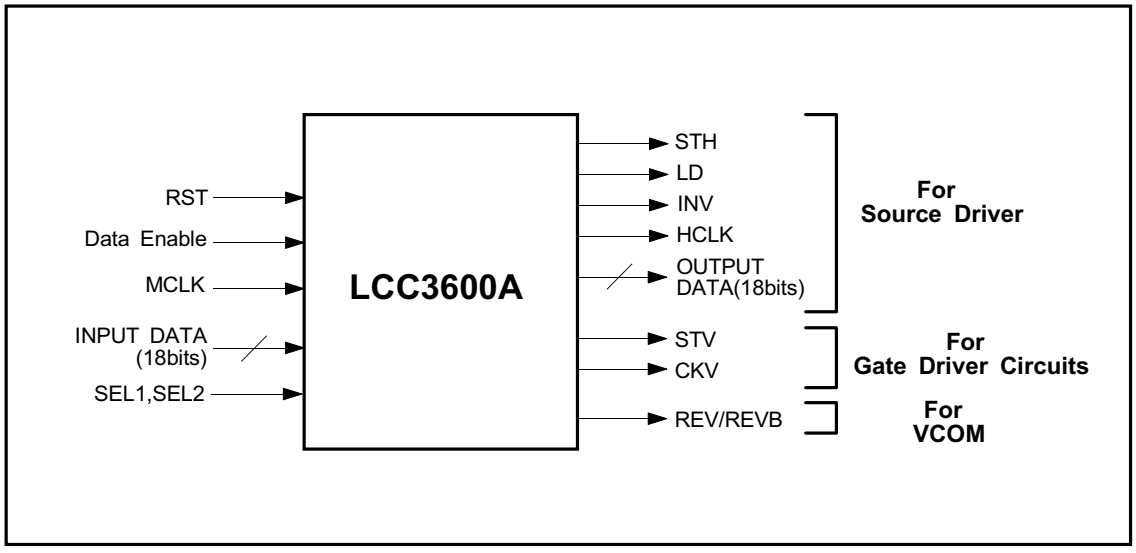


Figure 1. LCC3600A Block Diagram

LCC3600A PAD ARRANGEMENT

- Chip Size : 9.0mm × 9.0mm
- Chip Thickness : 0.75 ± 0.05 mm
- PAD Width : 0.2 +0.10/-0.02mm
- PAD Pitch : 0.5 ± 0.06mm

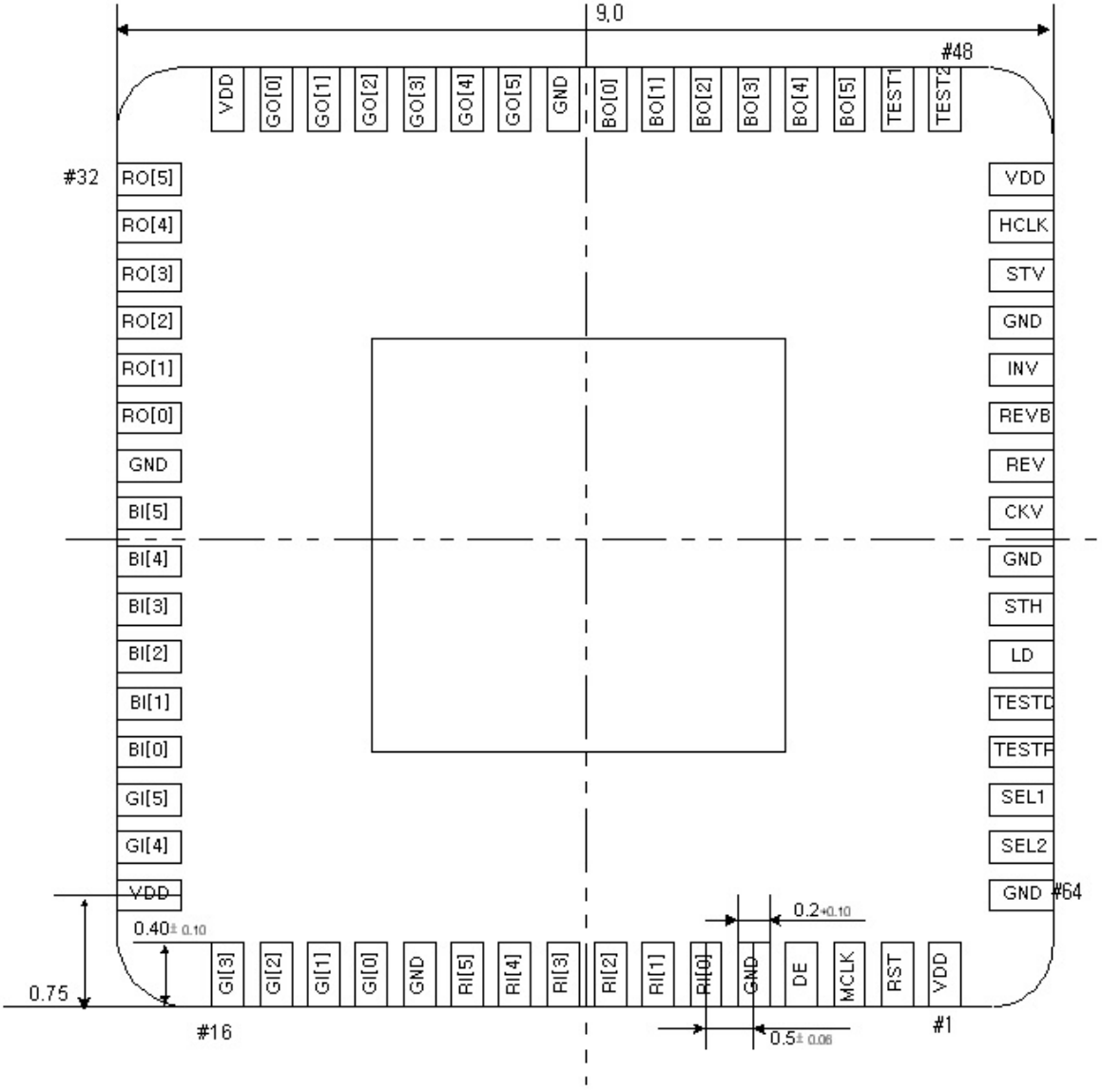


Figure 2. LCC3600A PAD arrangement(Bottom view)

PIN DESCRIPTIONS

SYMBOL	I/O	PIN NUMBER	DESCRIPTIONS
RST	I	2	System Reset Pin. Initializes the IC when low.
MCLK	I	3	Main Clock. Typ=5MHz.
DE	I	4	Data Enabling Signal.
RI[0] ~ RI[5]	I	6~11	6bits Red Input Data.
GI[0] ~ GI[5]	I	13~16,18~19	6bits Green Input Data.
BI[0] ~ BI[5]	I	20~25	6bits Blue Input Data.
RO[0] ~ RO[5]	O	27~32	6bits Red Output Data.
GO[0] ~ GO[5]	O	34~39	6bits Green Output Data.
BO[0] ~ BO[5]	O	41~46	6bits Blue Output Data.
TEST1	I	47	IC Test Input. Leave it open.
TEST2	I	48	IC Test Input. Leave it open.
HCLK	O	50	Shift clock for the Source Driver.
STV	O	51	Start pulse for the Gate Driver Circuits.
INV	O	53	Data inversion signal.
REVB	O	54	Signal for the VCOM generator
REV	O	55	Signal for the VCOM generator
CKV(CPV)	O	56	Shift clock for the Gate Driver Circuits.
STH	O	58	Start pulse for the Source Driver.
TP(LD)	O	59	Latch Input for the Source Driver.
TESTDB	I	60	IC Test Input. Must connect to VDD.
TESTRE	I	61	IC Test Input. Must connect to VDD.
SEL1	I	62	Control signal for CKV signal.
SEL2	I	63	SEL1 / SEL2 / CKV t1 (f=5MHz): L / L / 22 mclks (4.4us); L / H / 25 mclks (5.0us); H / L / 28 mclks (5.6us); H / H / 31 mclks (6.2us) *refer to the Figure3
VDD3I VDD3P VDD3O	-	1,17, 33, 49	Power Supply. 3.0 ~ 3.6V
GNDI GNDP GNDO	-	5,12,26, 40,52, 57,64	Ground(0V)

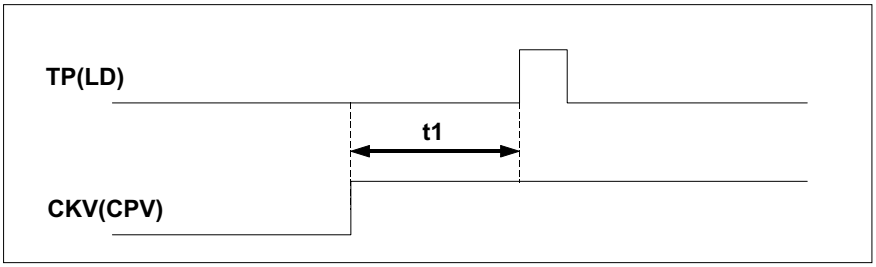


Figure 3. Description for t1

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
DC supply Voltage	V_{DD}	-3.0V to 3.8	V
DC input Voltage	V_{IN}	-0.3V to V_{DD} + 0.3	V
DC input Current	I_{IN}	±10	mA
Storage Temperature	T_{STG}	-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating	Unit
DC supply voltage	V_{DD}	3.0 to 3.6	V
Operating temperature	T_A	0 to 70	°C

ELECTRICAL CHARACTERISTICS

1) DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.0 to 3.6 V, T_A=25℃)

Characteristics	Symbol	Test Condition		Min	Typ	Max	Unit
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	Normal	-10	-	10	μA
Input with pull-down			Down	10	-	60	
Input Low Current	I_{IL}	$V_{IN}=V_{SS}$	Normal	-10	-	10	μA
Input with pull-up			Up	-60	-	-10	
Input High Voltage	V_{IH}	CMOS		0.7V_{DD}	-	-	V
Input Low Voltage	V_{IL}	CMOS		-	-	0.3V_{DD}	V
Output High Voltage	V_{OH}	2mA buffer,I_{OH}=-2mA		2.4	-	-	V
		4mA buffer.I_{OH}=-4mA		2.4	-	-	
Output Low Voltage	V_{OL}	2mA buffer,I_{OL}=2mA		-	-	0.4	V
		4mAbuffer,I_{OL}=4mA		-	-	0.4	

CHARACTERISTIC : These DC parameters guarantee the I/O cell characteristic at the static state only, not at the dynamic state.

* HCLK, STV, CKV : 4mA buffer , Others : 2mA buffer

* Output Load : HCLK : 40pF, Others : 35pF

2) AC ELECTRICAL CHARACTERISTICS

Signal	Description	Symbol	Min	Typ	Max	Unit
MCLK	Frequency	$1/T_C$	-	5	20	MHz
	High level width	T_{CH}	3	-	-	ns
	Low level width	T_{CL}	3	-	-	ns
INPUT DATA	setup time	T_{DS}	3	-	-	ns
	hold time	T_{DH}	3	-	-	ns
DE	setup time	T_{ES}	3	-	-	ns
	hold time	T_{EH}	3	-	-	ns

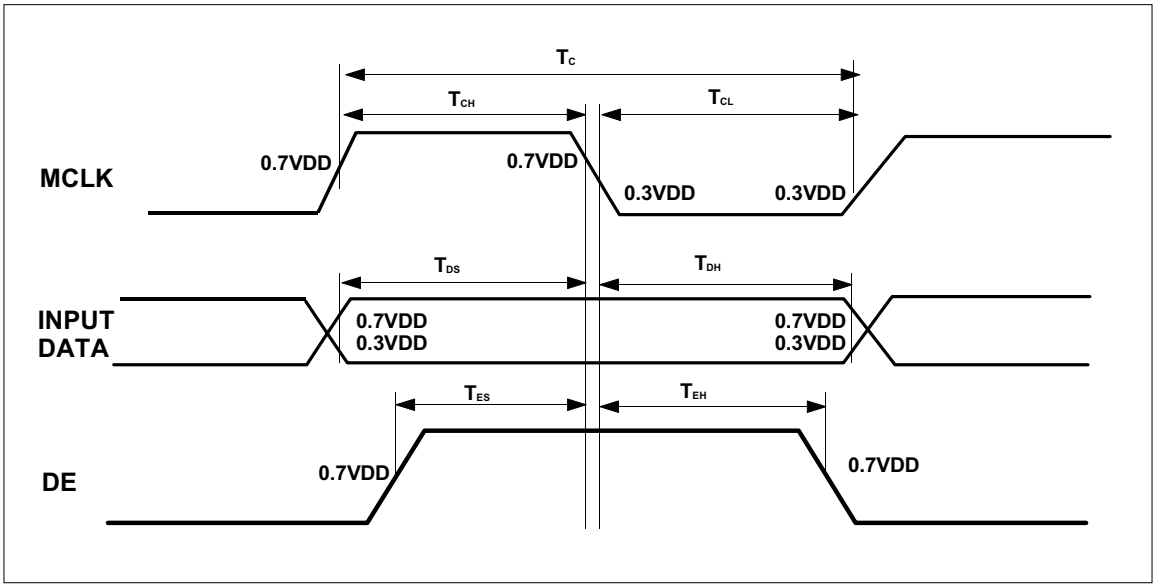


Figure 4. AC Timing Diagram

INPUT TIMING SPEC

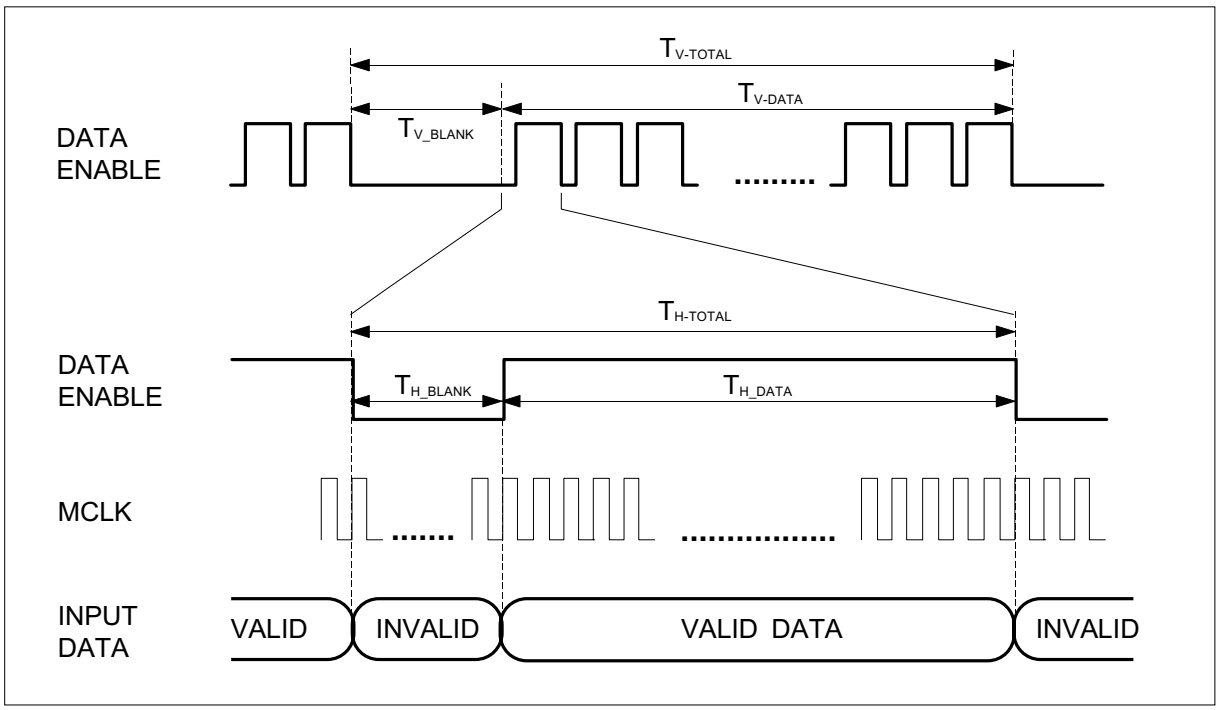


Figure 5. Input Signal Timing Diagram

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Vertical Total	$T_{V\text{-}TOTAL}$	324	327	-	Lines
Vertical Blank Time	T_{V_BLANK}	4	7	-	Lines
Vertical Display	$T_{V\text{-}DATA}$	-	320	-	Lines
Horizontal Total	$T_{H\text{-}TOTAL}$	254	282	512	MCLK
Horizontal Blank Time	T_{H_BLANK}	14	42	272	MCLK
Horizontal Display	T_{H_DATA}	-	240	-	MCLK

OUTPUT TIMING DIAGRAM

Vertical Timing

Vertical Output timing of LCC3600A is same as Figure 6 according to Data Enable signal. Output signals was divided into STH, LD, INV, 18bits RGB data as Input signals of Source Driver and STV, CKV as Input signals of Gate Driver and REV, REVB as generating signals of VCOM.

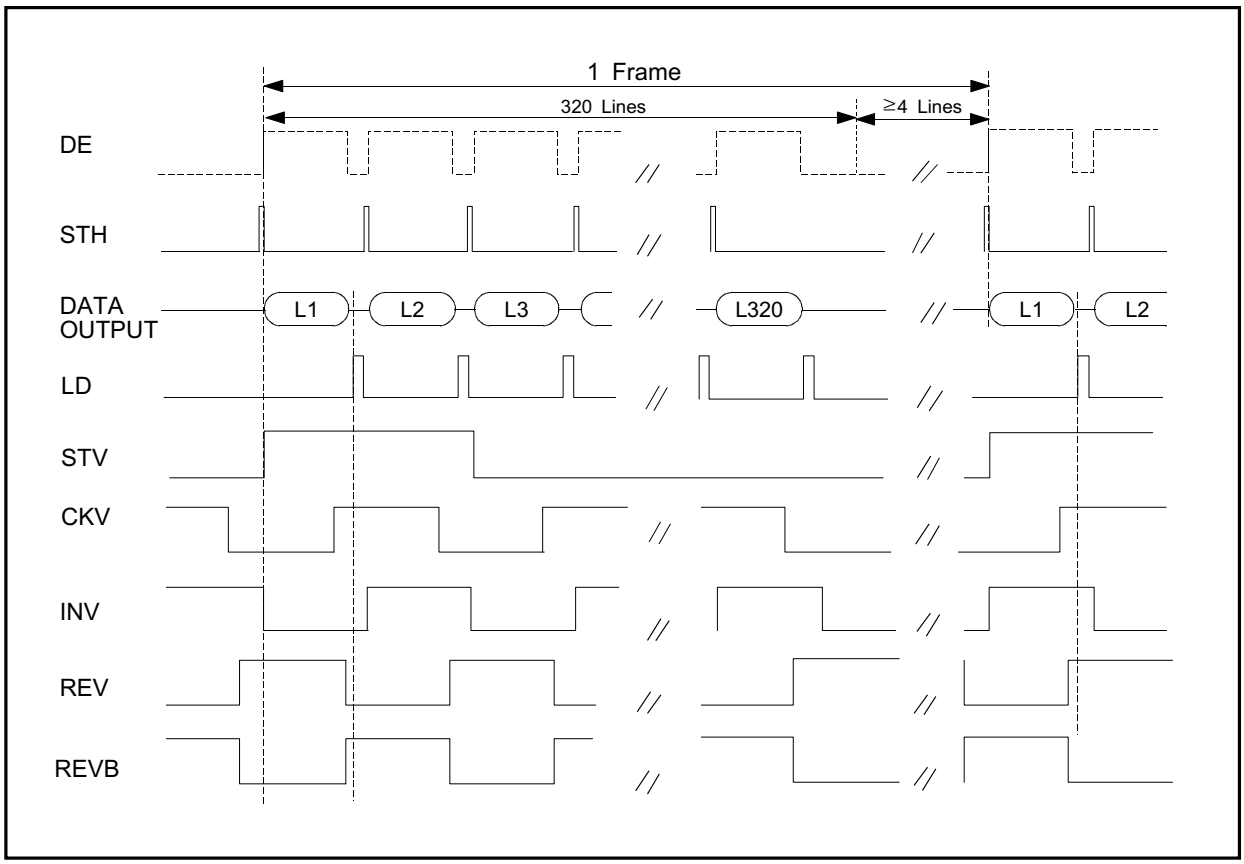


Figure 6. OUTPUT Timing Diagram1

- STH is a start-carry signal of Source driver that would be latched from High-edge of next clock after STH pulse High. After latching 240 Input data to Source driver, LD would be High that means to transmit the saved signals from Latch band to DAC. Please refer to Figure 7 in detail.
- INV is a Input signal of Source driver that would determine the data polarity of Latch band. INV has a period of 2H, because of Line Inversion.
- REV & REVB is to generate VCOM and have a period of 2H. Please, refer to Figure 7 in detail.

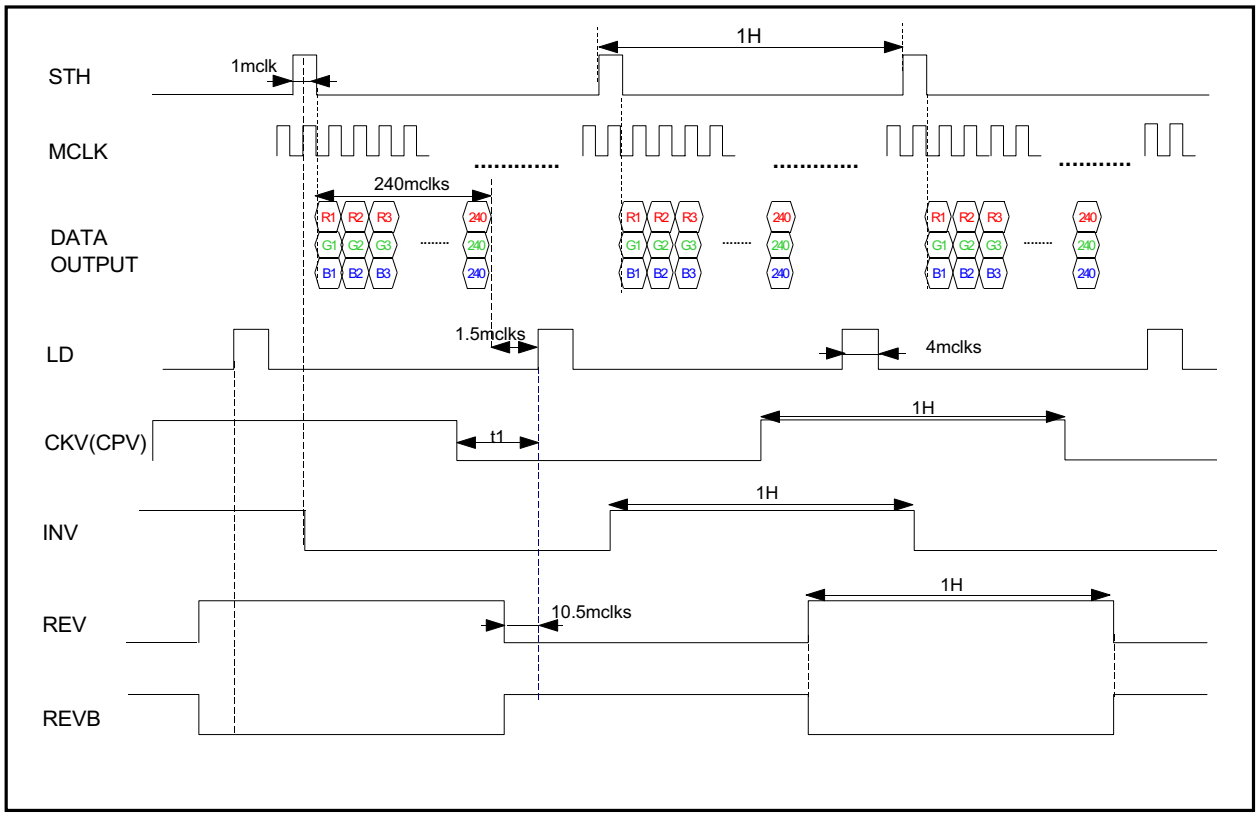


Figure 7. OUTPUT Timing Diagram2

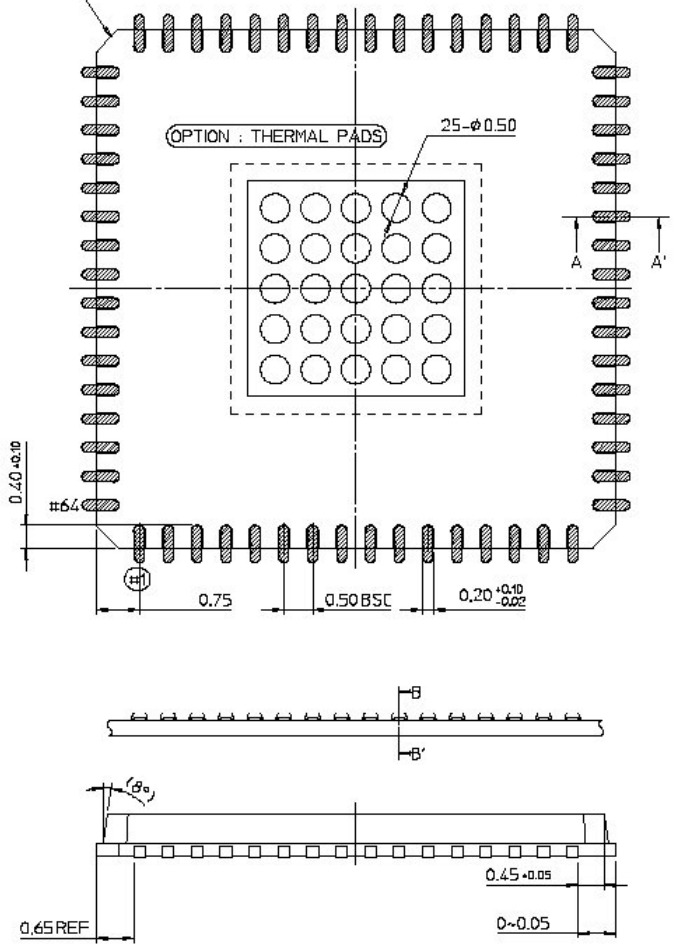
- STV & CKV is for Gate driver circuits integrated in TFT-LCD.
- STV is a vertical start pulse that generate a pulse each starting time of frame.
  The high of pulse has a period of 2H according to characteristics of panel.
- CKV is a vertical shift clock that has a period of 2H.
  A interval(t1) between CKV falling-edge and LD rising-edge could be adjusted by option-pin SEL1/SEL2. Please refer to following table.
- It is recommended SEL1/2=L/H for the best display quality, if "f_{mclk}= 5MHz".

SEL1	SEL2	CKV t1(f_{mclk}=5MHz)
L	L	22 mclks (4.4us)
L	H	25 mclks (5.0us)
H	L	28 mclks (5.6us)
H	H	31 mclks (6.2us)

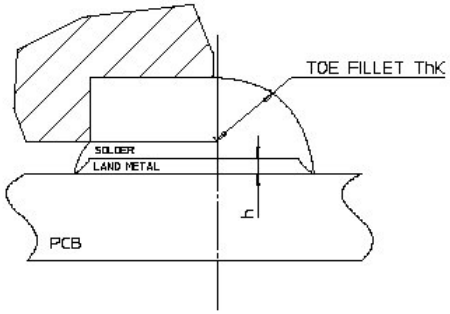
- Other timing conditions were adjusted by LCC3600A according to characteristics of panel.
  If the timing conditions were adjusted abnormally, the panel could have a abnormal display.

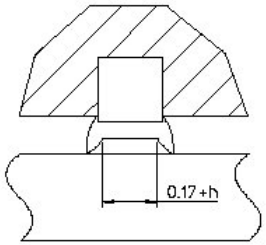
REV.	DATE	ECN#
00	2002. 02. 01.	

PKG OUTLINE

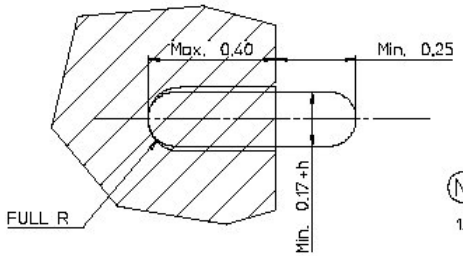


SECTION B-B'





SECTION A-A'



OPTION TABLE

OPTION	DESCRIPTION
A	NO THERMAL PADS
B	WITH THERMAL PADS

NOTE

1. The solder joint reliability depends on The Toe Fillet Thickness. It must be made as thick as possible.
2. The stencil aperture opening should be so designed that maximum paste release is achieved.
3. The stencil thickness of 0.125mm is recommanded for this component.
4. For optimum paste release the area and aspect ratios should be greater than 0.66 and 1.50 respectively.
   Area Ratio = Area of Aperture Opening / Aperture Wall Area.
   Aspect Ration = Aperture Width / Stencil Thickness.
5. The thermal pads improve thermal and electrical performance of this package.

TITLE		DESIGNER
64-ELP-0909 PCB BOARD GUIDE LINE		K.L.JANG
UNIT: mm	TOLERANCE: ±0.05	SCALE: 13/1
SHEET: 1/1		
DWG. NO.: JK-010XX-0	SPEC NO.: ADSXXXXX	ELECTRONICS