Leadtrend

LD7550

8/27/2004

Green-Mode PWM Controller

General Description

The LD7550 is a low cost, low startup current, current mode PWM controller with green-mode power-saving operation. The integrated functions such as the leading-edge blanking of the current sensing, internal slope compensation and the small SOT-26 package provide the users a high efficiency, low external component counts, and low cost solution for AC/DC power applications.

The special green-mode control is not only to achieve the low power consumption but also to offer a non-audible-noise operation when the LD7550 is operating under light load or no load condition.

The LD7550 is designed for the low power adaptor or charger applications. The LD7550 is with both SOT-26 and DIP-8 package.
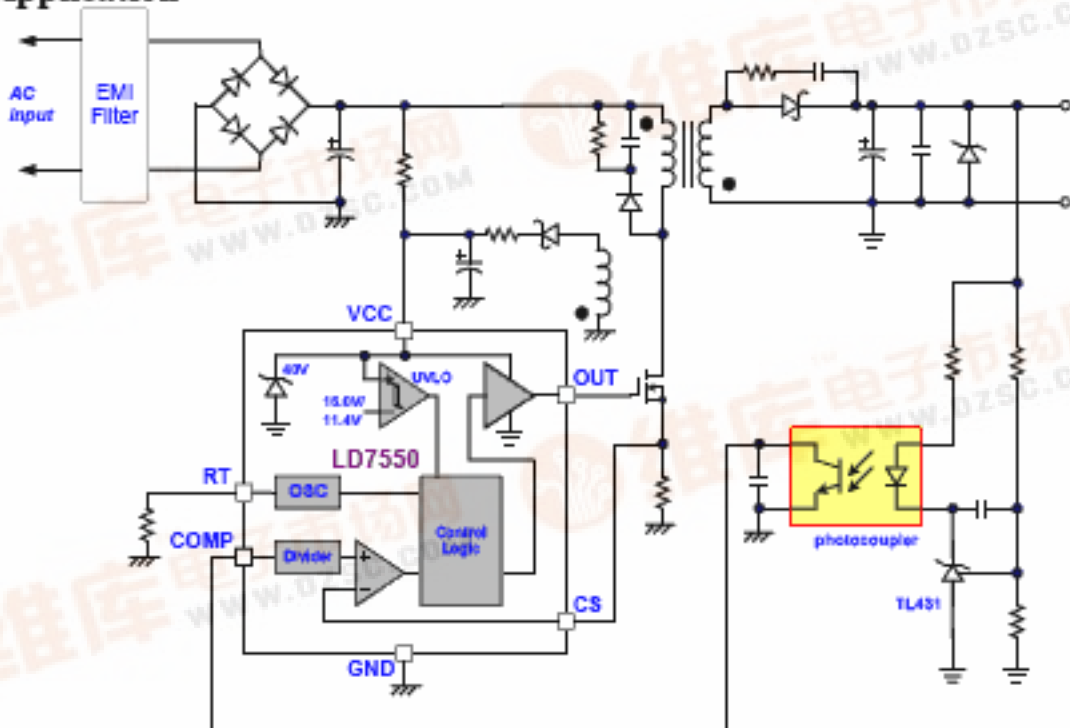
† Patent pending

Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (Typical 5µA)
- Under Voltage Lockout (UVLO)
- Current Mode Control with Cycle-by-Cycle Peak Current Limiting
- Leading-Edge Blanking on CS Pin
- Programmable Switching frequency
- Internal Slope Compensation
- Proprietary Green-Mode Control for Power Saving ⓐ
- Non-audible-noise Green Mode Control
- 300mA Driving Capability

Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- 384X Replacement

ⓐ Note: Please see Application Information
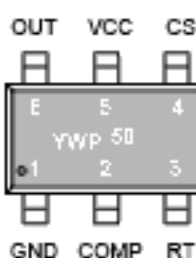
Typical Application

Leadtrend Technology Corporation
LD7550-DS-00 July 2004

Pin Configuration

DIP-8 (TOP VIEW)   SOT-26 (TOP VIEW)

GND COMP NC RT

TOP MARK
YYWW##

OUT VCC NC CS

OUT VCC CS

E   5   4
YWP 50
1   2   3

GND COMP RT

YY, Y : Year code
WW, W: Week code
P   : LD75..
        (Product family code)
##   : Production code

Ordering Information

Part number	Temperature range	Package	TOP MARK	Shipping
LD7550 IL		SOT-26	YWP/50	3000 /tape & reel
LD7550 IN	-30 to 85 (˚C)	DIP-8	LD7550IN	3600 /tube
LD7550 BL		SOT-26 (PB free)	(*) YWP/50	3000 /tape & reel
LD7550 BN		DIP-8 (PB free)	LD7550BN	3600 /tube

(*)   Identified in different laser ink

Pin Descriptions

PIN (DIP-8)	PIN (SOT-26)	NAME	FUNCTION
1	6	OUT	Gate drive output to drive the external MOSFET
2	5	VCC	Supply voltage pin
3		NC	Unconnected pin
4	4	CS	Current sense pin, connect to sense the MOSFET current
5	3	RT	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency.
6		NC	Unconnected pin
7	2	COMP	Voltage feedback pin (same as the COMP pin in UC384X), By connecting a photo-coupler to close the control loop and achieve the regulation.
8	1	GND	Ground

Block Diagram
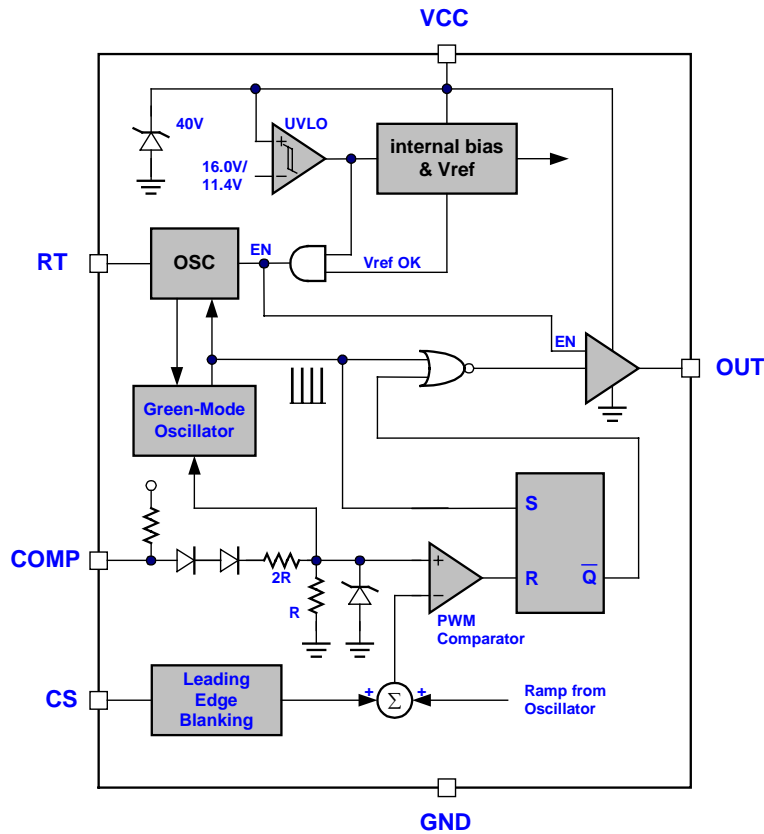
Absolute Maximum Ratings

Supply Voltage VCC	36V
COMP, RT, CS	-0.3 ~7V
Operating Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package thermal resistance (DIP-8)	100°C/W
Package thermal resistance (SOT-26)	250°C/W
Lead temperature (DIP-8, Soldering, 10sec)	260°C
Lead temperature (SOT-26, Soldering, 10sec)	260°C

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not limited.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			5	25	μA
Operating Current	V_{COMP}=0V		3	4	mA
	V_{COMP}=3V		2		mA
	V_{COMP}=open		0.7		mA
UVLO (off)		10.4	11.4	12.4	V
UVLO (on)		14.8	16.0	17.5	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		2.2	3.0	mA
Open Loop Voltage	COMP pin open		5.0		V
Green Mode Threshold VCOMP			2.35		V
Current Sensing (CS Pin)					
Maximum Input Voltage		0.80	0.85	0.90	V
Leading Edge Blanking Time			250		nS
Input impedance			50		KΩ
Delay to Output			300		nS
Oscillator (RT pin)					
Frequency	RT=100KΩ	61.5	66.5	71.5	KHz
Green Mode Frequency	Fs=66.5KHz		20		KHz
Temp. Stability	(-30°C ~85°C)			5	%
Voltage Stability	(VCC=12V-30V)			2	%
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	8			V
Rising Time	Load Capacitance=1000pF		50	200	nS
Falling Time	Load Capacitance=1000pF		30	125	nS

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Typical Performance Characteristics
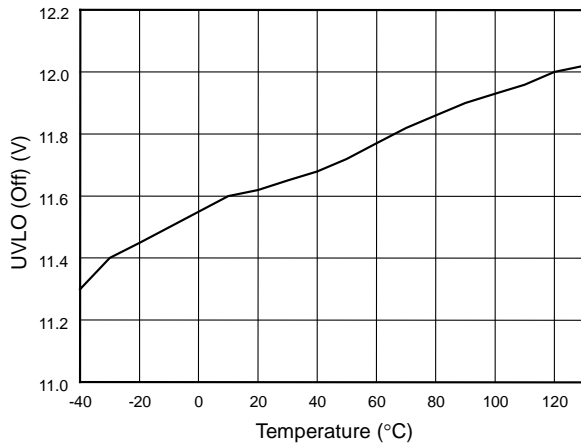

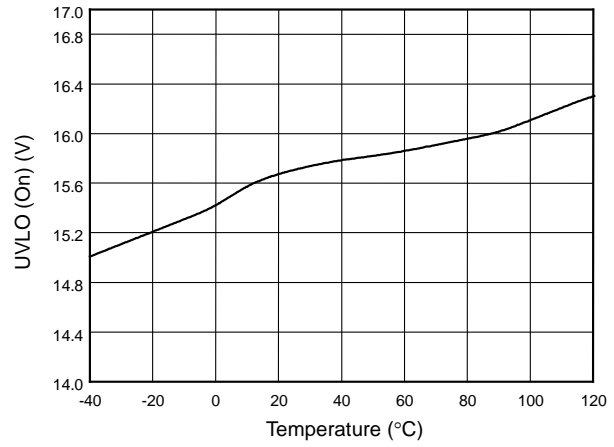Fig. 1   UVLO (Off) vs. Temperature

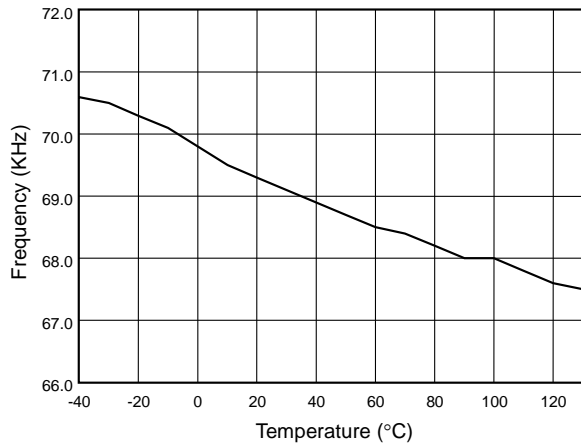Fig. 2   UVLO (On) vs. Temperature

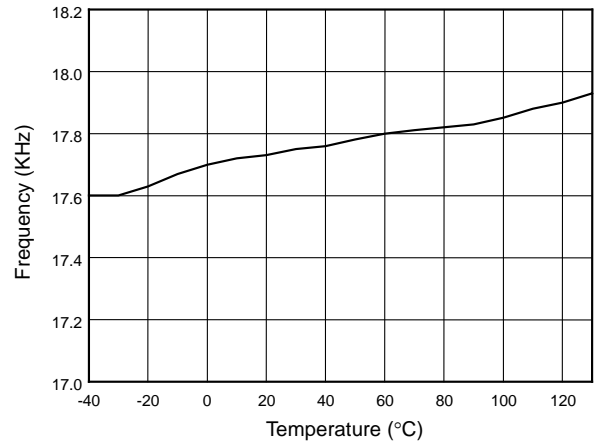Fig. 3   Frequency vs. Temperature

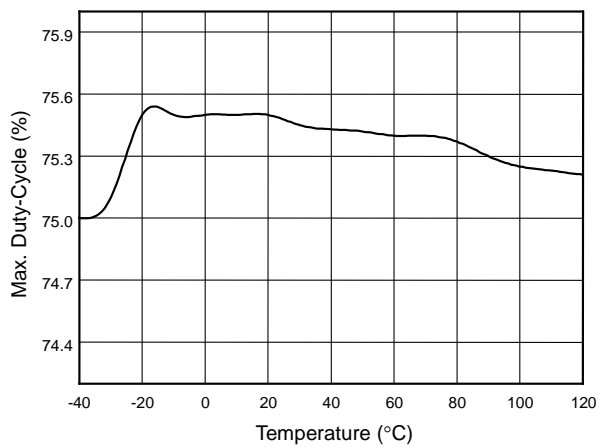Fig. 4   Green-Mode Frequency vs. Temperature

Fig. 5   Duty-Cycle (max.) vs. Temperature

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Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers need to be powerful to integrate more functions to reduce the external part counts. The LD7550 is targeted on such application to provide an easy and cost effective solution; its detail features are described as below:

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented to detect the voltage on the Vcc pin to ensure the supply voltage is enough to power on the LD7550 PWM controller and further to drive the power MOSFET. As shown in Fig. 6, a hysteresis is implemented to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 11.4V, respectively.
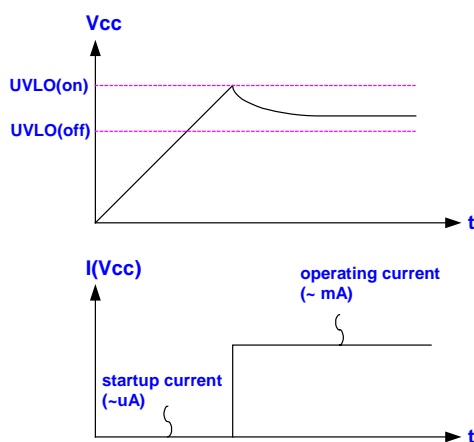

Fig. 6

Startup Current and Startup Circuit

The typical startup circuit to power up the LD7550 is shown in Fig. 7. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse generated from LD7550 to drive power MOSFET. Therefore, the current through R1 is to provide the startup current as well as charge the capacitor C1. Whenever the Vcc voltage is higher enough to power on the LD7550 and further to

deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. The lower startup current requirement on the PWM controller will help to increase the R1 value and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7550 is only 25µA.

Theoretically, R1 can be very high resistance value. However, higher R1 will cause longer startup time. By properly select the value of R1 and C1; it can be optimized under the consideration of R1 power consumption and the startup time.
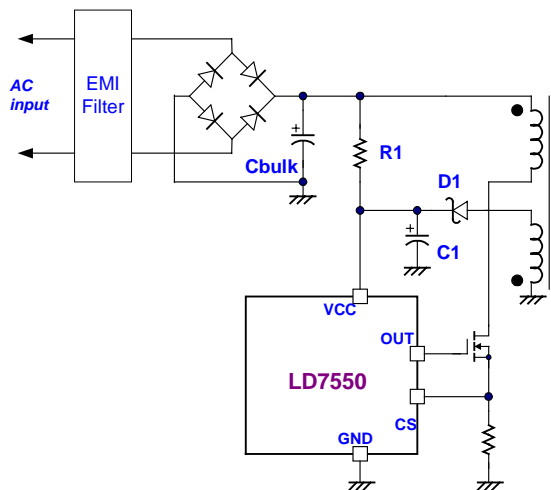

Fig. 7

Current Sensing and Leading-edge Blanking

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 8, the LD7550 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

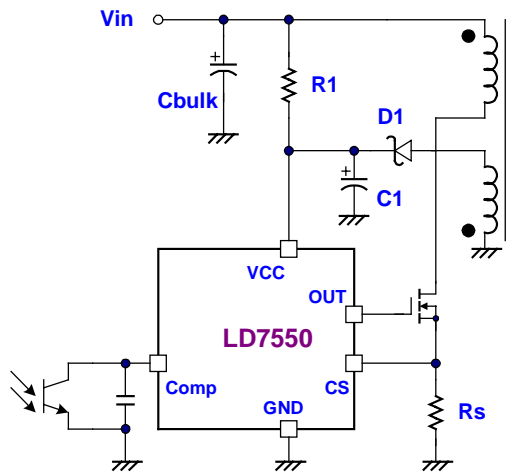$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

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Fig. 8

A 250nS leading-edge blanking time is included in the input of CS pin to prevent the false-trigger caused by the current spike and further to eliminate the need of R-C filter which is usually needed in the typical UC384X application (Fig. 9).
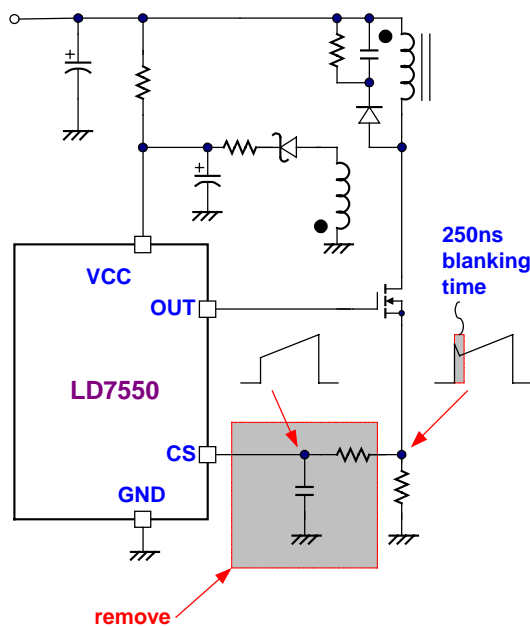

Fig. 9

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly.   And the maximum duty-cycle of LD7550 is limited to 75% to avoid the transformer saturation.

Oscillator and Switching Frequency

Connecting a resistor from RT pin to GND according to the equation can program the normal switching frequency:

$$f_{SW} = \frac{66.5}{RT_{(K\Omega)}} \times 100 (KHz)$$

The suggested operating frequency range of LD7550 is within 50KHz to 130KHz.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 in the secondary side through the photo-coupler to the COMP pin of LD7550.   The input stage of LD7550, like the UC384X, is with 2 diodes voltage offset then feeding into the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally thus can be eliminated on the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated more than 50%. To stabilize the control loop, the slope compensation is needed in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In LD7550, the internal slope compensation circuit has been implemented to simplify the external circuit design.

On/Off Control

The LD7550 can be controlled to turn off by pulling COMP pin to lower than 1.2V.   The gate output pin of LD7550 will be disabled immediately under such condition. The off mode can be released when the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are many difference topologies has been implemented in different chips for the green-mode or power saving requirements such as "burst-mode control", "skipping-cycle Mode", "variable off-time control "…etc. The basic operation theory of all these approaches intended to

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reduce the switching cycles under light-load or no-load condition either by skip some switching pulses or reduce the switching frequency.

What LD7550 used to implement the power-saving operation is Leadtrend Technology's own IP[2]. In such approach, as shown in the block diagram, 2 oscillators are implemented in LD7550. The first oscillator is to take care the normal switching frequency, which can be set by the RT pin through an external resistor. Under this operation mode, as shown in Fig. 10, the 2nd oscillation (green-mode oscillator) is not activated. Therefore, the rising-time and the falling-time of the internal ramp will be constant to achieve good stability over all temperature range. Under the normal operation, this oscillator is dominated the switching frequency.
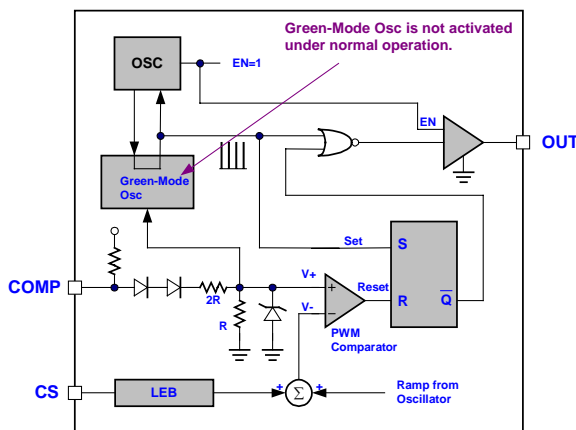

Fig. 10

As shown in Fig. 11, the green-mode oscillator detects the Comp pin signal to determine if it is within the green-mode operation. When the detected signal V+ is lower than the green-mode threshold V_{GREEN}, the green-mode oscillator is on. The green-mode oscillator, implemented by a VCO

(voltage controlled oscillator), is a variable frequency oscillator. The rising time of the VCO is proportional to (V_{GREEN}-V+), thus the lower voltage on V+ will generate longer rising time on VCO as well as lower frequency on VCO.

By using this dual-oscillator control, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.
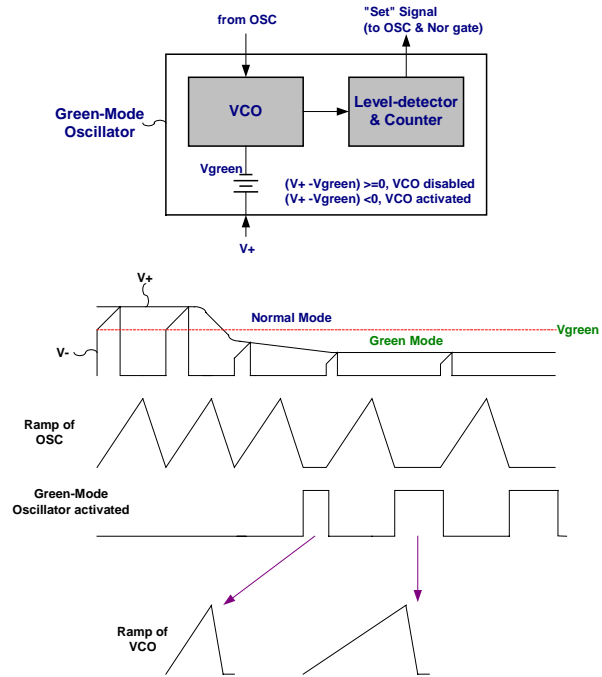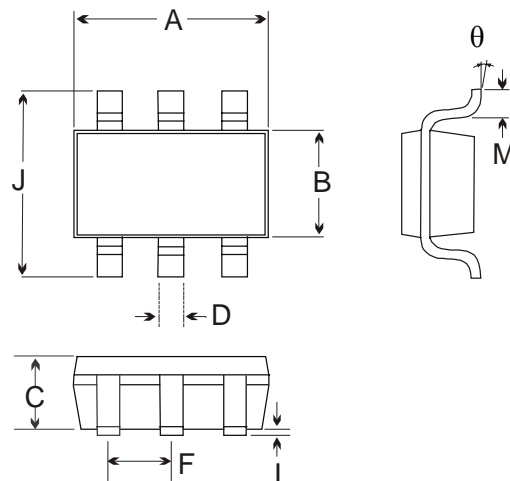

Fig. 11

② Note: Patent pending

Package Information

SOT-26

Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
	0	10 $^{\circ}$	0	10 $^{\circ}$

DIP-8
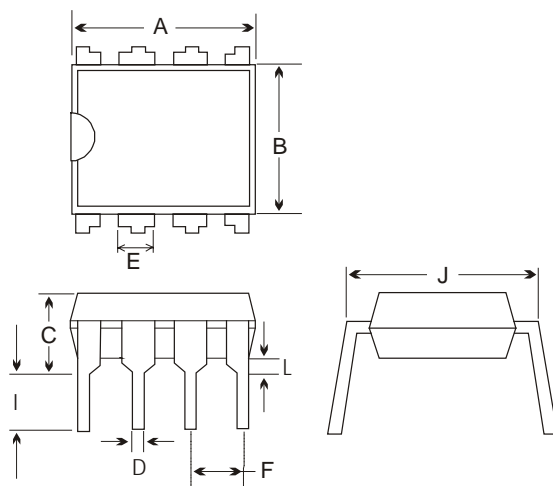
Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	**Max**	**Min**	**Max**
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.14
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

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