National Semiconductor

February 1995

LF13006/LF13007 Digital Gain Set

General Description

The LF13006 and LF13007 are precision digital gain sets used for accurately setting non-inverting op amp gains. Gains are set with a 3-bit digital word which can be latched in with $\overline{WR}$ and $\overline{CS}$ pins. All digital inputs are TTL and CMOS compatible.

The LF13006 shown below will set binary scaled gains of 1, 2, 4, 8, 16, 32, 64, and 128. The LF13007 will set gains of 1, 2, 5, 10, 20, 50, and 100 (a common attenuator sequence). In addition, both versions have several taps and two uncommitted matching resistors that allow customization of the gain.

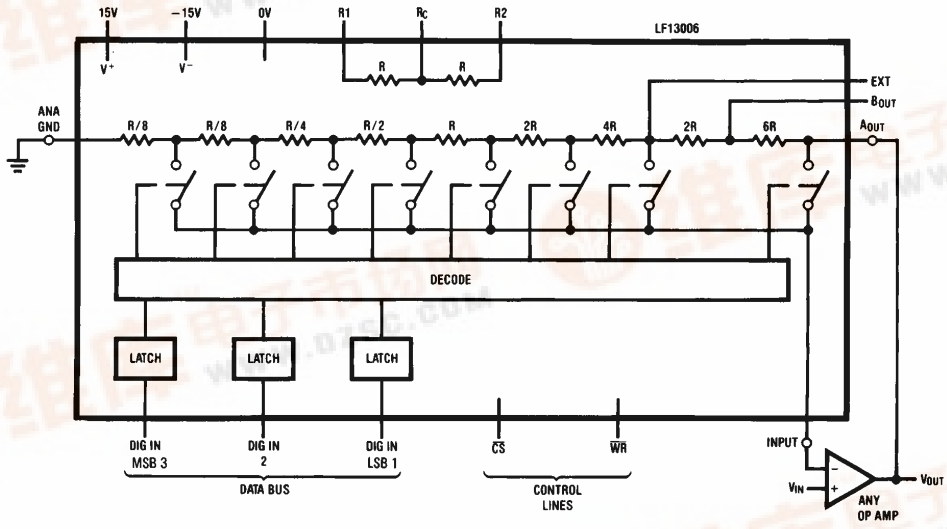
The gains are set with precision thin film resistors. The low temperature coefficient of the thin film resistors and their excellent tracking result in gain ratios which are virtually independent of temperature.

The LF13006, LF13007 used in conjunction with an amplifier not only satisfies the need for a digitally programmable amplifier in microprocessor based systems, but is also useful for discrete applications, eliminating the need to find 0.5% resistors in the ratio of 100 to 1 which track each other over temperature.

Features

- TTL and CMOS compatible logic levels
- Microprocessor compatible
- Gain error 0.5% max
- Binary or scope knob gains
- Wide supply range + 5V to ± 18V
- Packaged in 16-pin DIP

Block Diagram and Typical Application (LF13006)



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Note: R ≅ 15 kΩ

Order Number LF13006N or LF13007N
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+ to V^-	36V
Supply Voltage, V^+ to GND	25V
Voltage at Any Digital Input	V^+ to GND
Analog Voltage	V^+ to (V^- + 2V)

Operating Ratings (Note 1)

Operating Temperature Range	−40°C to +85°C
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics (Note 2)

Parameter	Conditions	Typ (Note 3)	Tested Limit (Note 4)	Design Limit (Note 5)	Units
Gain Error	A_{OUT} = ±10V ANA GND = 0V I_{INPUT} < 10 nA	0.3	0.5	**0.5**	%(max)
Gain Temperature Coefficient	A_{OUT} = ±10V ANA GND = 0V	0.001			%/°C
Digital Input Voltage Low High		 1.4 1.6	 0.8 2.0	 **0.8** **2.0**	 V(max) V(min)
Digital Input Current Low High	 V_{IL} = 0V V_{IH} = 5V	 −38 0.0001	 −100 1	 **−100** **1**	 μA(max) μA(max)
Positive Power Supply Current	All Logic Inputs Low	2	5	**5**	mA(max)
Negative Power Supply Current	All Logic Inputs Low	−1.7	−5	**−5**	mA(max)
$\overline{\text{Write}}$ Pulse Width, t_W	V_{IL} = 0V, V_{IH} = 5V		150		ns(min)
$\overline{\text{Chip Select}}$ Set-Up Time, t_{CS}	V_{IL} = 0V, V_{IH} = 5V		250		ns(min)
$\overline{\text{Chip Select}}$ Hold Time, t_{CH}	V_{IL} = 0V, V_{IH} = 5V		0		ns(min)
DIG IN Set-Up Time, t_{DS}	V_{IL} = 0V, V_{IH} = 5V		150		ns(min)
DIG IN Hold Time, t_{DH}	V_{IL} = 0V, V_{IH} = 5V		60		ns(min)
Switching Time for Gain Change	(Note 4)	200			ns(max)
Switch On Resistance		3			kΩ
Unit Resistance, R		15	12–18		kΩ
R1 and R2 Mismatch		0.3	0.5	**0.5**	%(max)
R1/R2 Temperature Coefficient		0.001			%/°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Parameters are specified at V^+ = 15V and V^- = −15V. Min V^+ to ground voltage is 5V. Min V^+ to V^- voltage is 5V. **Boldface numbers apply over full operating temperature ranges.** All other numbers apply at $T_A = T_j = 25°C$.

Note 3: Typicals are at 25°C and represent most likely parametric norm.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the operating temperature. These limits are not used to calculate outgoing quality levels.

Note 6: Settling time for gain change is the switching time for gain change plus settling time (see section on Settling Time).

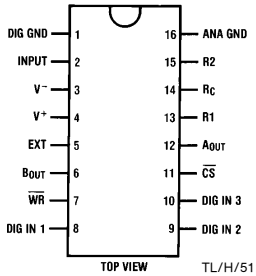
Note 7: $\overline{WR}$ minimum high threshold voltage increases to 2.4V under the extreme conditions when all three digital inputs are simultaneously taken from 0V to 5V at a slew rate of greater than 500V/μS.

GAIN TABLE

Digital Input			Gain			
			LF13006		LF13007	
DIG in 3	DIG in 2	DIG in 1	A_{OUT}	B_{OUT}	A_{OUT}	B_{OUT}
0	0	0	1	1	1	1
0	0	1	2	1.25	1.25	1
0	1	0	4	2.5	2	1.6
0	1	1	8	5	5	4
1	0	0	16	10	10	8
1	0	1	32	20	20	16
1	1	0	64	40	50	40
1	1	1	128	80	100	80

Connection Diagram

Dual-In-Line Package



TOP VIEW

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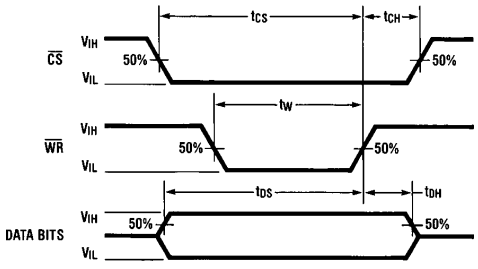
Switching Waveforms



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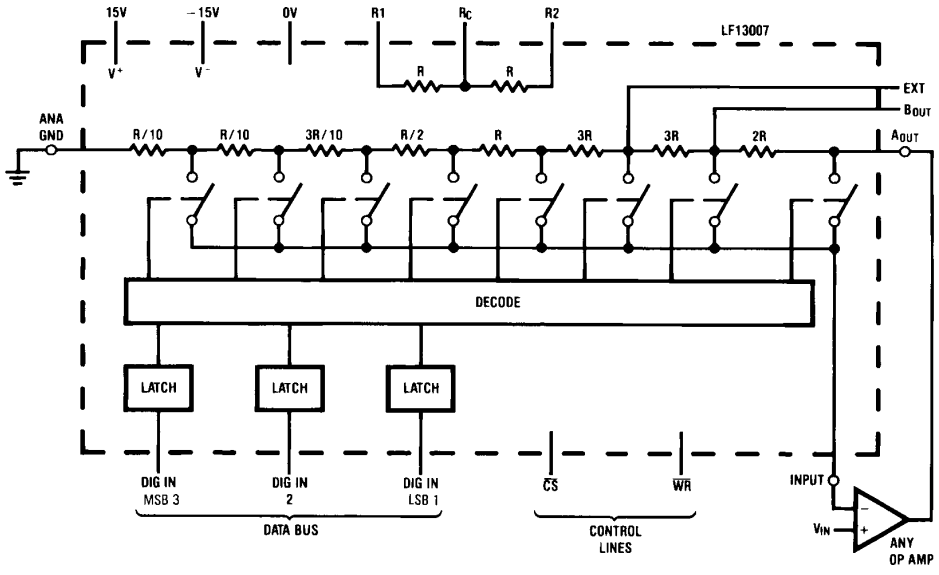
Block Diagram and Typical Application (Continued) (LF13007)



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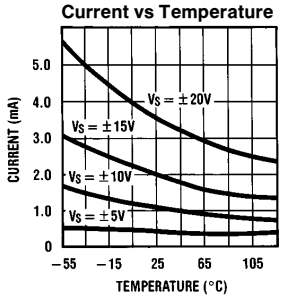
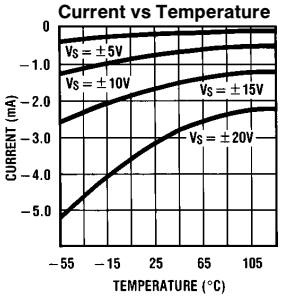
Note: R ≅ 15 kΩ

Typical Performance Characteristics

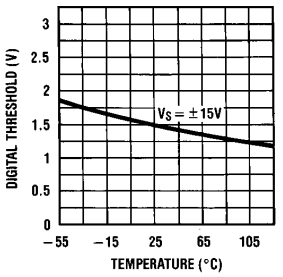
Positive Power Supply Current vs Temperature



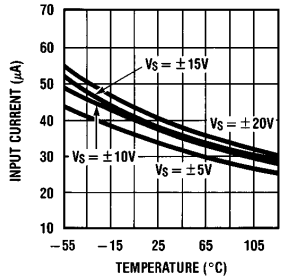
Negative Power Supply Current vs Temperature



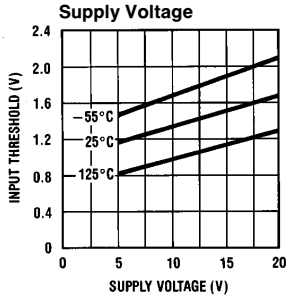
Digital Input Threshold vs Temperature



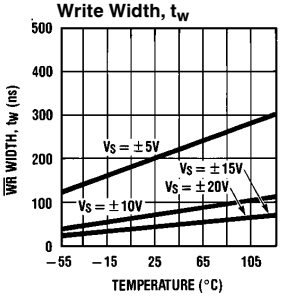
Logical 0 Input Bias Current vs Temperature



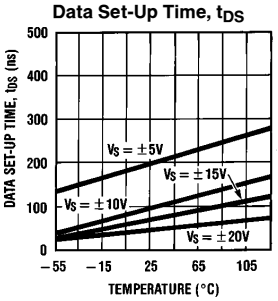
Digital Input Threshold vs Supply Voltage



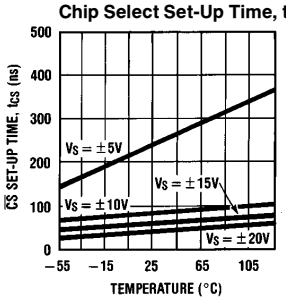
Write Width, t_W



Data Set-Up Time, t_{DS}



Chip Select Set-Up Time, t_{CS}



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Application Information

FLOW-THROUGH OPERATION

THE LF13006, LF13007 can be operated with control lines $\overline{CS}$ and $\overline{WR}$ grounded. In this mode new data on the digital inputs will immediately set the new gain value. Input data cannot be latched in this mode.

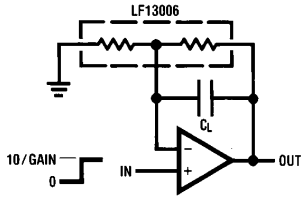
INPUT CURRENT

Current flowing through the input (pin 2) due to bias current of the op amp will result in a gain error due to switch impedance. Normally this error is very small. For example, 10 nA of bias current flowing through 3 kΩ of switch resistance will result in an error of 30 μV at the summing node. However, applications that have significant current flowing through the input must take this effect into account.

SETTLING TIME

Settling time is a function of the particular op amp used with the LF13006/7 and the gain that is selected. It can be optimized and stability problems can be prevented through the use of a lead capacitor from the inverting input to the output of the amplifier. A lead capacitor is effective whenever the feedback around an amplifier is resistive, whether with discrete resistors or with the LF13006/7. It compensates for the feedback pole created by the parallel resistance and capacitance from the inverting input of the op amp to AC ground.

Settling Time Test Circuit



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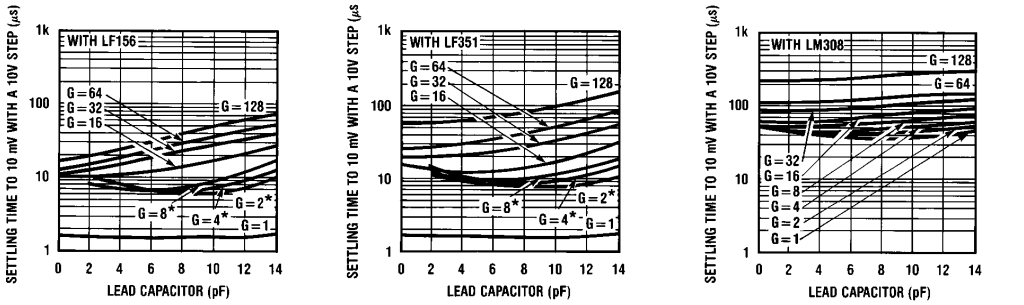
Typical Settling Time Curves



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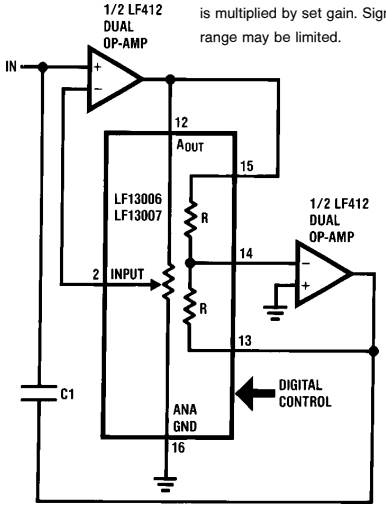
* Unstable at C_L less than 2 pF

Typical Applications

Variable Capacitance Multiplier

$C_{effective} = C1(\text{gain set } \#)$

Note: Output swing at input op amp is multiplied by set gain. Signal range may be limited.



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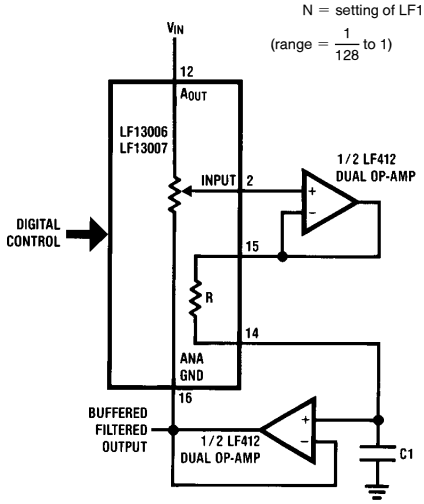
Variable Time Constant Filter

$$\text{Time constant} = \frac{R}{N} C1$$

N = setting of LF13006

$$(\text{range} = \frac{1}{128} \text{ to } 1)$$



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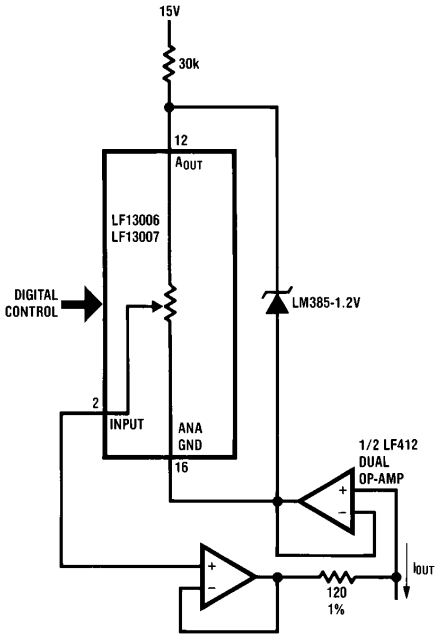
Typical Applications (Continued)

Programmable Current Source



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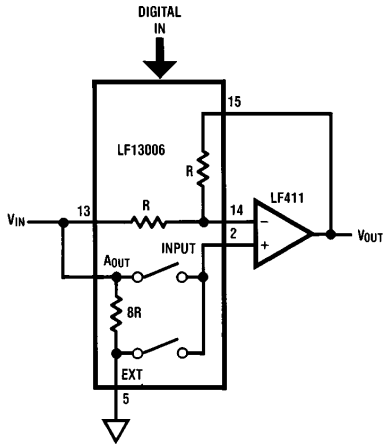
$$I_{OUT} = \frac{1.2V}{120\Omega}\left[\frac{1}{\text{gain set \#}}\right]$$

Switchable Gain of ±1



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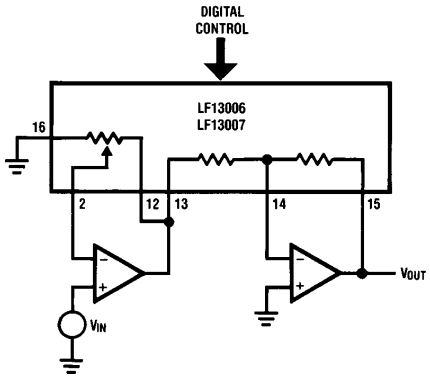
Note: Digital code = 000, $V_{OUT} = V_{IN}$;
Digital code = 001, $V_{OUT} = -V_{IN}$

Inverting Gains



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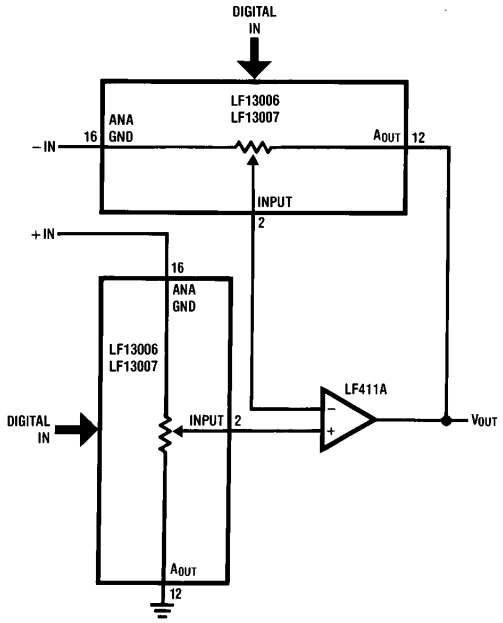
Inverting gain with high input impedance can be obtained with the LF13006, LF13007 by using the two on-board resistors and a dual op amp as shown.

Programmable Differential Amp



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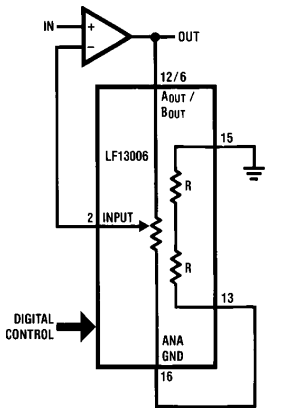
Note 1: Actual gain = set gain − 1 since LF13006s are in "inverting mode".
Note 2: Set gain must be same on both LF13006s.

Typical Applications (Continued)

Altered Gain Range



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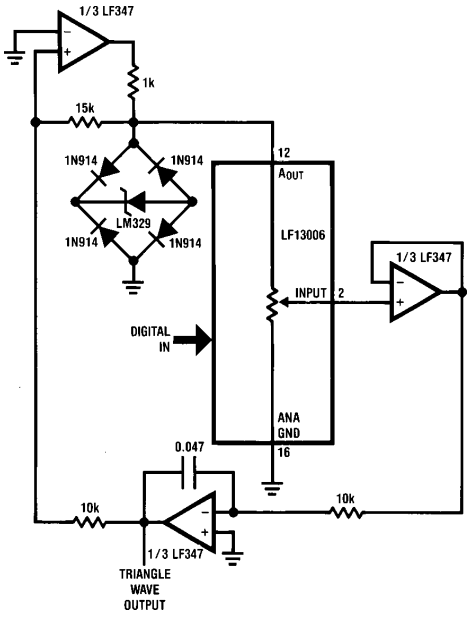
One Octave per Bit Function Generator



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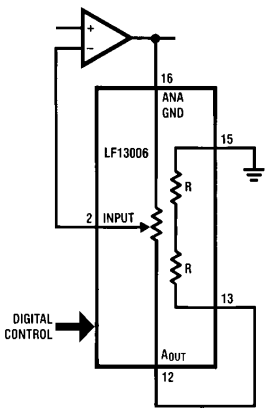
Variable Gains of Almost 1



TL/H/5114–16

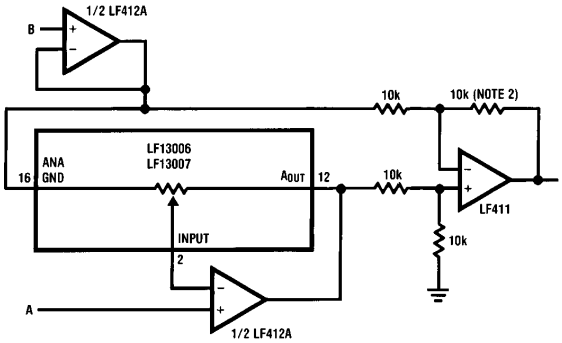
GAINS

A_{OUT}	B_{OUT}
1	1
1.8	1.2
3	2
4.5	3
6	4
7.2	4.8
8	5.33
8.47	5.65

GAINS

9
1.8
1.29
1.125
1.059
1.029
1.014
1.007

Programmable Instrumentation Amp



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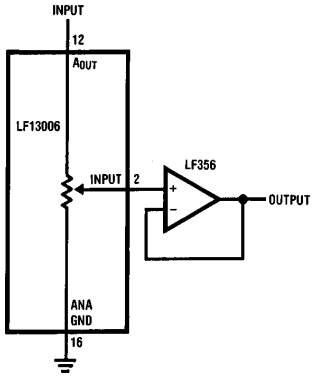
Attenuator (0 dB to −42 dB in 6 dB steps)



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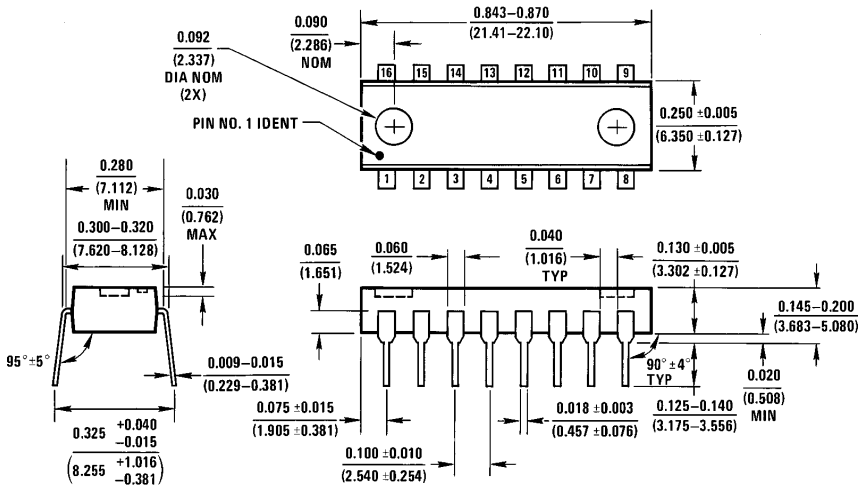
Note 1: $V_{OUT} = N\,(A - B)$, N = set gain.

Note 2: All 10k resistors 0.1% matched.

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number LF13006N or LF13007N
NS Package Number N16A

N16A (REV E)

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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