LOGIC DEVICES INCORPORATED

LF3304
Dual Line Buffer/FIFO

FEATURES

- 100 MHz Data Rate for Video and other High-Speed Applications
- One 24-bit, Two 12-bit, Three 8-bit Data Paths, or One Double Depth 12-bit
- Dual Modes: Line Buffer or FIFO
- User-Programmable FIFO Flags
- User-Resettable Read and Write Pointers
- Single 3.3 V Power Supply, 5 V Tolerant I/O
- 100-lead PQFP

DESCRIPTION

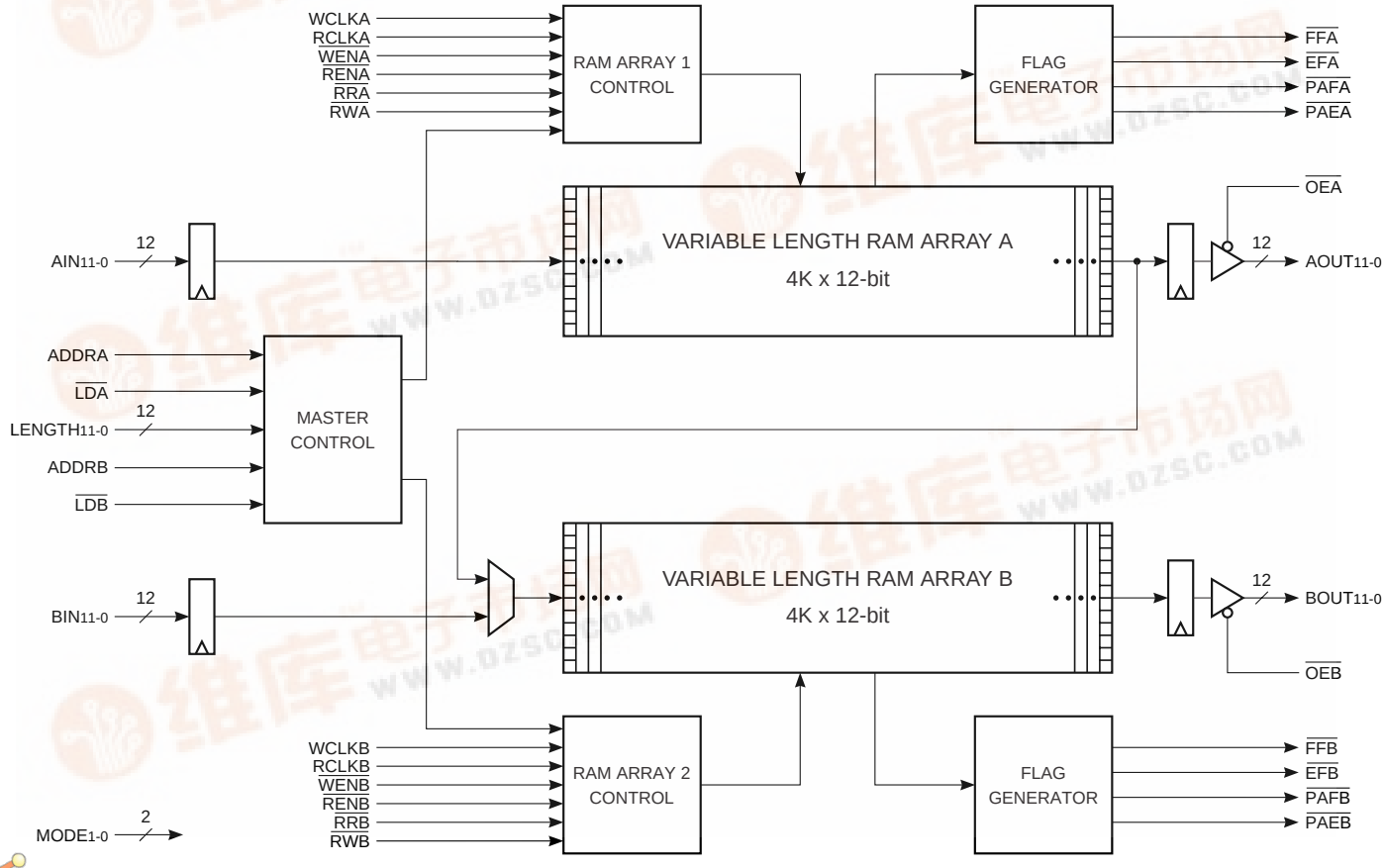
The **LF3304** is a dual line buffer / FIFO, designed to operate at HDTV rates. The LF3304 will operate in two distinct modes: Line Buffer and FIFO. In these modes the two memories can operate independently or with common control.

The LF3304 comprises two 12-bit 4K memories configurable in a variety of ways including: Two 12-bit 4K deep line buffers (independent lengths), Three 8-bit 4K deep line buffers (common lengths), One 12-bit 8K deep line buffer, or Two 12-bit 4K FIFOs (independent operation).

In FIFO mode, independent Read and Write Resets give the designer control over the internal pointers providing flexibility not commonly found in ordinary FIFOs.

The LF3304 operatates at a maximum data rate of 100 MHz and is available in a 100-lead PQFP package.

LF3304 Block Diagram



LINE BUFFER MODE SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clocks

WCLKA — Write Clock A

WCLKA and RCLKA must be tied together for RAM Array A to properly operate as a Line Buffer. The rising edge of xCLKA strobes all appropriate enabled registers.

RCLKA — Read Clock A

See WCLKA description.

WCLKB — Write Clock B

WCLKB and RCLKB must be tied together for RAM Array B to properly operate as a Line Buffer. The rising edge of xCLKB strobes all appropriate enabled registers.

RCLKB — Read Clock B

See WCLKB description.

Inputs

AIN11-0 — Data Input A

AIN11-0 is the 12-bit registered data input port.

BIN11-0 — Data Input B

BIN11-0 is the 12-bit registered data input port.

LENGTH11-0 — Line Buffer Length

The 12-bit value is used to specify the length of each of the RAM Arrays. An integer value ranging from 0 to 4095 is used to select a delay ranging from 2 to 4097 clock cycles. The value placed on LENGTH11-0 is equal to the desired delay minus 8. To set the length of RAM Array A the data presented on LENGTH11-0 is loaded into the device on the active edge of WCLKA in conjunction with $\overline{\text{LDA}}$ being driven LOW. To set the length of RAM Array B the data presented on LENGTH11-0 is loaded into the device on the active edge of WCLKB in conjunction with $\overline{\text{LDB}}$ being driven LOW. If an equal length is desired for both RAM Arrays, the data presented on LENGTH11-0 is loaded into the device on the active edge of WCLK (WCLKA and WCLKB tied together) in conjuction with $\overline{\text{LDx}}$ ($\overline{\text{LDA}}$ and $\overline{\text{LDB}}$ tied together) being driven LOW.

MODE1-0 — Mode Select

The mode select inputs determine the operating mode of the LF3304 (Table 1) for data being input on the next clock cycle. When switching between modes, the internal pipeline latencies of the device must be observed. After switching operating modes, either the user must allow enough clock cycles to pass to flush the internal RAM Array or $\overline{\text{RWx}}$ and $\overline{\text{RRx}}$ must be driven LOW together before valid data will appear on the outputs.

Controls

$\overline{\text{LDA}}$ — RAM Array A Load

When $\overline{\text{LDA}}$ is LOW, data on LENGTH11-0 is latched in the length register on the rising edge of xCLKA.

$\overline{\text{LDB}}$ — RAM Array B Load

When $\overline{\text{LDB}}$ is LOW, data on LENGTH11-0 is latched in the length register on the rising edge of xCLKB.

$\overline{\text{WENA}}$ — Write Enable A

Driving $\overline{\text{WENA}}$ LOW places the device in programmable delay mode and driving $\overline{\text{WENA}}$ HIGH places RAM Array A in recirculate mode (programmable circular buffer). When in recirculate mode, the write pointer position remains fixed while data on AIN11-0 is ignored. When switching back from recirculate mode to delay mode, $\overline{\text{RWA}}$ and $\overline{\text{RRA}}$ should be brought LOW to properly reset the Write and Read pointers.

TABLE 1. DEVICE CONFIGURATION

MODE1-0		Mode Select
0	0	Dual Line Buffer
0	1	Cascaded Line Buffer
1	0	Dual FIFO
1	1	Reserved

$\overline{\text{RENA}}$ — Read Enable B

In Line Buffer mode, $\overline{\text{RENA}}$ must be kept LOW.

$\overline{\text{WENB}}$ — Write Enable B

Driving $\overline{\text{WENB}}$ LOW places the device in programmable delay mode and driving $\overline{\text{WENB}}$ HIGH places RAM Array B in recirculate mode (programmable circular buffer). When in recirculate mode, the write pointer position remains fixed while data on BIN11-0 is ignored. When switching back from recirculate mode to delay mode, $\overline{\text{RWB}}$ and $\overline{\text{RRB}}$ should be brought LOW to properly reset the Write and Read pointers.

$\overline{\text{RENB}}$ — Read Enable B

In Line Buffer mode, $\overline{\text{RENB}}$ must be kept LOW.

$\overline{\text{RWA}}$ — Reset Write A

The write address pointer is reset to the first physical location when $\overline{\text{RWA}}$ is set LOW. After power up, the LF3304 requires a Reset Write for initialization because the write address pointer is not defined at that time.

$\overline{\text{RRA}}$ — Reset Read A

The read address pointer is reset to the first physical location when $\overline{\text{RRA}}$ is set LOW. After power up, the LF3304 requires a Reset Read for initialization because the read address pointer is not defined at that time.

$\overline{RWB}$ — Reset Write B

See $\overline{RWA}$ Description.

$\overline{RRB}$ — Reset Read B

See $\overline{RRA}$ description.

$\overline{OEA}$ — Output Enable A

When $\overline{OEA}$ is LOW, AOUT11-0 is enabled for output. When $\overline{OEA}$ is HIGH, AOUT11-0 is placed in a high-impedence state.

$\overline{OEB}$ — Output Enable B

When $\overline{OEB}$ is LOW, BOUT11-0 is enabled for output. When $\overline{OEB}$ is HIGH, BOUT11-0 is placed in a high-impedence state.

Outputs

AOUT11-0 — Data Output A

AOUT11-0 is the 12-bit registered data output port.

BOUT11-0 — Data Output B

BOUT11-0 is the 12-bit registered data output port.

FIFO MODE SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clocks

WCLKA — Write Clock A

Data present on AIN11-0 is written into the LF3304 on the rising edge of WCLKA when the device is configured for writing.

RCLKA — Read Clock A

Data is read from the LF3304 and presented on the output port (AOUT11-0) after **t**D has elapsed from the rising edge of RCLKA when the device is configured for reading and the output port is enabled. WCLKA and RCLKA can be tied together and driven by the same external clock or they may be controlled by separate external clocks.

WCLKB — Write Clock B

Data present on BIN11-0 is written into the LF3304 on the rising edge of WCLKB when the device is configured for writing.

RCLKB — Read Clock B

Data is read from the LF3304 and presented on the output port (BOUT11-0) after **t**D has elapsed from the rising edge of RCLKB when the device is configured for reading and the output port is enabled. WCLKB and RCLKB can be tied together and driven by the same external clock or they may be controlled by separate external clocks.

Inputs

AIN11-0 — Data Input A

AIN11-0 is the 12-bit registered data input port.

BIN11-0 — Data Input B

BIN11-0 is the 12-bit registered data input port.

ADDRA — Address A

If $\overline{LDA}$ is LOW, on the rising edge of WCLKA data present on AIN11-0 is written into the $\overline{PAFA}$ or $\overline{PAEA}$ register depending on ADDRA (see Table 2). The LSB, AIN0, corresponds to the LSB of $\overline{PAFA}$ and $\overline{PAEA}$ registers. The MSB, AIN11, corresponds to the MSB of $\overline{PAFA}$ and $\overline{PAEA}$ registers.

ADDRB — Address B

If $\overline{LDB}$ is LOW, on the rising edge of WCLKB data present on BIN11-0 is written into the $\overline{PAFB}$ or $\overline{PAEB}$ register depending on ADDRB (see Table 2). The LSB, BIN0, corresponds to the LSB of $\overline{PAFB}$ and $\overline{PAEB}$ registers. The MSB, BIN11, corresponds to the MSB of $\overline{PAFB}$ and $\overline{PAEB}$ registers.

MODE1-0 — Mode Select

The mode select inputs determine the operating mode of the LF3304 (Table 1) for data being input on the next clock cycle. When switching between modes, the internal pipeline latencies of the device must be observed. After switching operating modes, either the user must allow enough clock cycles to pass to flush the internal RAM Array or $\overline{RWx}$ and $\overline{RRx}$ must be driven LOW together before valid data will appear on the outputs.

LENGTH — Non-Flag Pins

In FIFO Mode, the unused LENGTH pins (LENGTH11, LENGTH10, LENGTH5, LENGTH4) must be tied LOW.

Controls

$\overline{LDA}$ — RAM Array A Load

When $\overline{LDA}$ is LOW, data on AIN11-0 is latched in the LF3304 on the rising edge of WCLKA.

TABLE 2. LOADING PROGRAMMABLE FLAG REGISTERS

ADDRA	ADDRB	LDA	LDB	WCLKA	WCLKB	Operation
0	x	0	x	↑	x	PAEA Register
1	x	0	x	↑	x	PAFA Register
x	0	x	0	x	↑	PAEB Register
x	1	x	0	x	↑	PAFB Register

$\overline{LDB}$ — RAM Array B Load

When $\overline{LDB}$ is LOW, data on BIN11-0 is latched in the LF3304 on the rising edge of WCLKB.

$\overline{WENA}$ — Write Enable A

If $\overline{WENA}$ is LOW, data on AIN11-0 is written to the device on the rising edge of WCLKA. When RAM Array A is full, $\overline{WENA}$ is ignored.

$\overline{RENA}$ — Read Enable A

If $\overline{RENA}$ is LOW, data from RAM Array A is read and presented on AOUT11-0 after t_D has elapsed from the rising edge of RCLKA if the output port is enabled. If $\overline{RENA}$ goes HIGH, the last value loaded in the RAM Array A output register will remain unchanged. When RAM Array A is empty, $\overline{RENA}$ is ignored.

$\overline{WENB}$ — Write Enable B

If $\overline{WENB}$ is LOW, data on BIN11-0 is written to the device on the rising edgle of WCLKB. When RAM Array B is full, $\overline{WENB}$ is ignored.

$\overline{RENB}$ — Read Enable B

If $\overline{RENB}$ is LOW, data from RAM Array B is read and presented on BOUT11-0 after tD has elapsed from the rising edge of RCLKB if the output port is enabled. If $\overline{RENB}$ goes HIGH, the last value loaded in the RAM Array B output register will remain unchanged. When RAM Array B is empty, $\overline{RENB}$ is ignored.

$\overline{RWA}$ — Reset Write A

The write address pointer is reset to the first physical location when $\overline{RWA}$ is set LOW. After power up, the LF3304 requires a Reset Write for initialization because the write address pointer is not defined at that time.

$\overline{RRA}$ — Reset Read A

The read address pointer is reset to the first physical location when $\overline{RRA}$ is set LOW. After power up, the LF3304 requires a Reset Read for initialization because the read address pointer is not defined at that time.

$\overline{RWB}$ — Reset Write B

See $\overline{RWA}$ Description.

$\overline{RRB}$ — Reset Read B

See $\overline{RRA}$ description.

$\overline{OEA}$ — Output Enable A

When $\overline{OEA}$ is LOW, AOUT11-0 is enabled for output. When $\overline{OEA}$ is HIGH, AOUT11-0 is placed in a high-impedence state. The flag outputs are not affected by $\overline{OEA}$.

$\overline{OEB}$ — Output Enable B

When $\overline{OEB}$ is LOW, BOUT11-0 is enabled for output. When $\overline{OEB}$ is HIGH, BOUT11-0 is placed in a high-impedence state. The flag outputs are not affected by $\overline{OEB}$.

Outputs

AOUT11-0 — Data Output A

AOUT11-0 is the 12-bit registered data output port.

BOUT11-0 — Data Output B

BOUT11-0 is the 12-bit registered data output port.

$\overline{FFA}$ — Full Flag A

$\overline{FFA}$ goes LOW when RAM Array A is full of data. When $\overline{FFA}$ is LOW, RAM Array A can not be written to. The Full Flag is synchronized to the rising edge of WCLKA.

$\overline{EFA}$ — Empty Flag A

$\overline{EFA}$ goes LOW when the read pointer is equal to the write pointer, indicating that RAM Array A is empty. When $\overline{EFA}$ is LOW, read operations can not be performed. The Empty Flag is synchronized to the rising edge of RCLKA.

$\overline{FFB}$ — Full Flag B

$\overline{FFB}$ goes LOW when RAM Array B is full of data. When $\overline{FFB}$ is LOW, RAM Array B can not be written to. The Full Flag is synchronized to the rising edge of WCLKB.

$\overline{EFB}$ — Empty Flag B

$\overline{EFB}$ goes LOW when the read pointer is equal to the write pointer, indicating that RAM Array B is empty. When $\overline{EFB}$ is LOW, read operations can not be performed. The Empty Flag is synchronized to the rising edge of RCLKB.

$\overline{PAFA}$ — Programmable Almost-Full Flag A

$\overline{PAFA}$ goes LOW when the write pointer is (Full – N) locations ahead of the read pointer. N is the value stored in the $\overline{PAFA}$ register and has no default value. $\overline{PAFA}$ is synchronized to the rising edge of WCLKA.

$\overline{PAEA}$ — Programmable Almost-Empty Flag A

$\overline{PAEA}$ goes HIGH when the write pointer is (N + 1) location ahead of the read pointer. N is the value stored in the $\overline{PAEA}$ register and has no default value. $\overline{PAEA}$ is synchronized to the rising edge of RCLKA.

$\overline{PAFB}$ — Programmable Almost-Full Flag B

$\overline{PAFB}$ goes LOW when the write pointer is (Full – N) locations ahead of the read pointer. N is the value stored in the $\overline{PAFB}$ register and has no default value. $\overline{PAFB}$ is synchronized to the rising edge of WCLKB.

$\overline{PAEB}$ — Programmable Almost-Empty Flag B

$\overline{PAEB}$ goes HIGH when the write pointer is (N + 1) location ahead of the read pointer. N is the value stored in the $\overline{PAEB}$ register and has no default value. $\overline{PAEB}$ is synchronized to the rising edge of RCLKB.

FIFO MODE OPERATION

Initialization

Upon power-up, the LF3304 requires the initialization of the internal read and write address pointers. This initialization sequence can be done by either a Flag Enable Reset or a Flag Disable Reset.

A Flag Enable Reset will force the FIFO to operate in a 'Flag Enabled' mode. In this mode, writing will be disabled when $\overline{FFx}$ is LOW and reading is disabled when $\overline{EFx}$ is LOW. Any 'write beyond full' event or 'read beyond empty' event will be disabled. Note: in an 'empty' state, the last data word read from the FIFO is held on the output bus until the next valid read cycle.

A Flag Disable Reset will force the FIFO to operate in a 'Flag Disabled' mode. In this mode, the user is allowed to write over previously unread data and read out previously read data. Consequently, any enabled write or read is valid thus allowing the write and read pointers to 'wrap-around'. Note: due to the nature of this mode, the flag status should be disregarded. For example, as the 4096th data word is written into the FIFO, assuming that no preceding read cycles have occured, $\overline{FFx}$ will be driven LOW thus indicating a 'full'state. While the FIFO is still in this 'full' state, the next enabled write will access address 000H, thus writing over data that has not yet been read out.

Flag Enable Reset

A Flag Enable Reset resets the read and write pointers and enables the flags to control the reading and writing of data according to the Full Flag and Empty Flag conditions. A Flag Enable Reset occurs when the following conditions are met:

1. $\overline{RWA}$ / $\overline{RWB}$ must be LOW for at least one WCLKA / WCLKB cycle.
2. $\overline{RRA}$ / $\overline{RRB}$ must be LOW for at least one RCLKA / RCLKB cycle.
3. $\overline{WENx}$ and $\overline{RENx}$ must be HIGH during the above two conditions plus one addition write or read cycle (which ever is longer).

The Flag Enable Reset condition can be disabled if one of the two Flag Disable Reset conditions are applied.

Flag Disable Reset

A Flag Disable Reset resets the read and write pointers and disables the flags from controlling the reading and writing of data. A Flag Disable Reset occurs when the following conditions are met:

1. $\overline{RWA}$ / $\overline{RWB}$ must be LOW for at least one WCLKA / WCLKB cycle while $\overline{WENx}$ is LOW.
2. $\overline{RRA}$ / $\overline{RRB}$ must be LOW for at least one RCLKA / RCLKB cycle while $\overline{RENx}$ is LOW.

Configuration of Programmable Flags

In order to load a FIFO A Programmable Flag Register, a rising edge of WCLKA, while $\overline{WENA}$ is LOW, latches AIN11-0 into either the $\overline{PAFA}$ or $\overline{PAEA}$ Register - depending on the states of ADDRA and $\overline{LDA}$ (See Table 2).

In order to load a FIFO B Programmable Flag Register, a rising edge of WCLKB, while $\overline{WENB}$ is LOW, latches BIN11-0 into either the $\overline{PAFB}$ or $\overline{PAEB}$ Register - depending on the states of ADDRB and $\overline{LDB}$ (See Table 2). See the Figure labeled "Programmable Flag Load Timing."

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +4.5 V
Input signal with respect to ground ..... –0.5 V to 5.5 V
Signal applied to high impedance output ..... –0.5 V to 5.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	3.00 V ≤ V_{CC} ≤ 3.60 V
Active Operation, Military	–55°C to +125°C	3.00 V ≤ V_{CC} ≤ 3.60 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

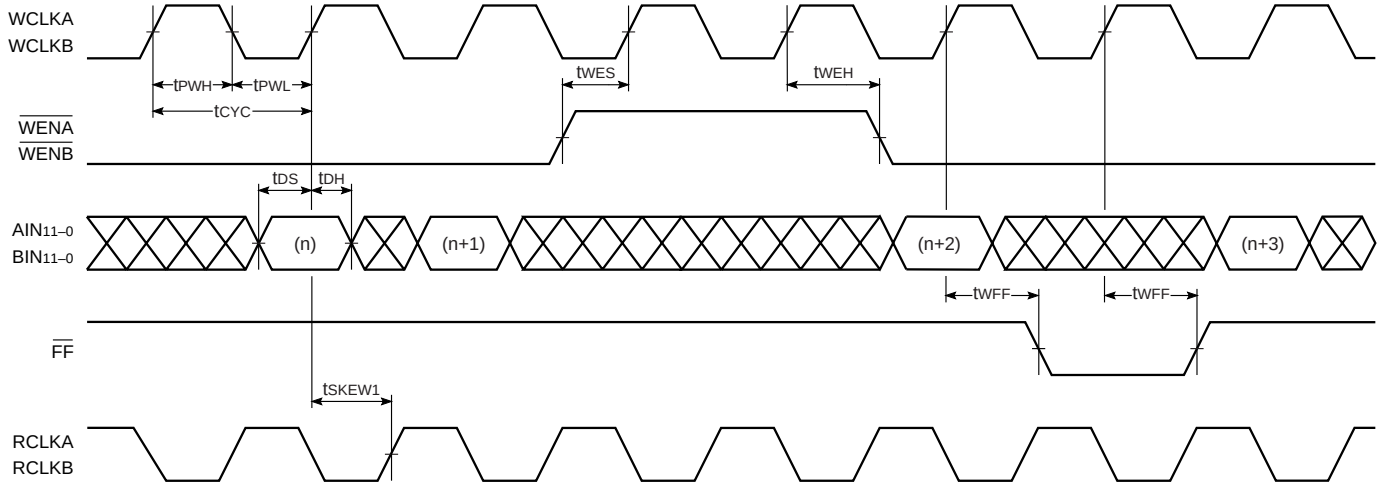
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		5.5	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			50	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			2	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

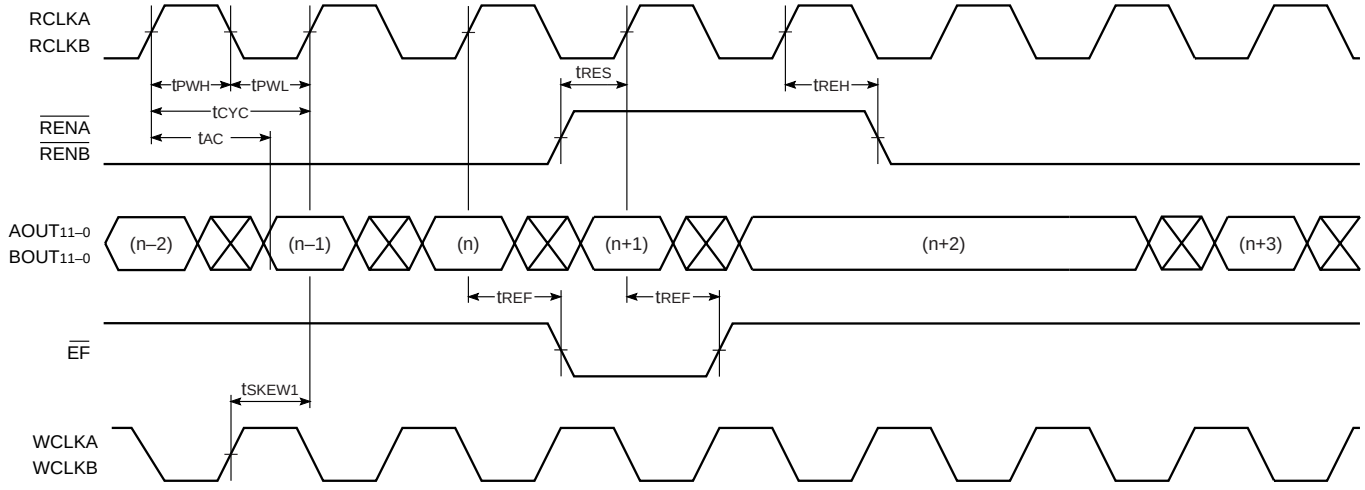
		LF3304–					
		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	15		12		10	
t_{PWH}	Clock Pulse Width High	5		4		3	
t_{PWL}	Clock Pulse Width Low	5		4		3	
t_{DS}	Data Setup Time	6		5		4	
t_{DH}	Data Hold Time	0		0		0	
t_{WES}	Write Enable Setup Time	6		5		4	
t_{WEH}	Write Enable Hold Time	0		0		0	
t_{RES}	Read Enable Setup Time	6		5		4	
t_{REH}	Read Enable Hold Time	0		0		0	
t_{LDS}	Load Setup Time	6		5		4	
t_{LDH}	Load Hold Time	0		0		0	
t_{RS}	Read/Write Reset Setup Time	6		5		4	
t_{RH}	Read/Write Reset Hold Time	0		0		0	
t_{AC}	Access Time		8		7		6
t_{WFF}	Write Clock to Full Flag		8		7		6
t_{REF}	Read Clock to Empty Flag		8		7		6
t_{PAF}	Write Clock to Programmable Almost-Full Flag		8		7		6
t_{PAE}	Read Clock to Programmable Almost-Empty Flag		8		7		6
t_{OHZ}	Output Enable to Output in Low Impedance		8		7		6
t_{OLZ}	Output Enable to Output in High Impedance		8		7		6
t_{SKEW1}	Skew Time Between Read and Write Clocks for $\overline{EF}$ and $\overline{FF}$		6		5		4
t_{SKEW2}	Skew Time Between Read and Write Clocks for $\overline{PAEx}$ and $\overline{PAFx}$		6		5		4

Write Cycle Timing



RWA = RWB = HIGH

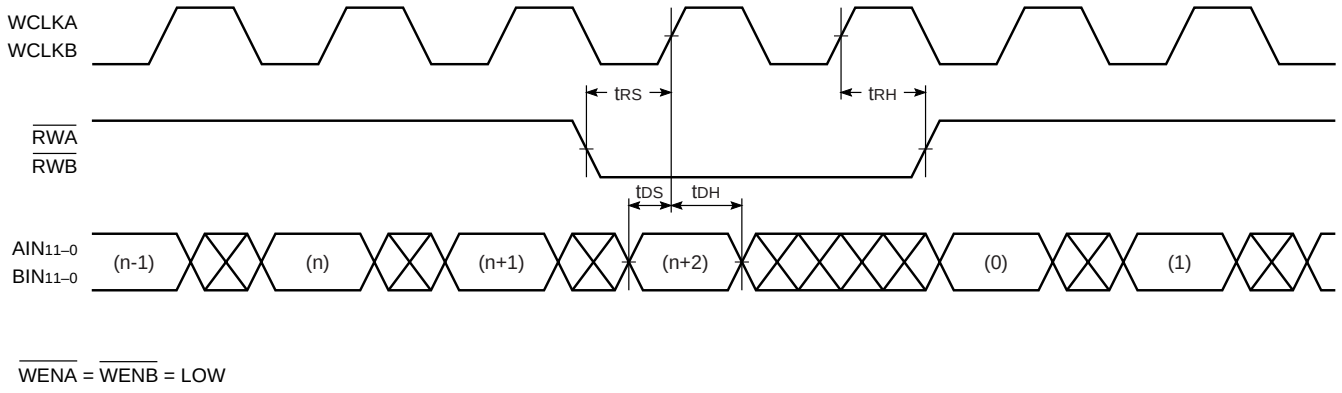
Read Cycle Timing



RRA = RRB = HIGH

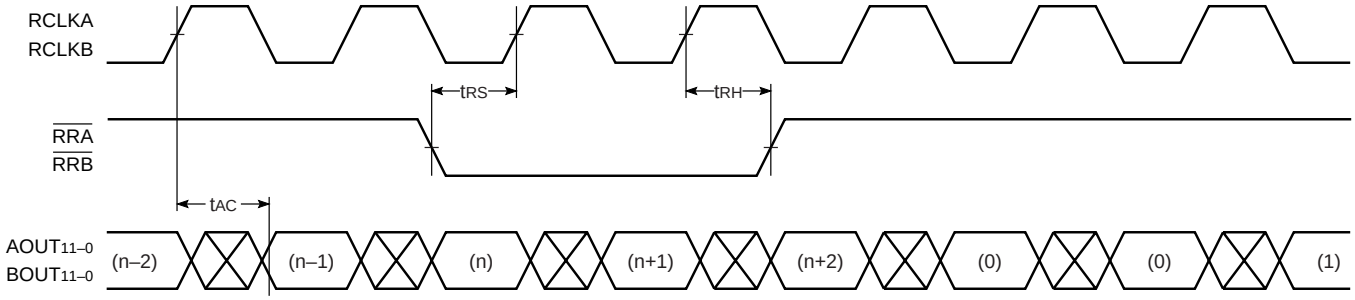
OEA = OEB = LOW

WRITE RESET TIMING



$\overline{WENA}$ = $\overline{WENB}$ = LOW

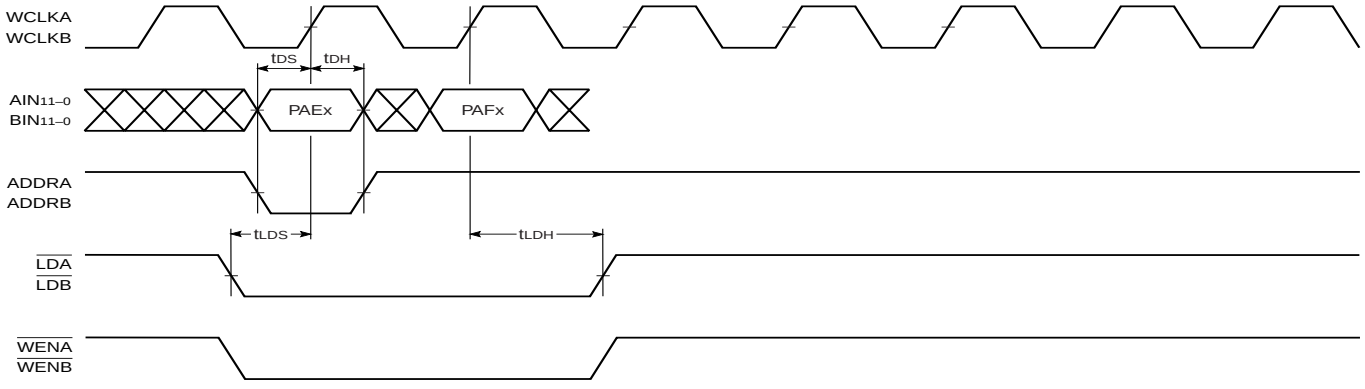
READ RESET TIMING



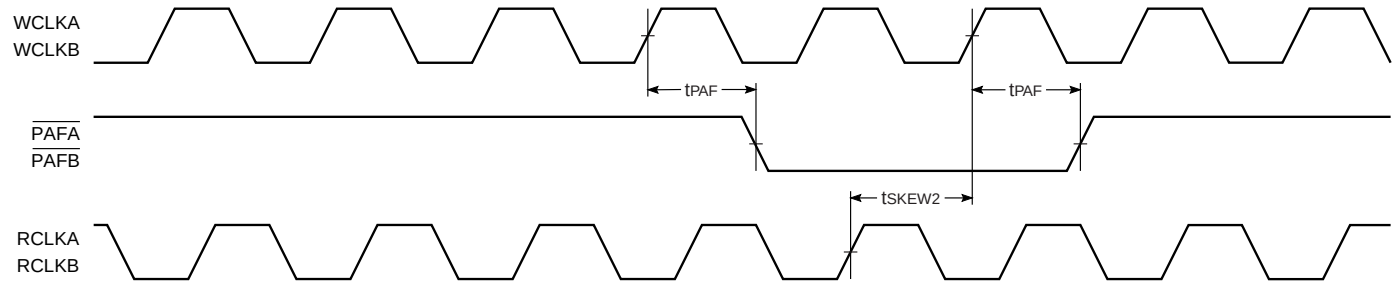
$\overline{RENA}$ = $\overline{RENB}$ = LOW

$\overline{OEA}$ = $\overline{OEB}$ = LOW

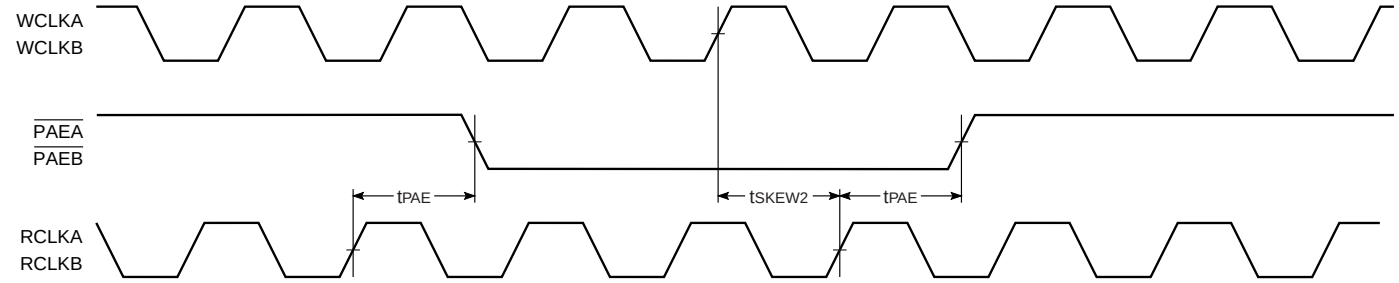
PROGRAMMABLE FLAG LOAD TIMING



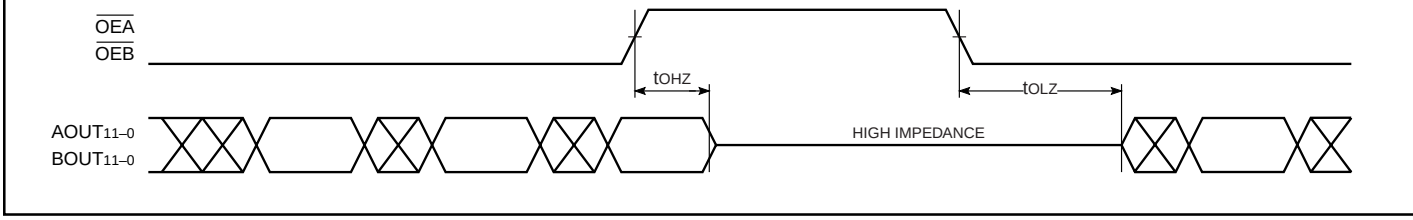
Programmable Almost Full Flag



Programmable Almost Empty Flag



Output Enable and Disable



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. The device can withstand indefinite operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with outputs changing every cycle and no load, at a 40 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except **t**DIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and **V**CC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the **t**ENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the **t**DIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

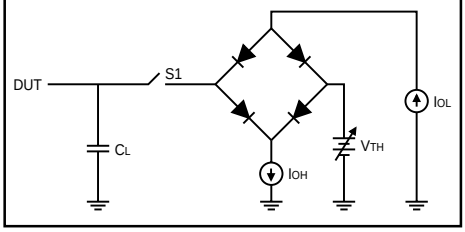
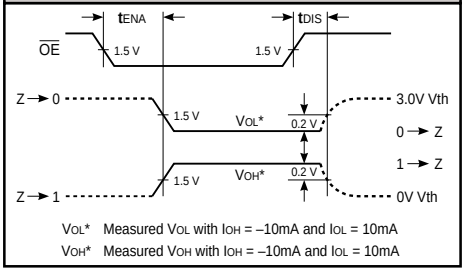
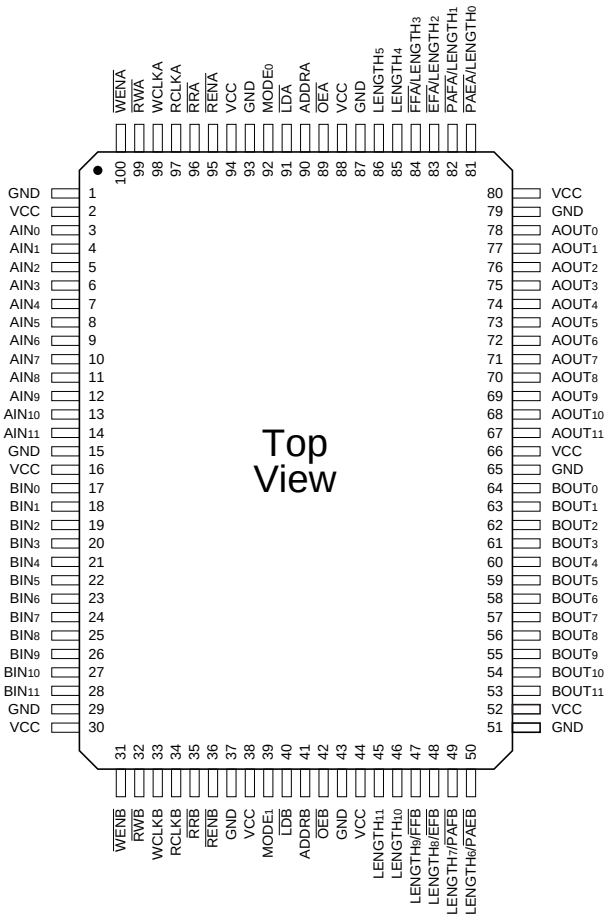


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
15 ns	LF3304QC15
12 ns	LF3304QC12
10 ns	LF3304QC10