National Semiconductor

LH0038/LH0038C True Instrumentation Amplifier

General Description

The LH0038/LH0038C is a precision true instrumentation amplifier (TIA) capable of amplifying very low level signals, such as thermocouple and low impedance strain gauge outputs. Precision thin film gain setting resistors are included in the package to allow the user to set the closed-loop gain from 100 to 2000. Since the resistors are of a homogeneous single chip construction, they track almost perfectly so that temperature variations of closed loop gain are virtually eliminated.

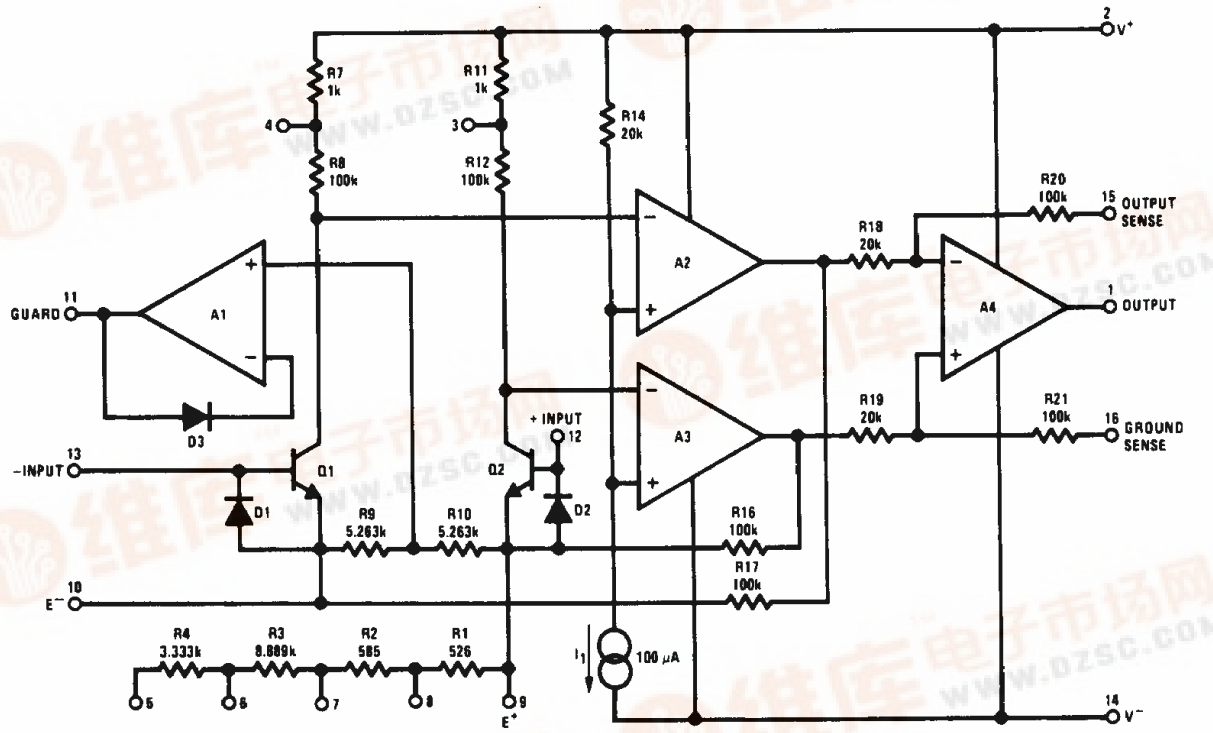
LH0038 exhibits excellent CMRR, PSRR, gain linearity, as well as extremely low input offset voltage, offset voltage drift and input noise voltage.

The devices are provided in a hermetically sealed 16-lead DIP. The LH0038 is guaranteed from −55°C to +125°C; whereas the LH0038C is guaranteed from −25°C to +85°C.

Features

- Ultra-low input offset voltage 25 μV typ., 100 μV max
- Ultra-low input offset drift 0.25 μV/°C max
- Ultra-low input noise 0.2 μVp-p
- Pin strap gain options 100, 200, 400, 500, 1k, 2k
- Excellent PSRR and CMRR 120 dB

Simplified Schematic Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±1V
Input Voltage	$\pm V_S$
Power Dissipation (Note 3)	500 mW
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0038	−55°C to +125°C
LH0038C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		LH0038			LH0038C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IOS}	Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$	$T_A = 25°C$		25	100		30	150	µV
						125			220	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Tempco				0.1	0.25		0.2	1.0	µV/°C
V_{OOS}	Output Offset Voltage		$T_A = 25°C$		3	10		5	25	mV
						15			30	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Tempco				25			25		µV/°C
I_B	Input Bias Current		$T_A = 25°C$		50	100		50	100	nA
						200			200	
I_{OS}	Input Offset Current		$T_A = 25°C$		2	5		7	10	
						8			15	
$\Delta I_B/\Delta T$	Input Bias Current Tempco				500			500		pA/°C
A_{VCL}	Closed Loop Gain	Gain Pins Jumpered								V/V
		None			100			100		
		6-10			200			200		
		6-9, 10-5			400			400		
		6-10, 5-9			500			500		
		7-10			1000			1000		
		8-10			2000			2000		
	Closed Loop Gain Error	$A_{VCL} = 100, 200$			0.1	0.3		0.1	0.4	%
		$A_{VCL} = 400, 500$			0.2	0.3		0.2	0.6	
		$A_{VCL} = 1000$			0.3	0.5		0.5	1.0	
		$A_{VCL} = 2000$			1.0	2.0		1.5	3.0	
	Gain Temperature Coefficient	$A_{VCL} = 1k$			7			7		ppm/°C
	Gain Nonlinearity	$100 \le A_{VCL} \le 2k$			1			1		ppm
V_{INCM}	Common-Mode Input Voltage Range			±10	±12		±10	±12		V
V_O	Output Voltage	$R_L \ge 10\ k\Omega$		±10	±12		±10	±12		
V_S	Supply Voltage Range			±5		±18	±5		±18	
	Guard Voltage Error	$-10V < V_{CM} < +10V$			±10	±100		±10	±100	mV
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_{VCL} = 100$	94	110		86	110		dB
			$A_{VCL} = 1000$	114	120		106	110		
PSRR	Power Supply Rejection Ratio	$\pm 5V \le \Delta V_S \le \pm 15V$	$A_{VCL} = 100$	94	110		94	110		
			$A_{VCL} = 1000$	110	120		100	110		

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DC Electrical Characteristics (Note 2) (Continued)

Symbol	Parameter	Conditions	LH0038			LH0038C			Units
			Min	Typ	Max	Min	Typ	Max	
I_{OSC}	Output Short Circuit Current	$T_A = 25°C$	±2	±5	±10	±2	±5	±10	mA
I_S	Supply Current	$T_A = 25°C$		1.6	2.0		1.6	3.0	
R_{IN} DIFF	Input Resistance	$A_{VCL} = 1000, T_A = 25°C$		5			5		MΩ
R_{IN}^{CM}	Common-Mode Input Resistance			1			1		GΩ
R_{OUT}	Output Resistance			1			1		mΩ

AC Electrical Characteristics $V_S = \pm 15V, T_A = 25°C$

Symbol	Parameter	Comment	Conditions		Typ	Units
e_n	Equivalent Input Noise Voltage	*Figure 1*	$R_S = 0, f = 0.1$ to 10Hz		0.2	μVp-p
$\overline{e_n}$	Equivalent Input Spot Noise Voltage	*Figure 1*	$R_S = 100\Omega$	f = 10 Hz	6.5	nV/√Hz
				f = 100 Hz	6.0	
				f = 1 kHz	6.0	
				f = 10 kHz	6.0	
BW	Large Signal Bandwidth		$V_{OUT} = \pm 10V$		1.6	kHz
S_r	Slew Rate		$V_{OUT} = \pm 10V$		0.3	V/μs
t_s	Settling Time to 0.01%	*Figure 13*		20V Step	120	μs
				−10V Step	80	
				+10V Step	60	
t_r	Rise Time		ΔV_{OUT}	$A_{VCL} = 100$	6	μs
				$A_{VCL} = 1000$	13	
$\overline{i_n}$	Equivalent Input Spot Noise Current		$R_S = 100$ MΩ	f = 10 Hz	0.1	pA/√Hz

Note 1: The inputs are protected by diodes for overvoltage protection. Excessive currents will flow for differential voltages in excess of ±1V. Input current should be limited to less than 10 mA.

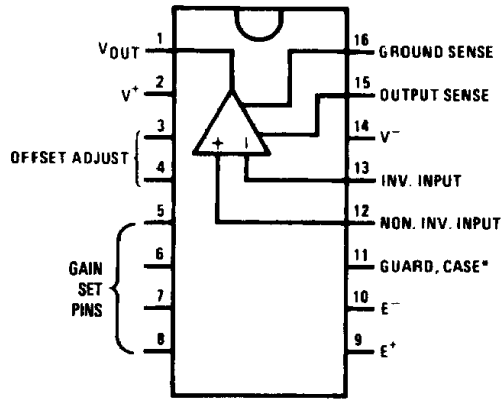
Note 2: Unless otherwise noted these specifications apply for $V_S = \pm 15.0V$, pin 15 connected to pin 1, pin 16 connected to ground, over the temperature range −55°C to +125°C for the LH0038 and −25°C to +85°C for LH0038C. $T_A = T_j$ unless otherwise specified.

Note 3: See Typical Performance Characteristics for Thermal Resistance Information.

Note 4: Refer to RETS0038D for LH0038D military specifications.

Connection Diagram

Dual-In-Line Package



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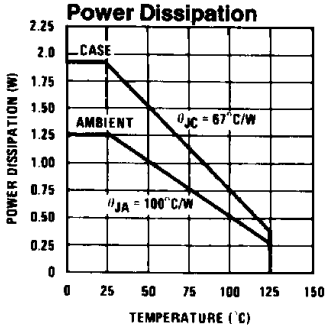
Top View

*Guard output is connected to the case.

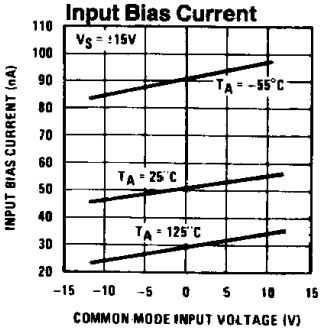
Order Number LH0038 or LH0038CD
See NS Package Number D16D

Typical Performance Characteristics

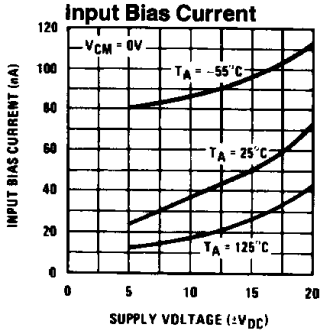
Power Dissipation



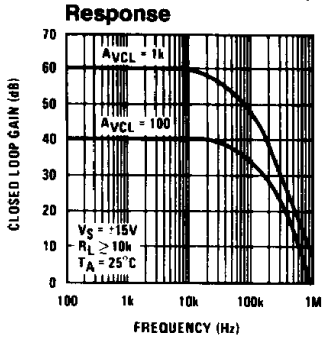
Input Bias Current



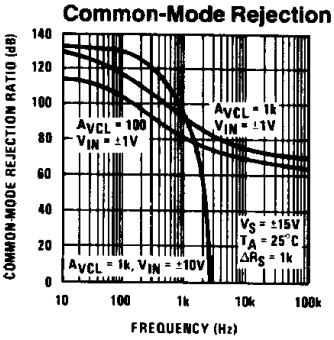
Input Bias Current



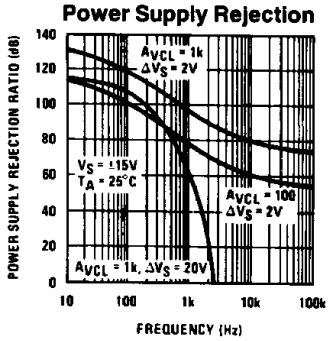
Closed Loop Frequency Response



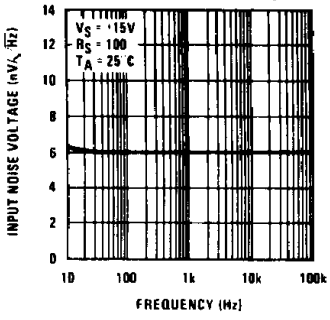
Common-Mode Rejection



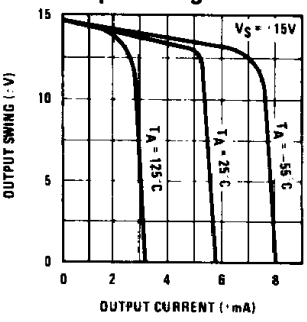
Power Supply Rejection



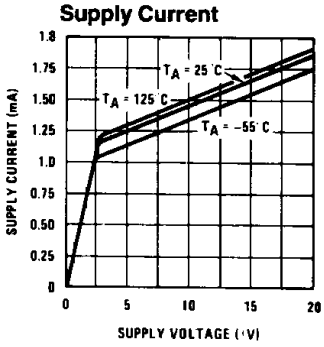
Input Noise Voltage (Includes Source Impedance)



Output Swing



Supply Current



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Wide Band Noise

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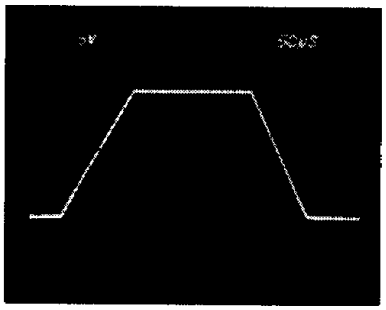
V_S = ±15V, R_S = 1 kΩ, A_V = 10k, DUT = 1k
Vertical sensitivity: 0.1 μV/CM
Horizontal sensitivity: 5 s/CM
Bandwidth: 0.1 Hz to 10 Hz

Pulse Response



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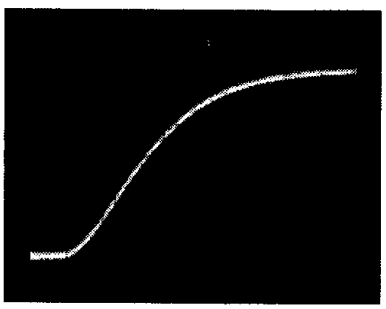
V_S = ±15V
R_L ≥ 10 kΩ
A_{VCL} = 1k

Rise Time



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V_S = ±15V
R_L ≥ 10kΩ
A_{VCL} = 1k

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Noise Test Circuit

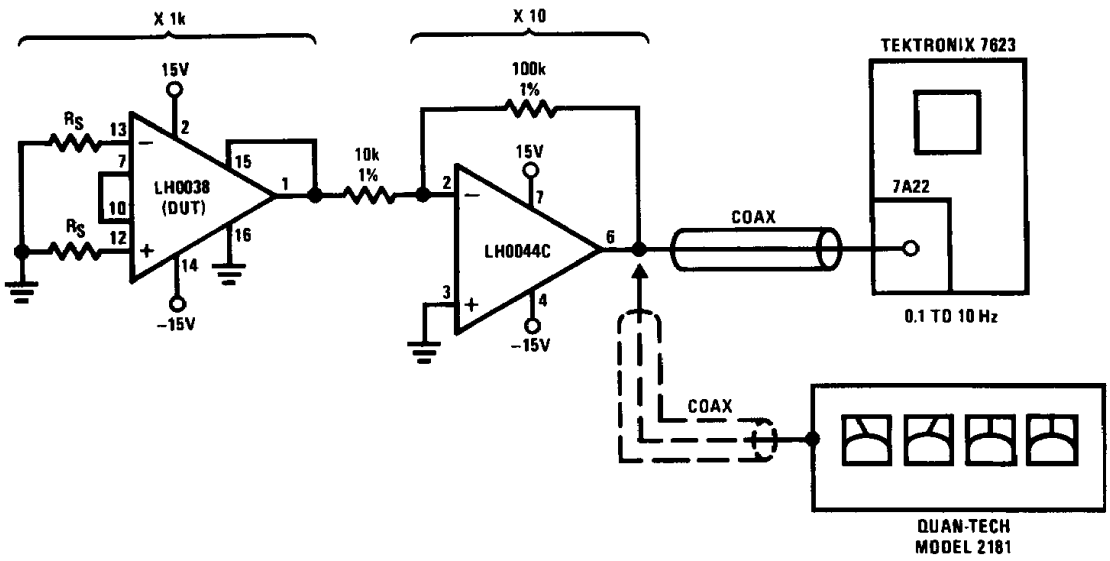

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FIGURE 1

Typical Application

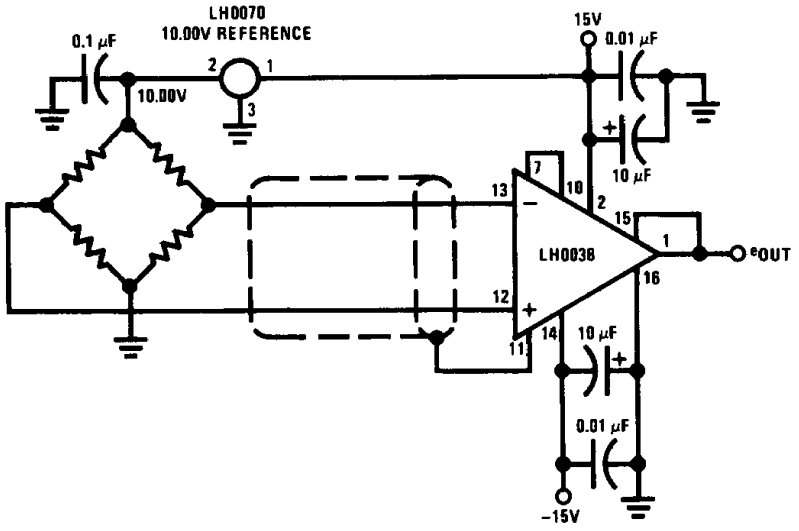

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FIGURE 2. X1000 Bridge Amplifier

Applications Information

THEORY OF OPERATION

The LH0038 is a 3-stage, true instrumentation amplifier composed of a well matched transistor differential pair, Q1 and Q2, a common-mode loop amplifier, A2 and A3, and a differential to single ended amplifier, A4. A simplified schematic is shown in *Figure 3.*

Current source, I_A, establishes a voltage across R14 of approximately 2V, which results in a 2V drop across R8 and R12. This constant voltage forces the first stage current to be 20 μA per side. The action of A2 and A3 is such that 20 μA is maintained constant despite the presence of common-mode signals. The differential outputs of A2 and A3 are applied to differential amplifier, A4, which converts the signal to a single-ended output and provides gain of 5. The total gain of the amplifier is, therefore, the fixed gain of 5 multiplied by the gain of the composite input stage.

Applications Information (Continued)

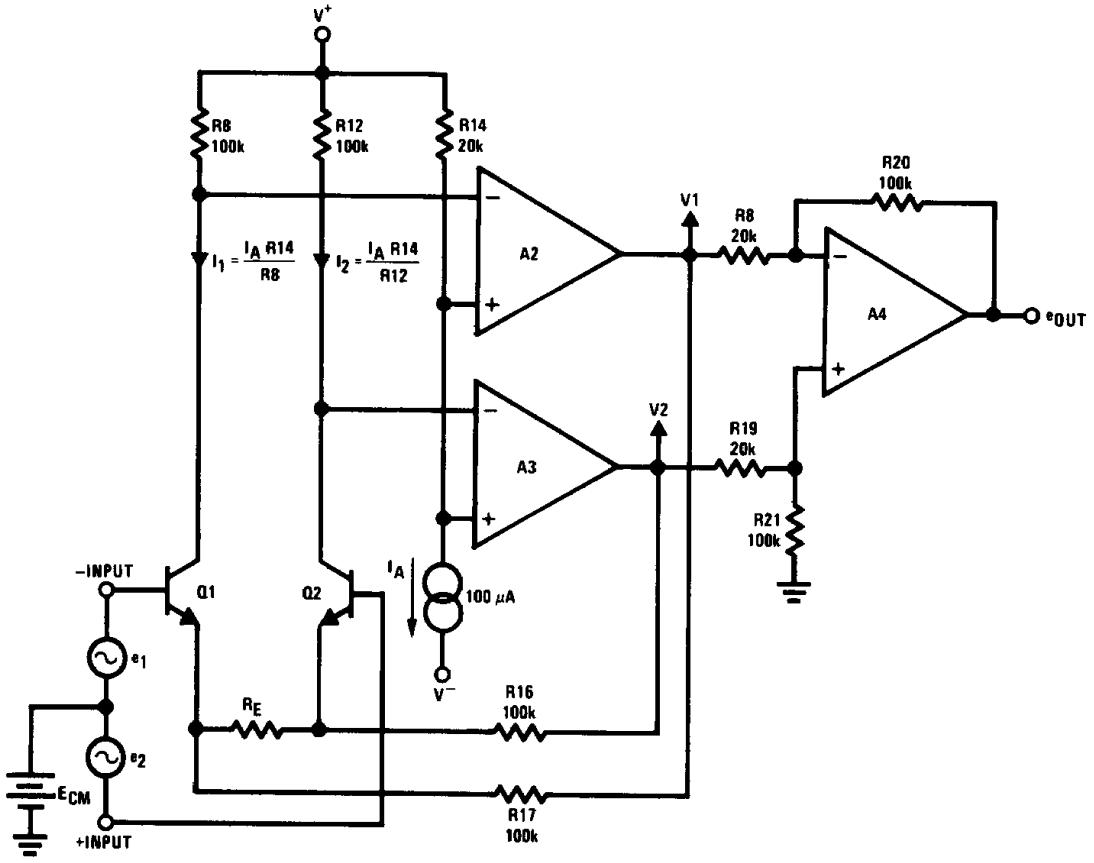

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FIGURE 3. LH0038 Simplified Schematic

The closed loop gain of the composite amplifier may be better understood by referring to *Figure 3*. The Q1–A2 loop may be viewed as differential amplifier with the inverting input at the base and non-inverting input at the emitter. Combining small signal AC and large signal DC analysis =

$$v1 = e1\left(\frac{R17 + R_E}{R_E}\right) - e2\left(\frac{R17}{R_E}\right) + E_{CM} - V_{BE1} - I_1R17 \quad (1)$$

By similar analysis:

$$v2 = e2\left(\frac{R16 + R_E}{R_E}\right) - e1\left(\frac{R16}{R_E}\right) + E_{CM} - V_{BE2} - I_2R16 \quad (2)$$

For $I_1 \equiv I_2$, $R17 \equiv R16$, $V_{BE1} \equiv V_{BE2}$, subtracting equation (1) from (2) results in:

$$v2 - v1 = (e2 - e1)\left(\frac{R16 + R_E}{R_E}\right) + (e2 - e1)\left(\frac{R16}{R_E}\right) \quad (3)$$

$$\frac{v2 - v1}{e2 - e1} = \frac{2\,R16}{R_E} + 1 \quad (4)$$

The differential input voltage (v2 − v1) is amplified by the closed loop gain of A4:

$$e_{OUT} = (A_{VCL4})(e2 - e1) \quad (5)$$

where:

$$A_{VCL4} = \frac{R20}{R8} = 5.00$$

$$\boxed{A_{VCL} = 5\left(\frac{2R16}{R_E} + 1\right)} \quad (6)$$

As an example, with all gain pins open, $R_E = 10.525\ k\Omega$, and;

$$A_{VCL} = 5\left(\frac{(2)\,(100k)}{R_E} + 1\right) = 100.0 \quad (7)$$

All other closed loop gain configurations place a precision resistor in parallel with $R_E(R9 + R10)$. For example, for a gain of 200, pin 6 is connected to pin 10 and the gain is predicted by:

$$A_{VCL} = 5.00\left[\frac{(2)\,(100k)}{(10.526) \parallel (10.000k)} + 1\right] = (5.00)\,(40) = 200 \quad (8)$$

CLOSED LOOP GAIN CONSIDERATIONS USING INTERNAL RESISTORS

Table 1 summarizes the primary gain configurations available with the LH0038. Obviously, other gains are possible. Using the internally supplied resistors has the advantage that R16, R17, and R_E all track thermally, minimizing the device's gain error as a function of temperature.

Gain adjustment by paralleling or series padding internally supplied resistors is generally discouraged since external resistors will generally not thermally track. It is recommended that the gain adjustment be done in a subsequent stage as shown in *Figure 4*.

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Applications Information (Continued)

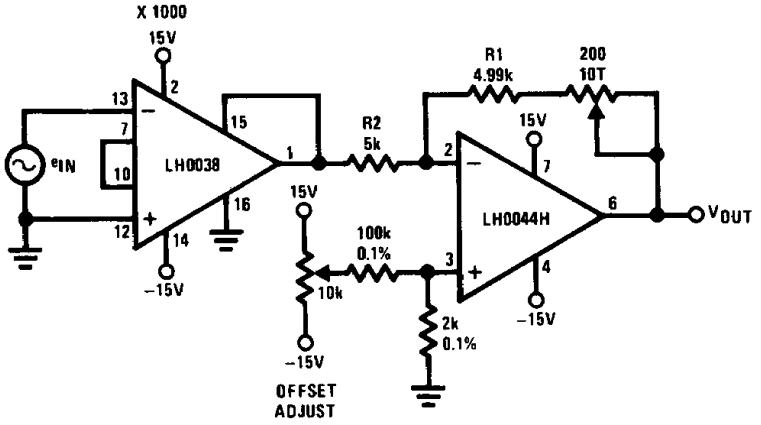

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FIGURE 4. Recommended Gain Adjust Circuit

TABLE I. LH0038 Internal Gain Configurations

Overall Gain	First Stage Gain	Pin Configuration	Effective R_E
100	20	All Gain Pins Open	10.5260 kΩ
200	40	Pin 6 to Pin 10	5.1281 kΩ
400	80	Pin 6 to Pin 9, Pin 10 to Pin 5	2.5316 kΩ
500	100	Pin 6 to Pin 10, Pin 9 to Pin 5	2.0202 kΩ
1000	200	Pin 7 to Pin 10	1.0050 kΩ
2000	400	Pin 8 to Pin 10	0.5013 kΩ

GUARD DRIVE

The LH0038 is provided with a guard drive output, which will always be at the input common-mode voltage. The guard drive amplifier is short-circuit proof and is capable of driving several thousand pF without danger of latch-up or oscillation.

The guard drive tied to a shielded input cable will greatly reduce noise pick-up, and also improve AC CMRR by maintaining the shield at the common-mode voltage. *Figure 5* illustrates the proper use of the guard drive. The guard drive output is also connected to the case to provide electrostatic shielding to the system.

REMOTE OUTPUT SENSE

The feedback network of the LH0038 may be closed directly at the load in order to eliminate errors due to lead resistance. Also, a unity gain buffer; e.g. LH0002, may be included within the feedback loop to increase output current capability as shown in *Figure 7*.

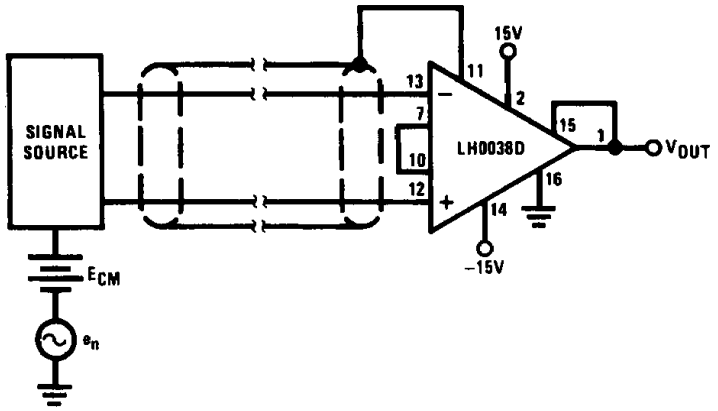

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FIGURE 5. Guard Drive Application

Applications Information (Continued)

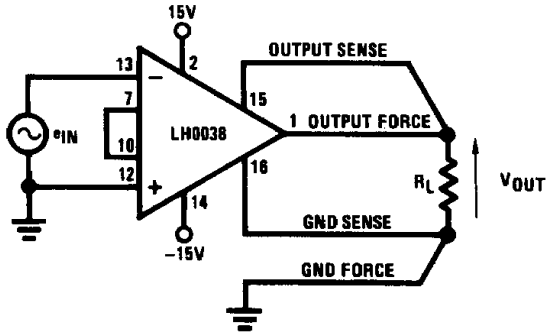

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FIGURE 6. Remote Sense Connection

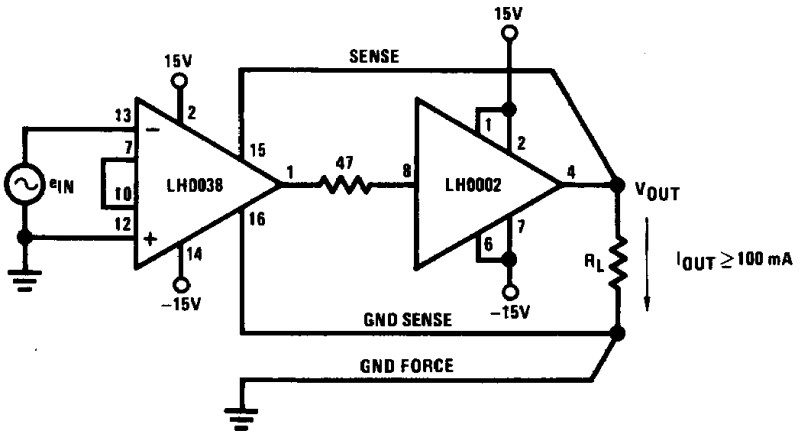

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FIGURE 7. Output Buffer Connection

OFFSET NULL

Offset of the LH0038 is trimmed by the factory to a very low value. The offset may be further trimmed using a 10 kΩ, 10 turn, 100 ppm/°C potentiometer as shown in *Figure 8*. However, a drift increase of 0.3 μV/°C will be caused for each 100 μV of offset adjusted. The recommended offset null is shown in *Figure 4* and is accomplished in the following stage.

BIAS CURRENT CONSIDERATIONS

The LH0038 exhibits bias current of approximately 50 nA per side, and requires a path to ground or supply. The practical limitation to the maximum resistance between the inputs and ground is dictated by negative common-mode range as shown in *Figure 9*. For example, for $V_{CM} = -10V$, $R_{CM} \leq 20\ M\Omega$.

The LH0038 input stage bias was optimized for minimum voltage noise so the input bias currents are higher than might otherwise be expected. Note, however, that the input currents are very well matched, resulting in an offset current value much lower than one might infer from the bias current. In order to take advantage of this low offset current, the source impedances at both inputs should be matched to minimize DC drift. Further, bias current is relatively constant with temperature (as opposed to an FET stage), so one can consider bias current compensation schemes such as shown in *Figure 10*. The danger with such techniques is that the offset current and noise contributed by the bias current compensator will dominate the system noise.

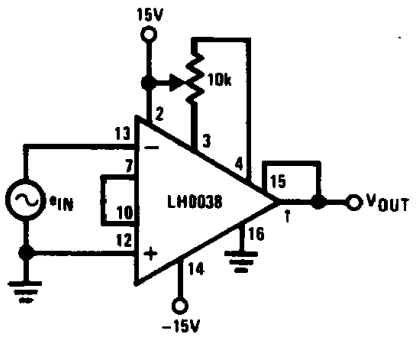

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FIGURE 8. Offset Adjust Circuit (See also *Figure 4*)

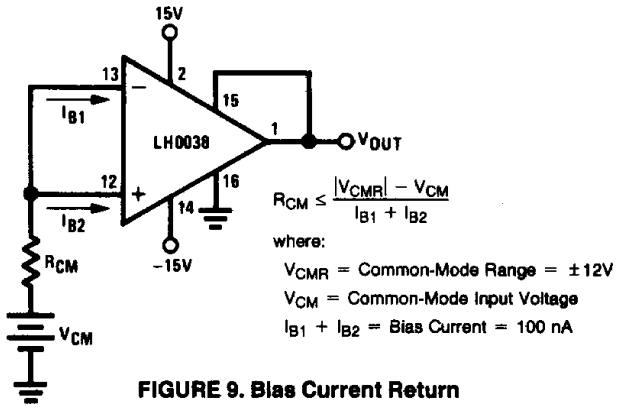

FIGURE 9. Bias Current Return

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Applications Information (Continued)

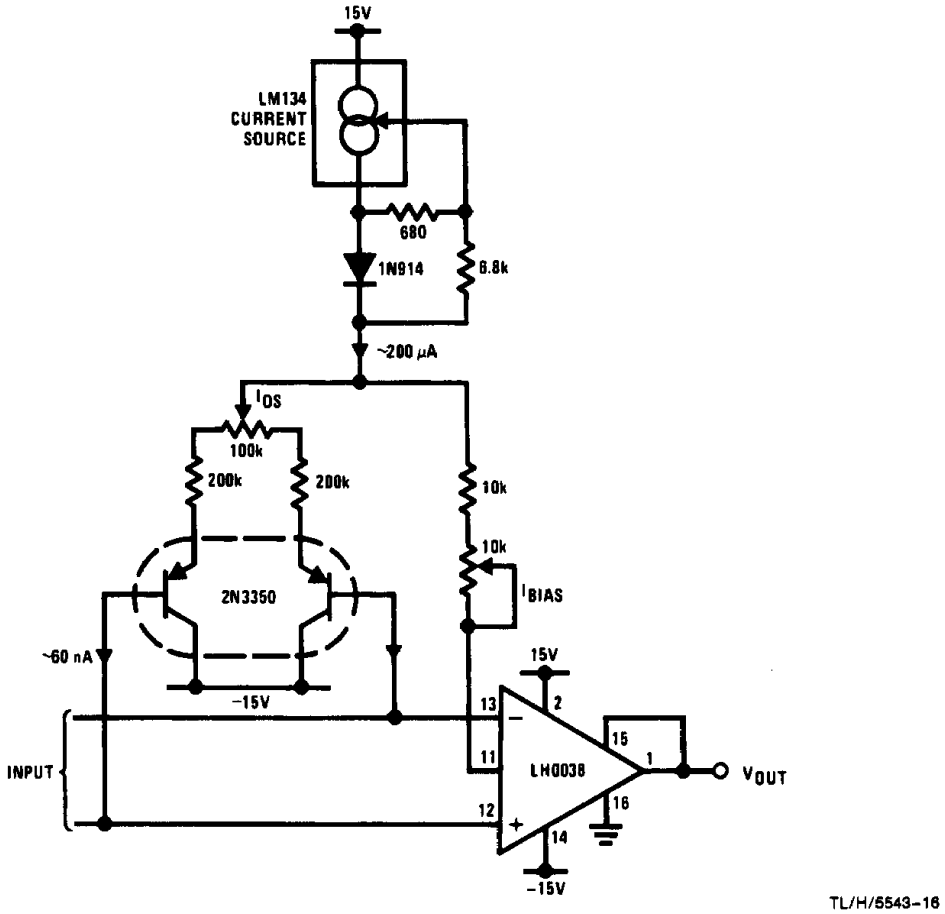

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FIGURE 10. Bias Current Compensation

SETTLING TIME

The LH0038 has been purposely over-compensated, and is therefore remarkably free from any undesirable transient response. Small signal settling time is governed by gain-bandwidth product; large signal settling time is dominated by slew rate.

Figure 11 shows an input voltage step of +10V to −10V applied, through a 1000 to 1 voltage divider, to the device configured for an inverting gain of 1000. The output of the device will therefore be equal to the negative of the input after the device is completely settled. By resistively subtracting the input before the divider from the device output, a pseudo summing node is generated. The voltage at this pseudo summing junction goes "off screen" on the photos, since in the first small time increment the input goes instantaneously to −10 mV and the output is still at +10V. About 130 μs after the input has gone negative, the output slews back in range and begins an exponential approach to the final value. *Figure 12* is the same set-up for a −10V to +10V input pulse. Note that there is no overshoot in either case. The test circuit is shown in *Figure 13.*

HIGH FREQUENCY CMRR

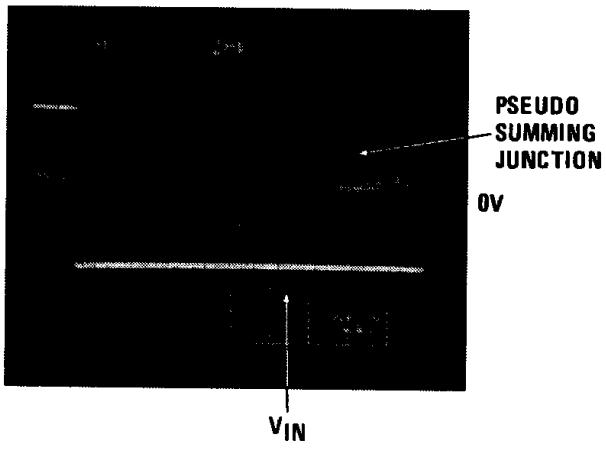
The LH0038 resistor ratios are carefully trimmed for optimum CMRR at DC through 60 Hz. Inevitably, this rejection will degrade at higher frequencies due to 2 separate effects: stray capacitance mismatch and slew rate limiting in the input stage. In most discrete instrumentation amplifier realizations, the stray capacitance mismatch dominates simply because the stray capacitances are relatively large (this can be trimmed out in a discrete amplifier). In a hybrid circuit such as the LH0038, stray capacitance is minimized, so the effects of mismatch are also minimized.

The response to a pulse or noise spike applied as a common-mode signal may be dominated by the slew characteristics of the input stage. Whenever the common-mode input slew rate exceeds 0.2 V/μs, the 2 input amplifiers will apply identical ramp signals to the final stage and cause its output to go to near 0V. Note that the amplifier is not really active under these conditions as normal mode signal variations will *not* be coupled to the output. Some time may be required for the amplifier to settle after a transient of this kind before the output can be considered representative of the input. Slew rate limiting will not normally be the limiting factor for sine wave common-mode signals as 0.2 V/μs corresponds to about 2 kHz (20 Vp-p).

POWER SUPPLY DECOUPLING

Although the LH0038 exhibits in excess of 120 dB PSRR at DC, the figure degrades to 100 dB at 120 Hz. It is recommended that both V^+ and V^- leads be by-passed with 1 μF electrolytic in shunt with 0.01 μF ceramic disc no further than 1 inch from the device.

Applications Information (Continued)



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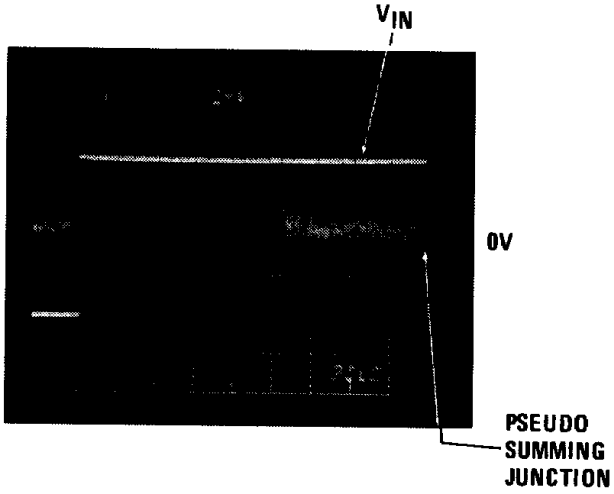
t_s, $A_V = 100$, $V_{IN} = -20V$

FIGURE 11. Settling Time



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t_s, $A_V = 100$, $V_{IN} = -20V$

FIGURE 12. Settling Time

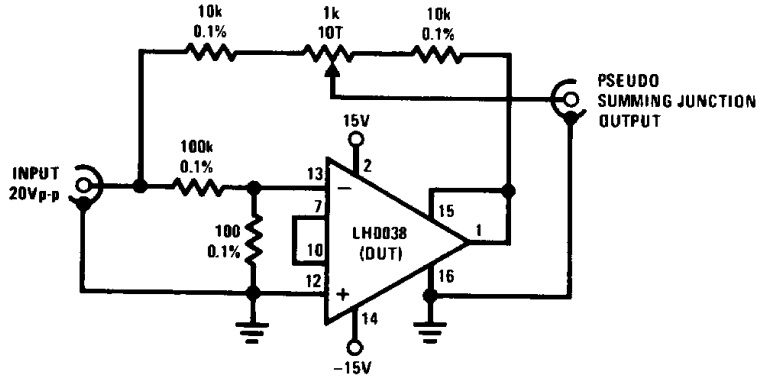

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FIGURE 13. Settling Time Test Circuit

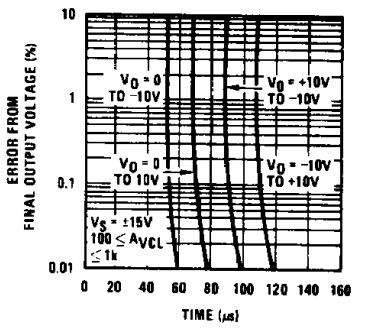

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FIGURE 14. Settling Time

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to 3 dB below the low frequency.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the outputs of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{IOS} = \frac{(V_{OS})\,2k - (V_{OS})\,100}{1900}$$

Where:

$(V_{OS})2k$ = overall offset voltage for A_{VCL} = 2k.

$(V_{OS})100$ = overall offset voltage for A_{VCL} = 100.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end points expressed as a percent of full-scale (10V for operations on ±15V supply). Note that this is a more stringent specification than deviation from the best straight line and is double the number that would be specified if the percentage were based on a 20V (±10V) range.

Guard Voltage Error: The voltage difference between the guard drive output and the average of the 2 input voltages.

Input Bias Current, I_B: The average of the 2 input currents.

Input Common-Mode Voltage Range, V_{INCM}: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Offset Current, I_{OS}: The difference in the currents into the 2 input terminals when the output is at zero.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Overall Offset Voltage, V_{OS}: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input amplifier offset voltage effects, V_{IOS}, and output amplifier effects, V_{OOS}. It is given by:

$$V_{OS} = (A_{VCL})\,(V_{IOS}) - V_{OOS}$$

Where:

A_{VCL} = closed loop gain = 100 to 2k

V_{IOS} = input stage offset voltage

V_{OOS} = output stage offset voltage

Output Offset Voltage, V_{OOS}: The output voltage when theoutputs of the input stage are forced to 0V. V_{OOS} may be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{OOS} = \frac{(20)\,(V_{OS})\,100 - (V_{OS})\,2k}{19}$$

Where:

(V_{OS}) 100 = overall offset voltage for A_{VCL} = 100

(V_{OS}) 2k = overall offset voltage for A_{VCL}

Output Voltage, V_O: The peak output voltage swing, referred to zero.

Offset Voltage Temperature Drift, $\Delta V_{IOS}/\Delta T$: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling times, t_s: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate, S_r: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current, $\pm I_s$: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Supply Voltage Range: The range of voltages on the supply terminals for which the device is operational. Note that the specifications are not guaranteed over the full supply voltage range unless specifically stated.

Transient Response, t_r: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from DC to the frequency where the amplifier open loop gain rolls off to 1.

Closed Loop Gain, A_{VCL}: The ratio of output voltage to input voltage under the stated conditions of source resistance (R_S) and load resistance (R_L).

Voltage Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.