

# LH168P

## 309-output TFT-LCD Source Driver IC

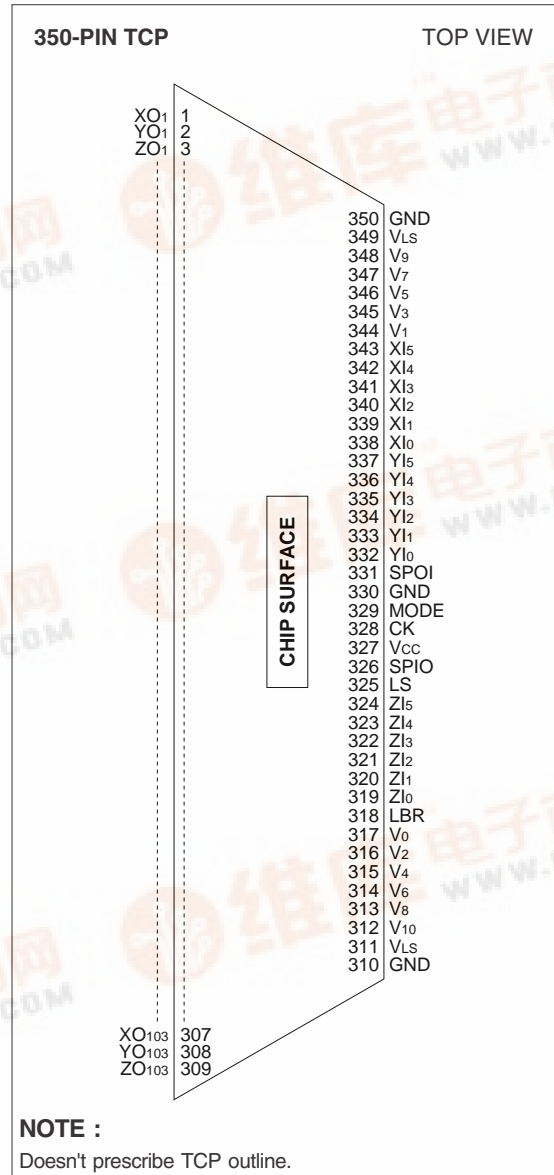
### DESCRIPTION

The LH168P is a 309-output TFT-LCD source driver IC which can simultaneously display 262 144 colors in 64 gray scales.

### FEATURES

- Selectable number of LCD drive outputs : 309/300
- Built-in 6-bit digital input DAC
- Possible to display 262 144 colors in 64 gray scales with reference voltage input of 11 gray scales : This reference voltage input corresponds to  $\gamma$  correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :  
Output shift direction can be selected  
XO<sub>1</sub>, YO<sub>1</sub>, ZO<sub>1</sub>→XO<sub>103</sub>, YO<sub>103</sub>, ZO<sub>103</sub> or  
ZO<sub>103</sub>, YO<sub>103</sub>, XO<sub>103</sub>→ZO<sub>1</sub>, YO<sub>1</sub>, XO<sub>1</sub>
- Shift clock frequency : 55 MHz (MAX.)
- Supply voltages
  - V<sub>CC</sub> (for logic system) : +3.0 to +5.5 V
  - V<sub>LS</sub> (for LCD drive system) : +3.0 to +5.5 V
- Package : 350-pin TCP (Tape Carrier Package)

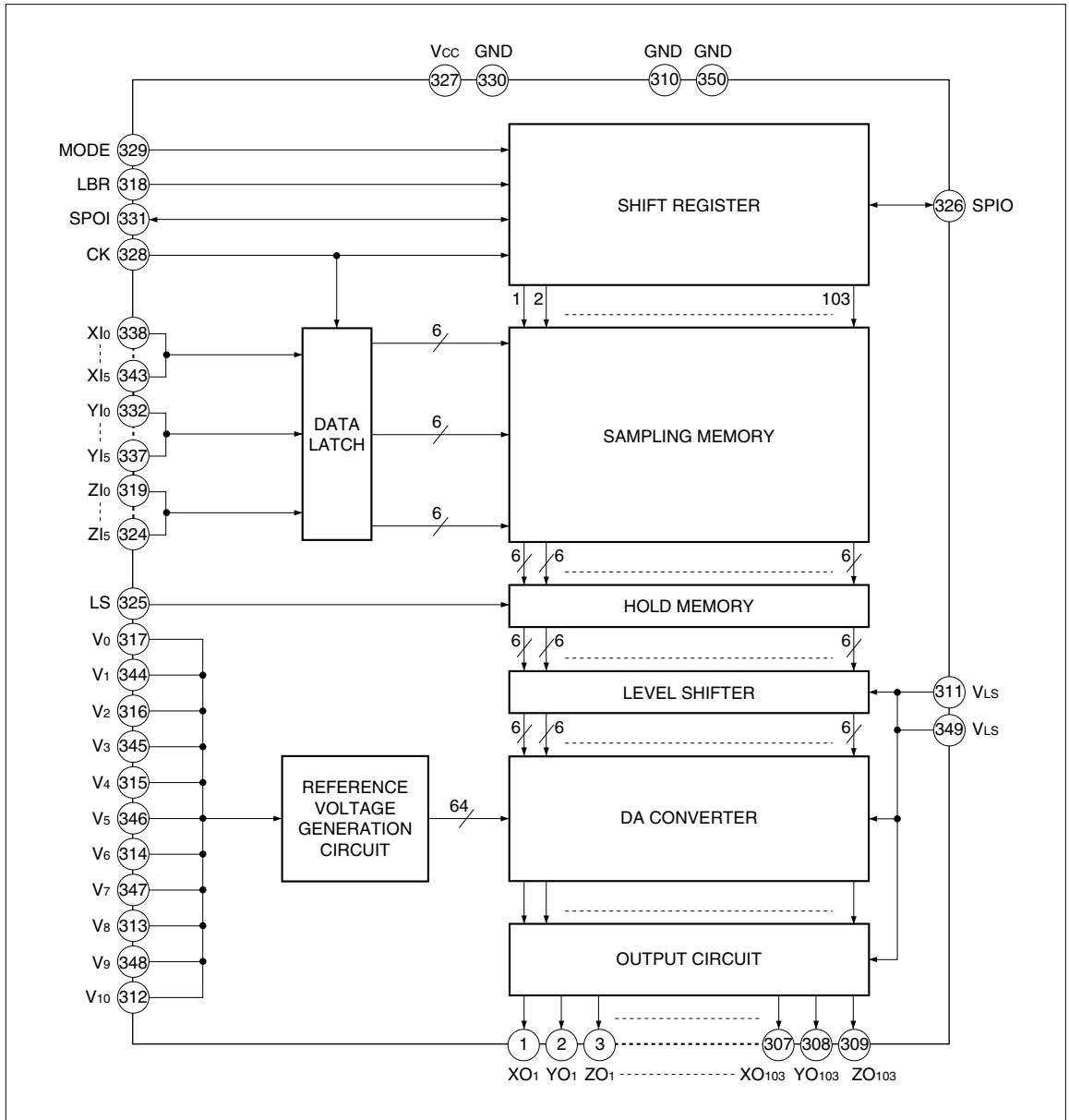
### PIN CONNECTIONS



**PIN DESCRIPTION**

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 309	XO <sub>1</sub> -ZO <sub>103</sub>	O	LCD drive output pins
310, 330, 350	GND	–	Ground pins
311, 349	V <sub>LS</sub>	–	Power supply pins for analog circuit
312 to 317	V <sub>10</sub> , V <sub>8</sub> , V <sub>6</sub> , V <sub>4</sub> , V <sub>2</sub> , V <sub>0</sub>	I	Reference voltage input pins
318	LBR	I	Shift direction selection input pin
319 to 324	ZI <sub>0</sub> -ZI <sub>5</sub>	I	Data input pins
325	LS	I	Latch input pin
326	SPIO	I/O	Start pulse input/cascade output pin
327	V <sub>CC</sub>	–	Power supply pin for digital circuit
328	CK	I	Shift clock input pin
329	MODE	I	309/300-output selection input pin
331	SPOI	I/O	Start pulse input/cascade output pin
332 to 337	YI <sub>0</sub> -YI <sub>5</sub>	I	Data input pins
338 to 343	XI <sub>0</sub> -XI <sub>5</sub>	I	Data input pins
344 to 348	V <sub>1</sub> , V <sub>3</sub> , V <sub>5</sub> , V <sub>7</sub> , V <sub>9</sub>	I	Reference voltage input pins

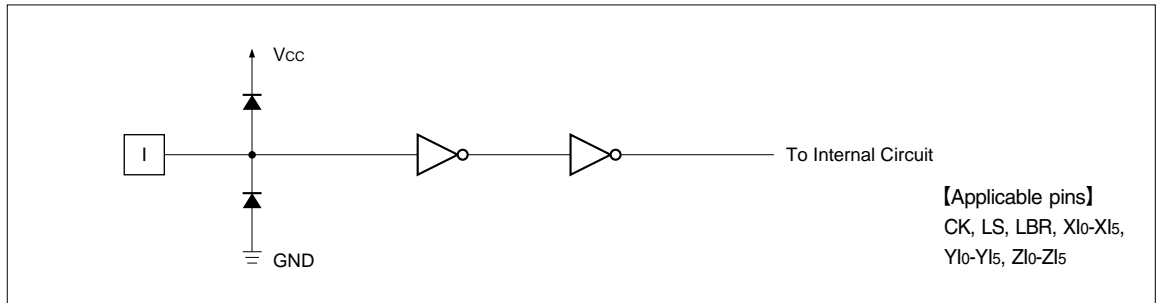
BLOCK DIAGRAM



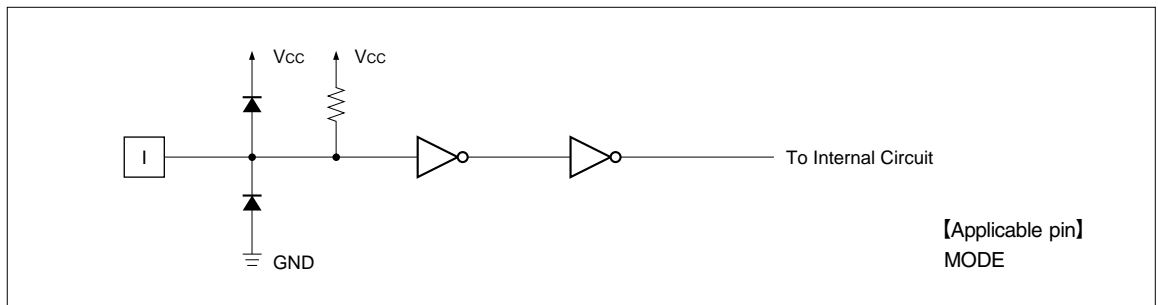
**FUNCTIONAL OPERATIONS OF EACH BLOCK**

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold Memory	Used for latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-corrected 64-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 64 gray scales to LCD drive output pin.

**INPUT/OUTPUT CIRCUITS**



**Fig. 1 Input Circuit (1)**



**Fig. 2 Input Circuit (2)**

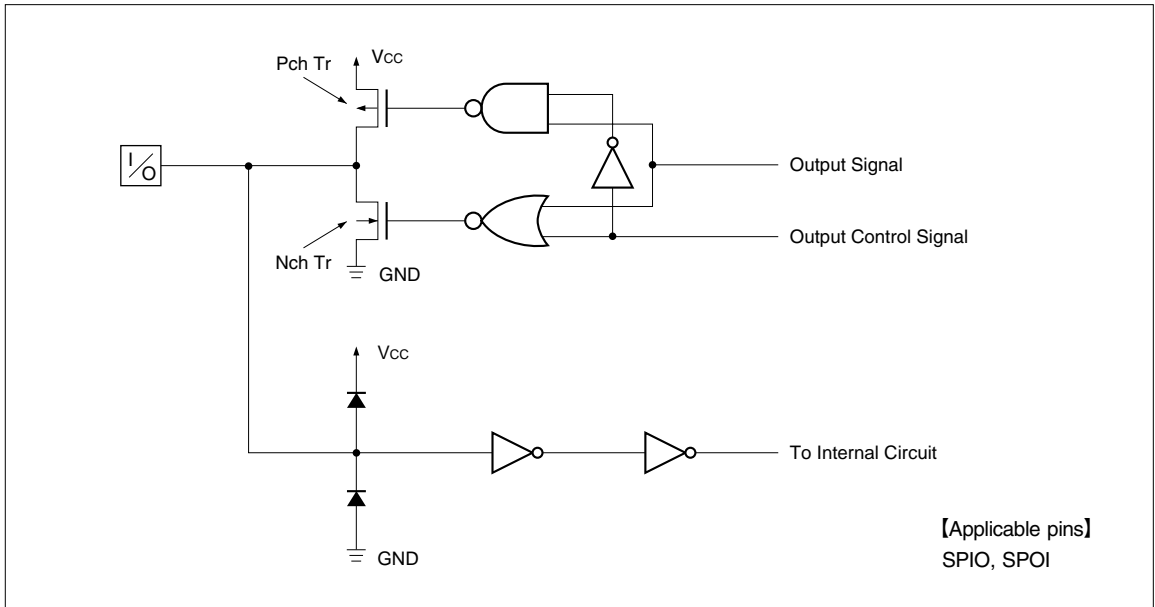


Fig. 3 Input/Output Circuit

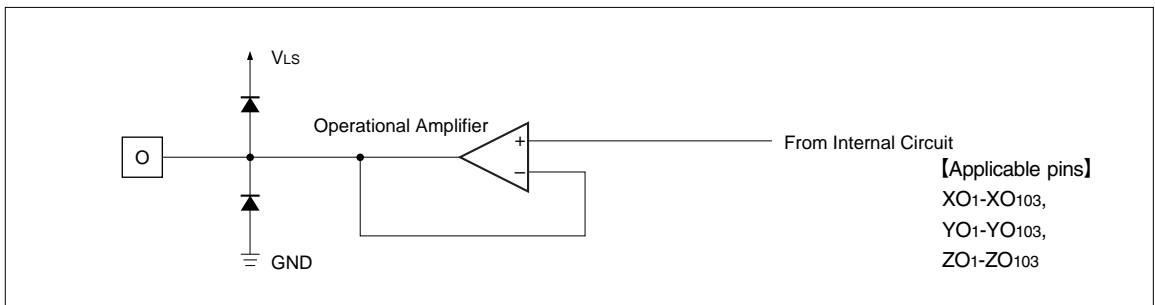


Fig. 4 Output Circuit

## FUNCTIONAL DESCRIPTION

### Pin Functions

SYMBOL	FUNCTION
Vcc	Used as power supply pin for digital circuit, connected to +3.0 to +5.5 V.
VLS	Used as power supply pin for analog circuit, connected to +3.0 to +5.5 V.
GND	Used as ground pin, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting, refer to <b>"Functional Operations"</b> .
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to <b>"Functional Operations"</b> .
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CK	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the rising edge.
V0-V10	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to <b>"Output Voltage Value"</b> . For internal gamma correction, refer to <b>"Gamma Correction Value"</b> .
XI0-XI5 YI0-YI5 ZI0-ZI5	Used as data input pins of R, G, and B colors. 6-bit data are input from data pins at the rising edge of CK. For relation between input data and output voltage values, refer to <b>"Output Voltage Value"</b> . Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
MODE	Used as input pin for selecting the number of LCD drive outputs (309 outputs or 300 outputs). When "L" is entered, it is 309-output mode. When "H" is entered, it is 300-output mode. This pin is pulled up at the inside.
XO1-XO103 YO1-YO103 ZO1-ZO103	Used as LCD drive output pins which output the voltage corresponding to the data input pins (XI0 to XI5, YI0 to YI5, ZI0 to ZI5). When 300-output mode, 9 output pins (XO51 to XO53, YO51 to YO53, ZO51 to ZO53) are invalid. Invalid output pins must be opened. Data of XO1 to XO103 correspond to XI0 to XI5. Data of YO1 to YO103 correspond to YI0 to YI5, and data of ZO1 to ZO103 correspond to ZI0 to ZI5. For relation between input data and output voltage values, refer to <b>"Functional Operations"</b> and <b>"Output Voltage Value"</b> .

## Functional Operations

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction.

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT ( $XO_1, YO_1, ZO_1 \rightarrow XO_{103}, YO_{103}, ZO_{103}$ )	LEFT SHIFT ( $ZO_{103}, YO_{103}, XO_{103} \rightarrow ZO_1, YO_1, XO_1$ )
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

**NOTE :**

Color data corresponding to X, Y, and Z vary depending on the output direction.

## Output Voltage Value

Two voltages are selected from all of the reference voltages ( $V_0$ - $V_{10}$ ) by the upper 3-bit data ( $D_5$ ,  $D_4$  and  $D_3$ ) of the 6-bit input data ( $D_5$ ,  $D_4$ ,  $D_3$ ,  $D_2$ ,  $D_1$  and  $D_0$ ) taken by time sharing, and intermediate

value is determined by the lower 3-bit data ( $D_2$ ,  $D_1$  and  $D_0$ ).

Relation between input data and output voltage values is shown below.

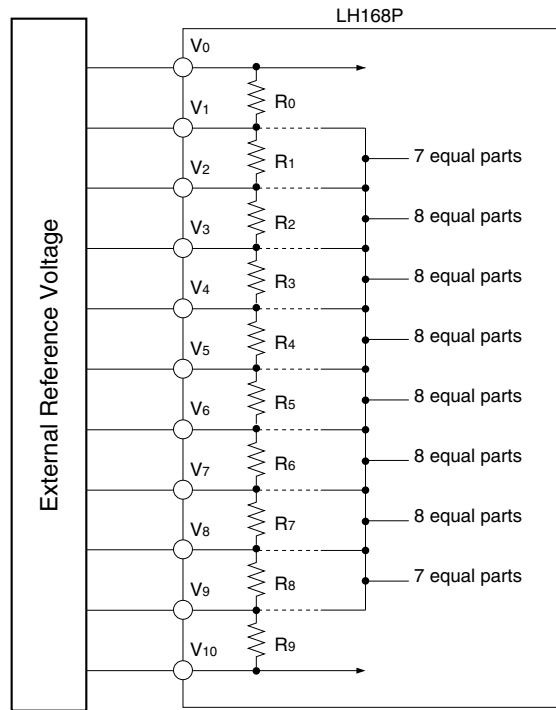
INPUT DATA	OUTPUT VOLTAGE	INPUT DATA	OUTPUT VOLTAGE
0	$V_0$	20	$V_6 + (V_5 - V_6) \times 7/8$
	$V_1$	21	$V_6 + (V_5 - V_6) \times 6/8$
1	$V_2 + (V_1 - V_2) \times 6/7$	22	$V_6 + (V_5 - V_6) \times 5/8$
2	$V_2 + (V_1 - V_2) \times 5/7$	23	$V_6 + (V_5 - V_6) \times 4/8$
3	$V_2 + (V_1 - V_2) \times 4/7$	24	$V_6 + (V_5 - V_6) \times 3/8$
4	$V_2 + (V_1 - V_2) \times 3/7$	25	$V_6 + (V_5 - V_6) \times 2/8$
5	$V_2 + (V_1 - V_2) \times 2/7$	26	$V_6 + (V_5 - V_6) \times 1/8$
6	$V_2 + (V_1 - V_2) \times 1/7$	27	$V_6$
7	$V_2$	28	$V_7 + (V_6 - V_7) \times 7/8$
8	$V_3 + (V_2 - V_3) \times 7/8$	29	$V_7 + (V_6 - V_7) \times 6/8$
9	$V_3 + (V_2 - V_3) \times 6/8$	2A	$V_7 + (V_6 - V_7) \times 5/8$
A	$V_3 + (V_2 - V_3) \times 5/8$	2B	$V_7 + (V_6 - V_7) \times 4/8$
B	$V_3 + (V_2 - V_3) \times 4/8$	2C	$V_7 + (V_6 - V_7) \times 3/8$
C	$V_3 + (V_2 - V_3) \times 3/8$	2D	$V_7 + (V_6 - V_7) \times 2/8$
D	$V_3 + (V_2 - V_3) \times 2/8$	2E	$V_7 + (V_6 - V_7) \times 1/8$
E	$V_3 + (V_2 - V_3) \times 1/8$	2F	$V_7$
F	$V_3$	30	$V_8 + (V_7 - V_8) \times 7/8$
10	$V_4 + (V_3 - V_4) \times 7/8$	31	$V_8 + (V_7 - V_8) \times 6/8$
11	$V_4 + (V_3 - V_4) \times 6/8$	32	$V_8 + (V_7 - V_8) \times 5/8$
12	$V_4 + (V_3 - V_4) \times 5/8$	33	$V_8 + (V_7 - V_8) \times 4/8$
13	$V_4 + (V_3 - V_4) \times 4/8$	34	$V_8 + (V_7 - V_8) \times 3/8$
14	$V_4 + (V_3 - V_4) \times 3/8$	35	$V_8 + (V_7 - V_8) \times 2/8$
15	$V_4 + (V_3 - V_4) \times 2/8$	36	$V_8 + (V_7 - V_8) \times 1/8$
16	$V_4 + (V_3 - V_4) \times 1/8$	37	$V_8$
17	$V_4$	38	$V_9 + (V_8 - V_9) \times 6/7$
18	$V_5 + (V_4 - V_5) \times 7/8$	39	$V_9 + (V_8 - V_9) \times 5/7$
19	$V_5 + (V_4 - V_5) \times 6/8$	3A	$V_9 + (V_8 - V_9) \times 4/7$
1A	$V_5 + (V_4 - V_5) \times 5/8$	3B	$V_9 + (V_8 - V_9) \times 3/7$
1B	$V_5 + (V_4 - V_5) \times 4/8$	3C	$V_9 + (V_8 - V_9) \times 2/7$
1C	$V_5 + (V_4 - V_5) \times 3/8$	3D	$V_9 + (V_8 - V_9) \times 1/7$
1D	$V_5 + (V_4 - V_5) \times 2/8$	3E	$V_9$
1E	$V_5 + (V_4 - V_5) \times 1/8$		
1F	$V_5$	3F	$V_{10}$

**$\gamma$  (gamma) Correction Value**

Between reference voltage input pins, 7 or 8 resistors of the same resistance value are connected in series.

When the resistance ratio between respective

reference voltage input pins matches the reference voltages ( $V_1$  to  $V_9$ ) for  $\gamma$  correction of LCD panel, the external power supply of the intermediate voltages (for  $V_1$  to  $V_9$  pins) is not required.



The following shows the ratio of  $\gamma$  correction resistance, when  $R_0$  equals 1.

R <sub>9</sub>	1.05
R <sub>8</sub>	1.42
R <sub>7</sub>	0.84
R <sub>6</sub>	0.66
R <sub>5</sub>	0.84
R <sub>4</sub>	0.90
R <sub>3</sub>	1.50
R <sub>2</sub>	2.77
R <sub>1</sub>	2.00
R <sub>0</sub>	1.00

## PRECAUTIONS

### Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

$V_{CC} \rightarrow$  logic input  $\rightarrow V_{LS}, V_0-V_{10}$

When disconnecting the power supply, follow the reverse sequence.

### Reference voltage input

The relation of the reference voltage input is shown here.

$GND < V_0 \leq V_1 \leq \dots \leq V_9 \leq V_{10} < V_{LS}$  or  
 $V_{LS} > V_0 \geq V_1 \geq \dots \geq V_9 \geq V_{10} > GND$

### Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

### Target output load

This IC is designed for a 150 pF output load capacity. When using this IC for other than 150 pF panels, confirm the device is having no problem before using it.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	$V_{CC}$	$V_{CC}$	-0.3 to +6.0	V	1, 2
	$V_{LS}$	$V_{LS}$	-0.3 to +6.0	V	
Input voltage	$V_I$	$V_0-V_{10}$	-0.3 to $V_{LS} + 0.3$	V	
	$V_I$	SPIO, SPOI, CK, LS, MODE, LBR, X10-X15, Y10-Y15, Z10-Z15	-0.3 to $V_{CC} + 0.3$	V	
Output voltage	$V_O$	SPIO, SPOI	-0.3 to $V_{CC} + 0.3$	V	
	$V_O$	XO1-ZO80	-0.3 to $V_{LS} + 0.3$	V	
Storage temperature	$T_{STG}$		-45 to +125	°C	

### NOTES :

1.  $T_A = +25$  °C
2. The maximum applicable voltage on any pin with respect to GND (0 V).

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	$V_{CC}$	+3.0		+5.5	V	1
	$V_{LS}$	+3.0		+5.5	V	
Reference voltage input	$V_0-V_{10}$	0		$V_{LS}$	V	
Clock frequency	f <sub>CK</sub>			55	MHz	
LCD drive output load capacity	CL			150	pF	
Operating temperature	$T_{OPR}$	-20		+75	°C	

### NOTE :

1. The applicable voltage on any pin with respect to GND (0 V).

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

(V<sub>CC</sub> = V<sub>LS</sub> = +3.0 to +5.5 V, T<sub>OPR</sub> = -20 to +75 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V <sub>IL</sub>		X10-X15, Y10-Y15, Z10-Z15, SPIO,	GND		0.3V <sub>CC</sub>	V	
Input "High" voltage	V <sub>IH</sub>		SPOI, CK, LS, LBR, MODE	0.7V <sub>CC</sub>		V <sub>CC</sub>	V	
Output "Low" voltage	V <sub>OL</sub>	I <sub>OL</sub> = 0.3 mA	SPIO, SPOI	GND		GND + 0.4	V	
Output "High" voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.3 mA		V <sub>CC</sub> - 0.4		V <sub>CC</sub>	V	
Input "Low" current	I <sub>ILL1</sub>		X10-X15, Y10-Y15, Z10-Z15, SPIO, SPOI, CK, LS, LBR			10	μA	
	I <sub>ILL2</sub>		MODE			400	μA	
Input "High" current	V <sub>ILH</sub>		X10-X15, Y10-Y15, Z10-Z15, SPIO, SPOI, CK, LS, LBR, MODE			10	μA	
Supply current (In operation mode)	I <sub>CC1</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz (Data sampling state)	V <sub>CC</sub> -GND			12	mA	
Supply current (In standby mode)	I <sub>CC2</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz SPI = GND is fixed. (Standby state)				4	mA	
Supply current (In operation mode)	I <sub>LS1</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz (Data sampling state)	V <sub>LS</sub> -GND			8	mA	
Supply current (In standby mode)	I <sub>LS2</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz SPI = GND is fixed. (Standby state)				7	mA	
Output voltage range	V <sub>OUT</sub>		XO1-ZO103	GND + 0.1		V <sub>LS</sub> - 0.1	V	1
Deviations between output voltage pins	V <sub>OD</sub>			-20		20	mV	
Output current	I <sub>O1</sub> , I <sub>O2</sub>			20	50		μA	
Resistance between reference voltage input pins	R <sub>GMA</sub>		V <sub>0</sub> -V <sub>10</sub>	10	20	30	kΩ	

## NOTES :

1. Criterion of evaluating voltage deviations.

(a) Between output voltage pins

Measuring values : Output voltage value at the time after  
10 μs at the rising edge of LS.

(Average of several times)

(Conditions) Output load capacity is 150 pF.

In a state when the reference voltage is fixed.

Expecting values : Calculated following these specifications.

(Conditions) In a state when the reference voltage is fixed.

(b) Between LCD drivers

Measuring values : Applicable to (a).

(Conditions) Applicable to (a).

Expecting values : Applicable to (a).

(Conditions) Applicable to (a).

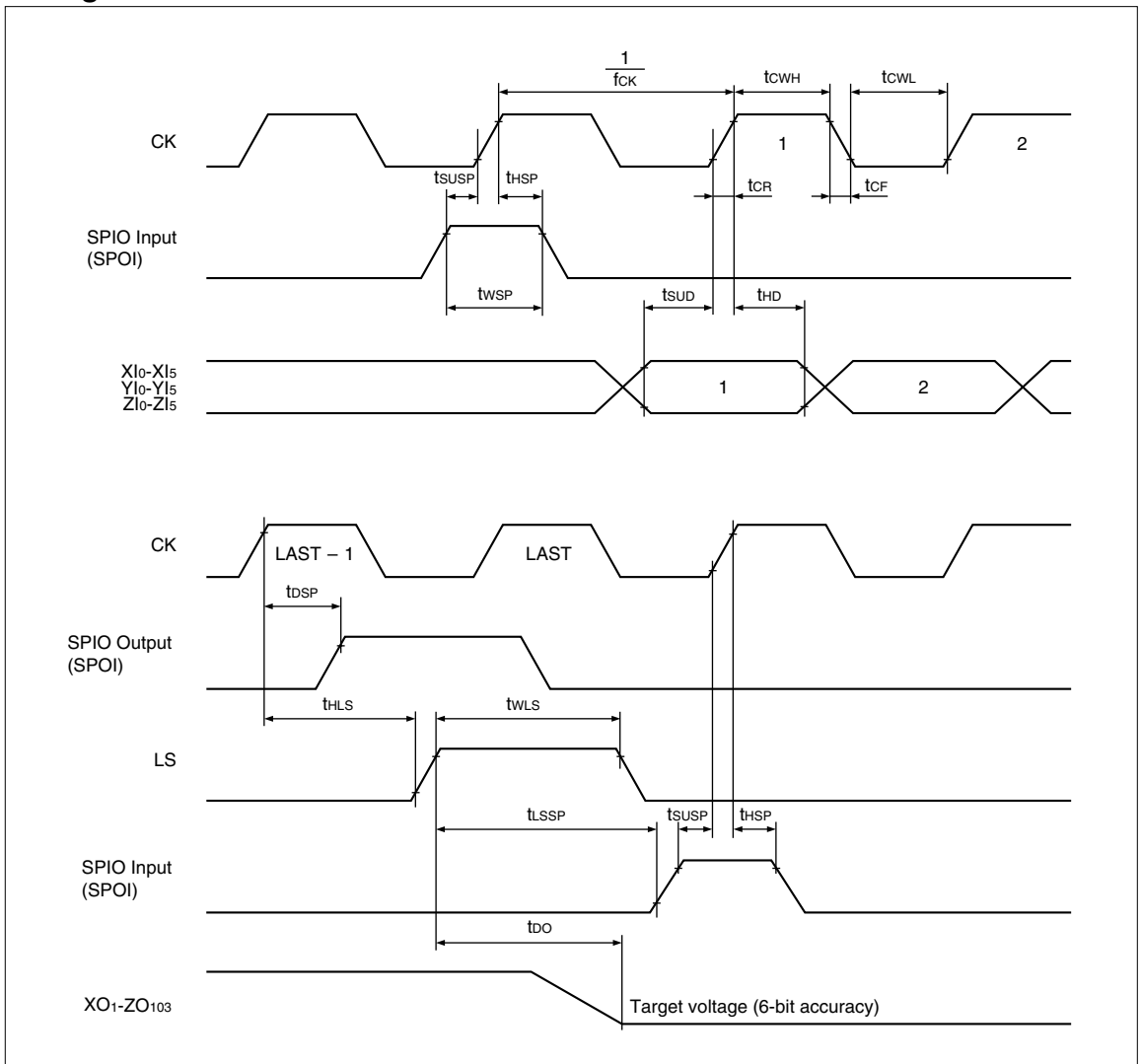
Each input voltage between the LCD drivers must be  
made perfectly equal by connecting corresponding  
reference voltage input pins.2. I<sub>O1</sub> : Applied voltage = 3.0 V for output pins XO1 to ZO103.Output voltage = 2.5 V for output pins XO1 to ZO103.  
V<sub>CC</sub> = V<sub>LS</sub> = 5.0 VI<sub>O2</sub> : Applied voltage = 2.0 V for output pins XO1 to ZO103.Output voltage = 2.5 V for output pins XO1 to ZO103.  
V<sub>CC</sub> = V<sub>LS</sub> = 5.0 V

## AC Characteristics

(VCC = VLS = +3.0 to +5.5 V, TOPR = -20 to +75 °C)

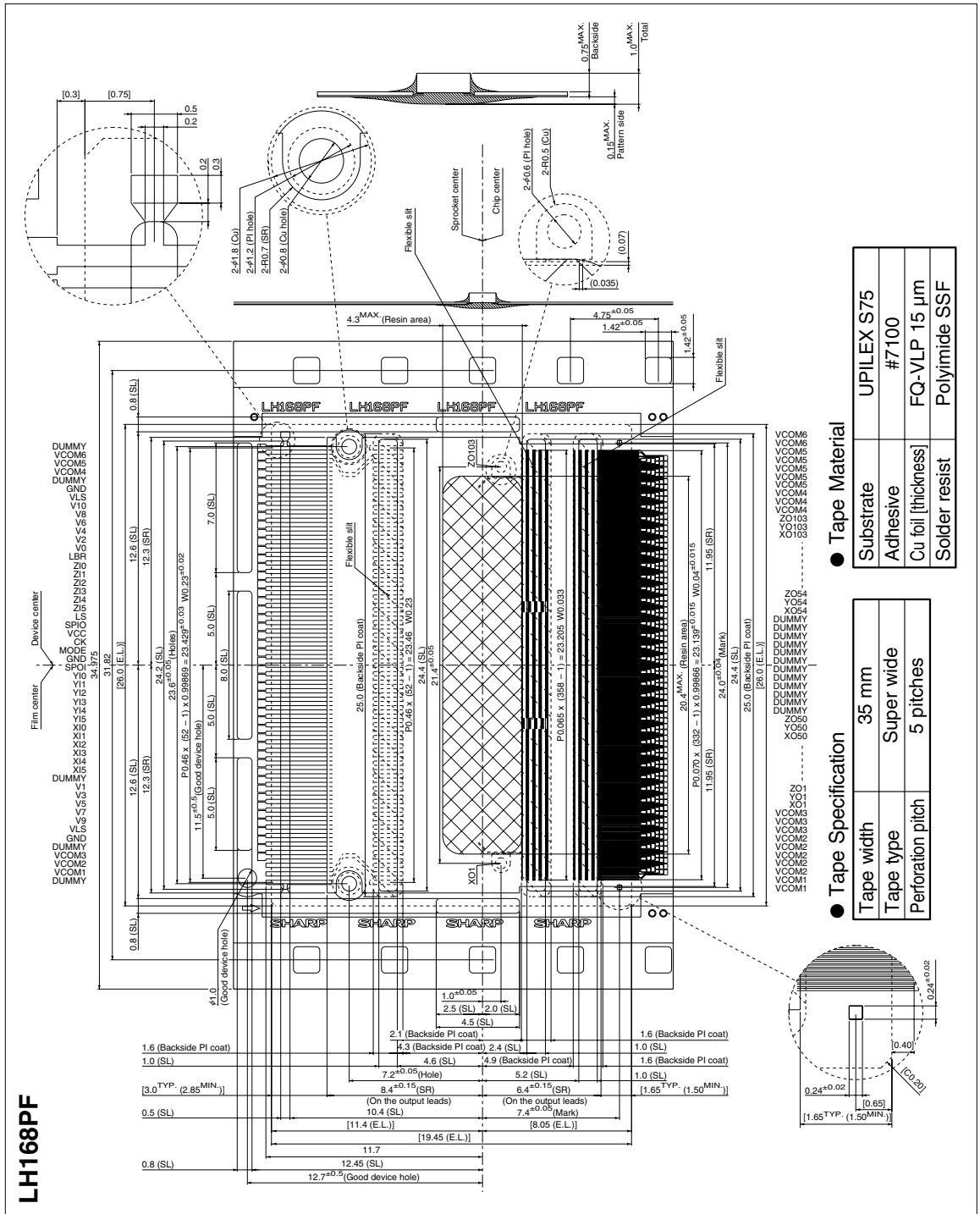
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f <sub>CK</sub>		CK			55	MHz
"H" level pulse width	t <sub>CWH</sub>			4			ns
"L" level pulse width	t <sub>CWL</sub>			4			ns
Input rise time	t <sub>CR</sub>					10	ns
Input fall time	t <sub>CF</sub>					10	ns
Data setup time	t <sub>SUD</sub>		X10-X15, Y10-Y15, Z10-Z15	4			ns
Data hold time	t <sub>HD</sub>			0			ns
Start pulse setup time	t <sub>SUSP</sub>		SPIO, SPOI	4			ns
Start pulse hold time	t <sub>HSP</sub>			0			ns
Start pulse width	t <sub>WSP</sub>					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t <sub>DSP</sub>	CL = 15 pF					12
LCD drive output delay time	t <sub>DO</sub>	CL = 150 pF	XO1-ZO103			10	μs
LS signal-SPI signal setup time	t <sub>LSSP</sub>		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t <sub>HLS</sub>			7			ns
LS signal "H" level width	t <sub>WLS</sub>			$\frac{1}{f_{CK}}$			ns

Timing Chart



PACKAGES

(Unit : mm)



**● Tape Material**

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	FQ-VLP 15 μm
Solder resist	Polyimide SSF

**● Tape Specification**

Tape width	35 mm
Tape type	Super wide
Perforation pitch	5 pitches

