LH1694

256-output TFT-LCD Gate Driver IC

DESCRIPTION

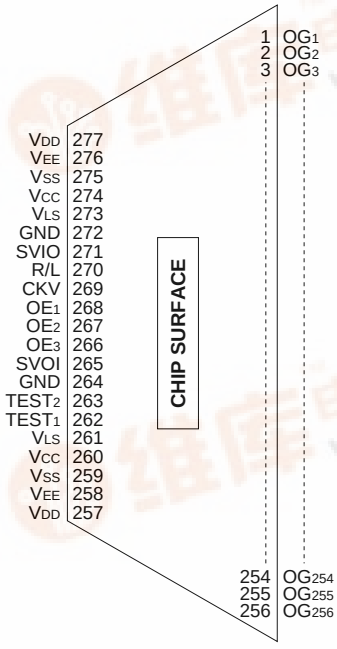
The LH1694 is a 256-output TFT-LCD gate driver IC.

FEATURES

- Number of LCD drive outputs : 256
- LCD drive output sequence :
  Output shift direction can be selected
  $OG_1 \rightarrow OG_{256}$ or $OG_{256} \rightarrow OG_1$
- Enable chain connection
- Usable with both positive/negative power supplies
- Output signal masking function
- Input signal voltage : +2.7 to +3.6 V
- LCD drive voltage : +16.0 to +42.0 V
- Operating temperature : −30 to +85 ˚C
- Package : 277-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

277-PIN TCP TOP VIEW



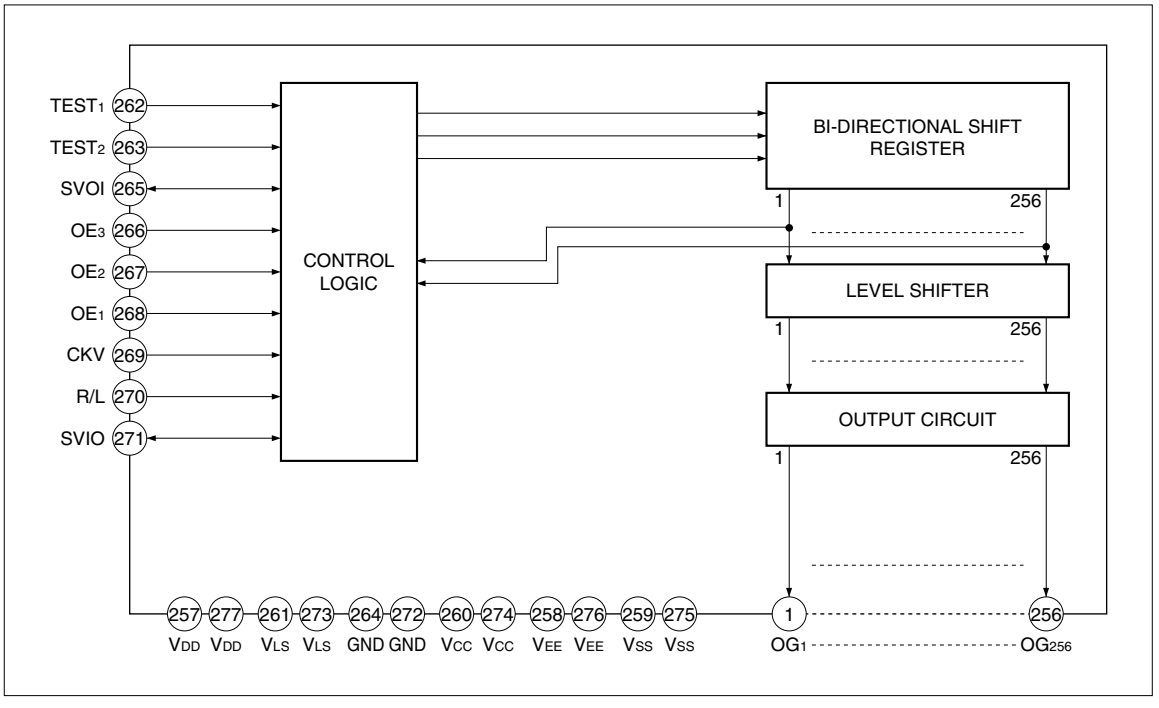
NOTE :

Doesn't prescribe TCP outline.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 256	OG_1-OG_{256}	O	LCD drive output pins
257, 277	V_{DD}	–	Power supply pins for LCD drive
258, 276	V_{EE}	–	Power supply pins for LCD drive
259, 275	V_{SS}	–	Power supply pins for logic system
260, 274	V_{CC}	–	Power supply pins for logic system
261, 273	V_{LS}	–	Power supply pins for logic input/output systems
264, 272	GND	–	Ground pins for logic input
262, 263	$TEST_1$, $TEST_2$	I	IC test pins
265	SVOI	I/O	Vertical scanning start pulse input/output pin
266 to 268	OE_3-OE_1	I	Input pins for output enable
269	CKV	I	Vertical shift clock input pin
270	R/L	I	Pin for selecting bi-directional shift register and setting cascade sequence
271	SVIO	I/O	Vertical scanning start pulse input/output pin

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Control Logic	Used to create signals necessary for mode selecting signal, cascade sequence setting signal and for operation of bi-directional shift register.
Bi-directional Shift Register	Used as transfer circuit of LCD drive output start signal. It is possible to set LCD drive output sequence of $OG_1 \rightarrow OG_{256}$ direction or $OG_{256} \rightarrow OG_1$ direction.
Level Shifter	Used as circuit which shifts LCD drive output signals transferred by bi-directional shift register to V_{DD}-V_{EE} level.
Output Circuit	Configured with output buffers to output V_{DD}-V_{EE} level.

INPUT/OUTPUT CIRCUITS

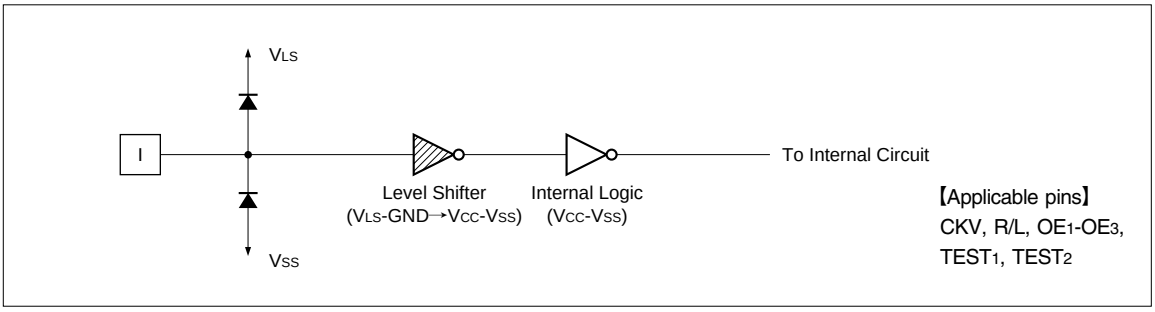


Fig. 1 Input Circuit

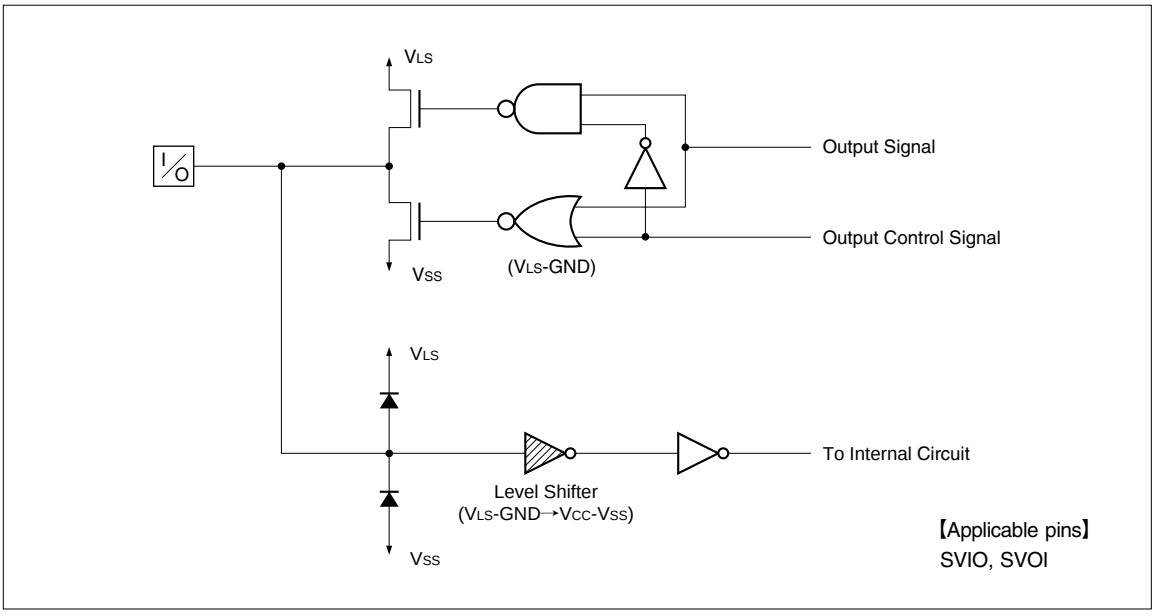


Fig. 2 Input/Output Circuit

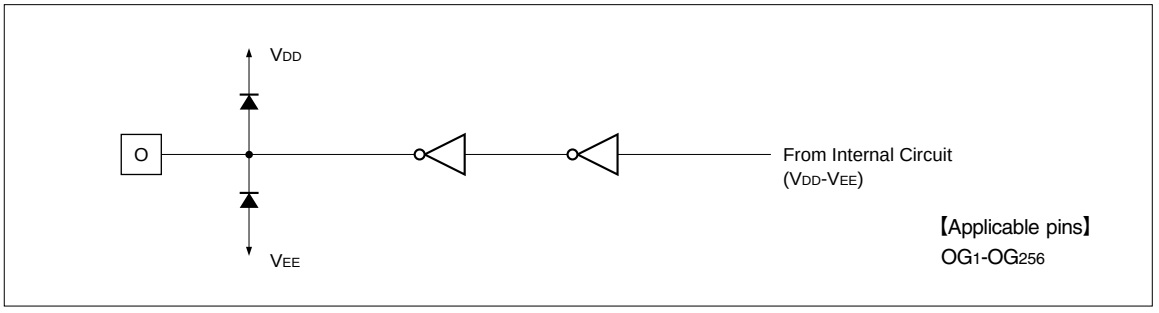


Fig. 3 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
V_{DD}	Used as power supply pin for high level LCD drive.
V_{LS}	Used as power supply pin for input level shifters.
GND	Used as power supply pin for input level shifters.
V_{CC}	Used as power supply pin for logic system, normally connected to V_{SS} + 5.0 V.
V_{EE}	Used as power supply pin for low level LCD drive.
V_{SS}	Used as logic system power supply pin.
CKV	Used as vertical shift clock pulse input pin.
SVIO SVOI	Used as vertical scanning start pulse input/output pins. Data input/output pins for shift register. During input, data is read at the rising edge of the CKV. During output, data is output at the falling edge of the CKV. • When R/L = "H". SVOI is set to data output pin for next cascade, and SVIO is set to input pin for shift data. • When R/L = "L". SVOI is set to input pin for shift data, and SVIO is set to data output pin for next cascade.
R/L	Used as input pin for selecting the shift direction of bi-directional shift register and for setting the sequence of cascade connection. LCD drive outputs shift from OG_1 to OG_{256} when set to "H". LCD drive outputs shift from OG_{256} to OG_1 when set to "L".
OE_1 OE_2 OE_3	Input pins for output-enable. LCD drive output is set to "L", when OE_1, OE_2, and OE_3 pins are set to "H", and it has no relation with clock input. Relationship between enable control and output pins; OE_1 : OG_1, OG_4 ··· OG_{250}, OG_{253}, OG_{256} OE_2 : OG_2, OG_5 ··· OG_{251}, OG_{254} OE_3 : OG_3, OG_6 ··· OG_{252}, OG_{255}
$TEST_1$ $TEST_2$	Used as input pins for IC testing. Must be set to "H".
OG_1-OG_{256}	Used as output pins for LCD drive output, and which output data at 2 levels. • Selecting data is output at V_{DD} level . • Non-selecting data is output at V_{EE} level .

Functional Operations

LH1694 can select the LCD drive output level (OG_1 to OG_{256}) by the set of the input signal (CKV, SVIO, SVOI, OE_1, OE_2, OE_3).

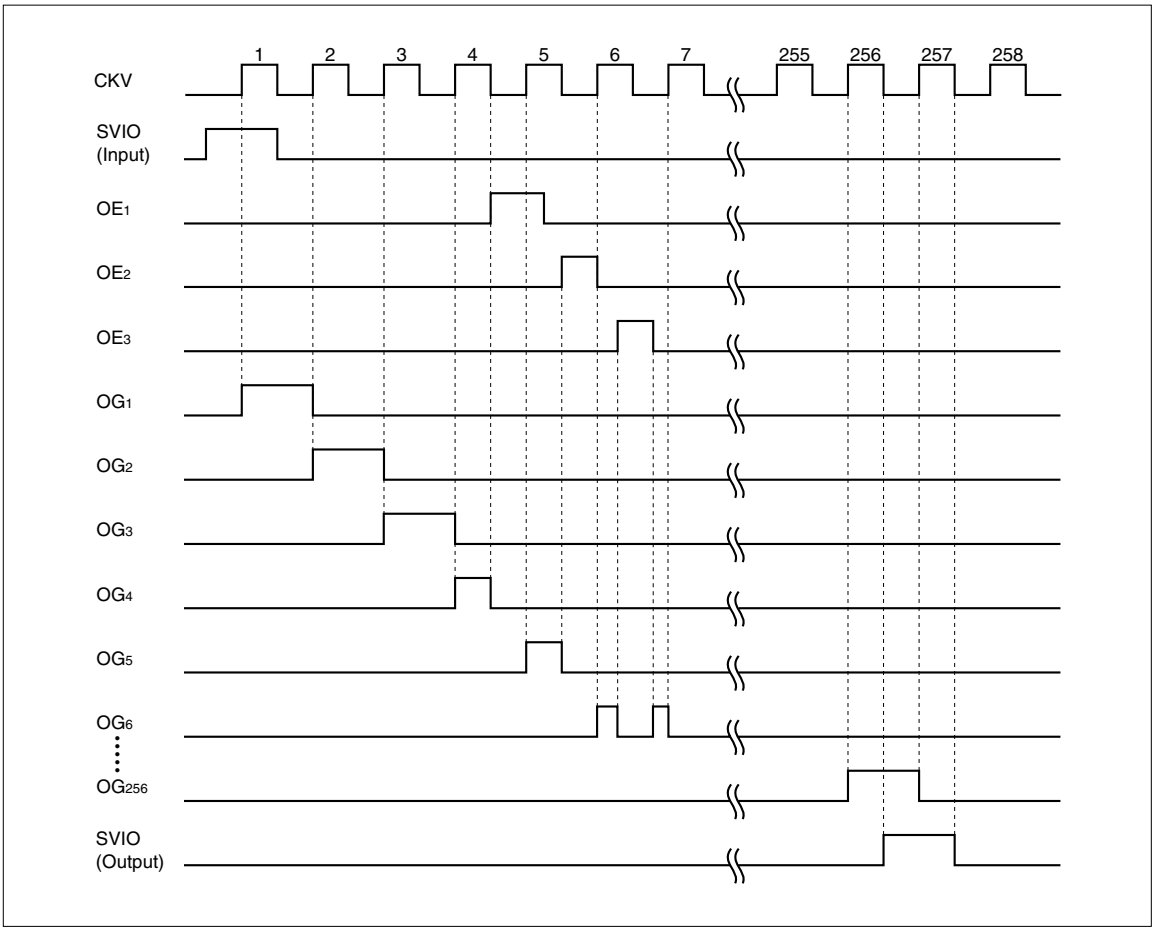
When the pin for selecting the bi-directional shift register (R/L) is set to "H", LCD drive outputs shift from OG_1 to OG_{256}, and when set to "L", LCD drive outputs shift from OG_{256} to OG_1.

OE_1,OE_2 and OE_3 are signals for output-enable. Output pins output non-selecting data (V_{EE} level) when OE_1 to OE_3 pins are set to "H" and it has no relation with input clock.

While R/L = "H" input data from SVIO is read at the rising edge of shift clock (CKV), and outputs to LCD drive output pin OG_1 at the width for one cycle of shift clock. Next LCD drive output pins from OG_2 to OG_{256} are sequentially shifted at the rising edge of the CKV for one cycle. Shift signal of OG_{256} is read at the falling edge of the clock signal, and the input data for the next cascade is output from the SVOI pin.

While R/L = "L" input data from SVOI is read at the rising edge of shift clock (CKV), and outputs to LCD drive output pin OG_{256} at the width for one cycle of shift clock. Next LCD drive output pins from OG_{255} to OG_1 are sequentially shifted at the rising edge of the CKV for one cycle. Shift signal of OG_1 is read at the falling edge of the clock signal and the input data for the next cascade is output from the SVIO pin.

Example of Input/Output Timing (R/L = "H")



PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

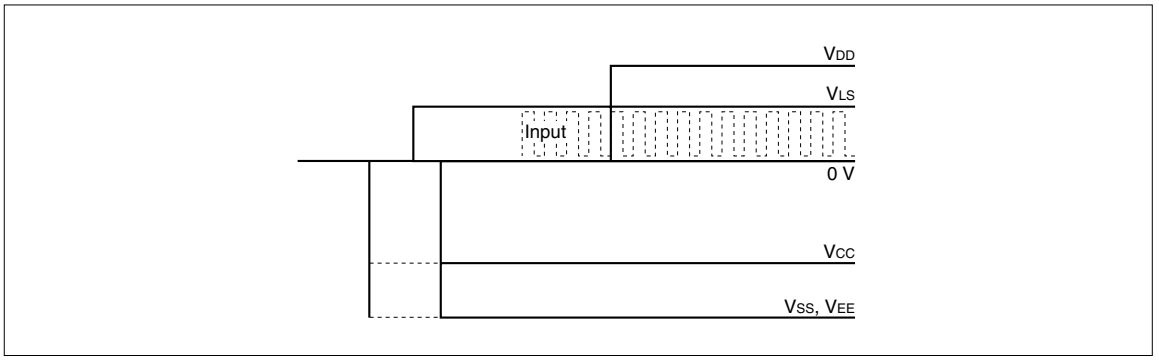
Logic system power supply (V_{LS}) or internal logic system power supply (V_{SS}, V_{CC}; $V_{CC} > V_{SS}$) → logic input → LCD drive power supply (V_{EE}, V_{DD})

It is possible to set voltage V_{EE} to the same as V_{SS}. When connecting the power supply when $V_{EE} = V_{SS}$, observe the following sequence and the recommended sequence figure shown below.

Logic system power supply (V_{LS}), internal logic system power supply (V_{SS}, V_{CC}; $V_{CC} > V_{SS}$) and low-level LCD drive power supply (V_{EE}) → logic input → high-level LCD drive power supply (V_{DD})

When disconnecting the power supply, follow the reverse sequence.

Since the logic state of the internal circuit is unstable immediately after the logic system power is supplied, input CKV and SVIO (or SVOI) while initializing the internal circuit (minimum input clock number is 256 CKV).



Input pin setting

Input pins other than CKV, SVIO and SVOI must be set to "H" or "L" level.

Maximum ratings

When connecting or disconnecting the power, this IC must be used within the range of the absolute maximum ratings.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V_{DD}	V_{DD}	−0.3 to +45.0	V	1, 2
	V_{LS}	V_{LS}	−0.3 to +7.0	V	
	$V_{CC} - V_{SS}$	V_{CC}, V_{SS}	−0.3 to +7.0	V	
	$V_{EE} - V_{SS}$	V_{EE}, V_{SS}	−0.3 to +45.0	V	
	$V_{DD} - V_{EE}$ (V_{SS})	V_{DD}, V_{EE}, V_{SS}	−0.3 to +45.0	V	
Input voltage	V_{IN}	CKV, SVIO, SVOI, R/L, OE_1-OE_3, $TEST_1$, $TEST_2$	−0.3 to V_{LS} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	˚C	

NOTES :

1. T_A = +25 ˚C
2. The maximum applicable voltage on any pin with respect to 0 V.

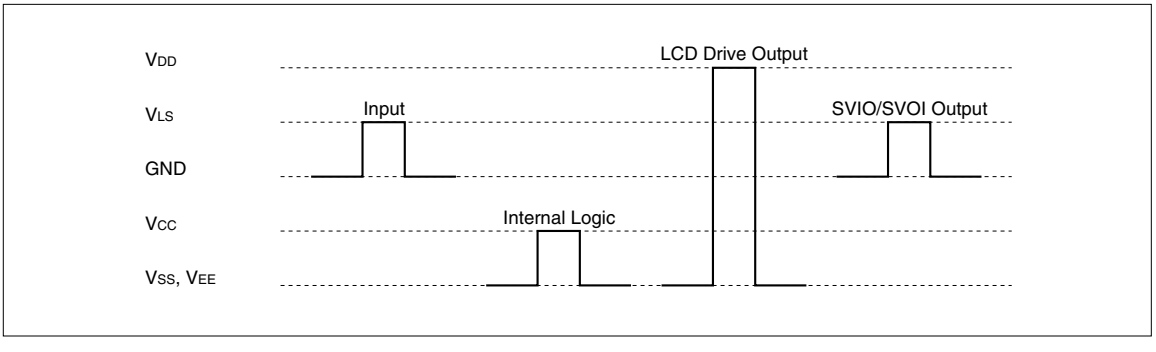
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}	+5.5		+35.0	V	1
	V_{LS}	+2.7	+3.3	+3.6	V	
	V_{SS}	−20.0		−5.0	V	
	V_{CC}	V_{SS} + 4.5		V_{SS} + 5.5	V	
	$V_{EE} - V_{SS}$	0		+11.0	V	
	$V_{DD} - V_{EE}$ (V_{SS})	+16.0	+25.0	+42.0	V	
Input voltage	V_{IN}	0		V_{LS}	V	
Operating temperature	T_{OPR}	−30		+85	˚C	

NOTE :

1. The applicable voltage on any pin with respect to 0 V.

Each power supply pin of LH1694 is set as shown below.



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{LS} = +2.7 to +3.6 V, V_{EE} = V_{SS}, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}	V_{LS} = 2.7 to 3.0 V	CKV, SVIO, SVOI, OE_1-OE_3, R/L			0.2V_{LS}	V	
		V_{LS} = 3.0 to 3.6 V				0.3V_{LS}	V	
Input "High" voltage	V_{IH}	V_{LS} = 2.7 to 3.0 V		0.8V_{LS}			V	
		V_{LS} = 3.0 to 3.6 V		0.7V_{LS}			V	
Output "Low" voltage	V_{OL}	I_{OL} = 0.4 mA	OG_1-OG_{256}			V_{EE} + 0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.4 mA		V_{DD} − 0.4			V	
Input "Low" current	I_{IL}	V_I = 0 V	CKV, SVIO, SVOI, OE_1-OE_3, R/L			5.0	µA	
Input "High" current	I_{IH}	V_I = V_{LS}				5.0	µA	1
Supply current	I_{DD}					100	µA	2
	I_{LS}					1.5	mA	
	I_{CC}					100	µA	
	I_{EE}					100	µA	

NOTES :

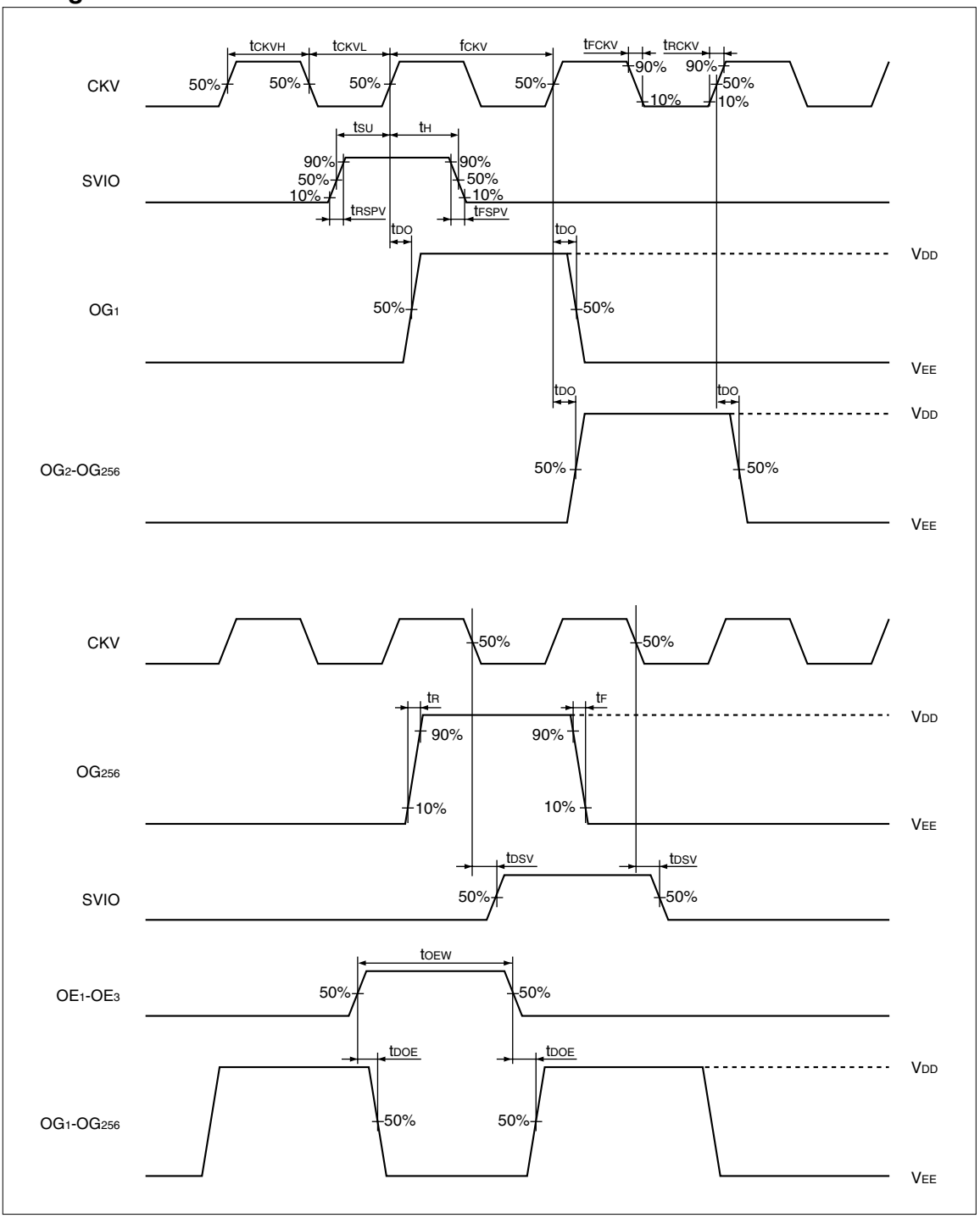
1. All input pins : 3.3 V
2. CKV : Frequency = 31 kHz, "L" period width t_{WL} = 16.2 µs
   SVIO : Frequency = 60 Hz
   OE_1 to OE_3 : 0 V
   Other input pins : 3.3 V
   All output pins are opened.

AC Characteristics

(V_{LS} = +2.7 to +3.6 V, V_{EE} = V_{SS}, T_{OPR} = −30 to +85 °C)

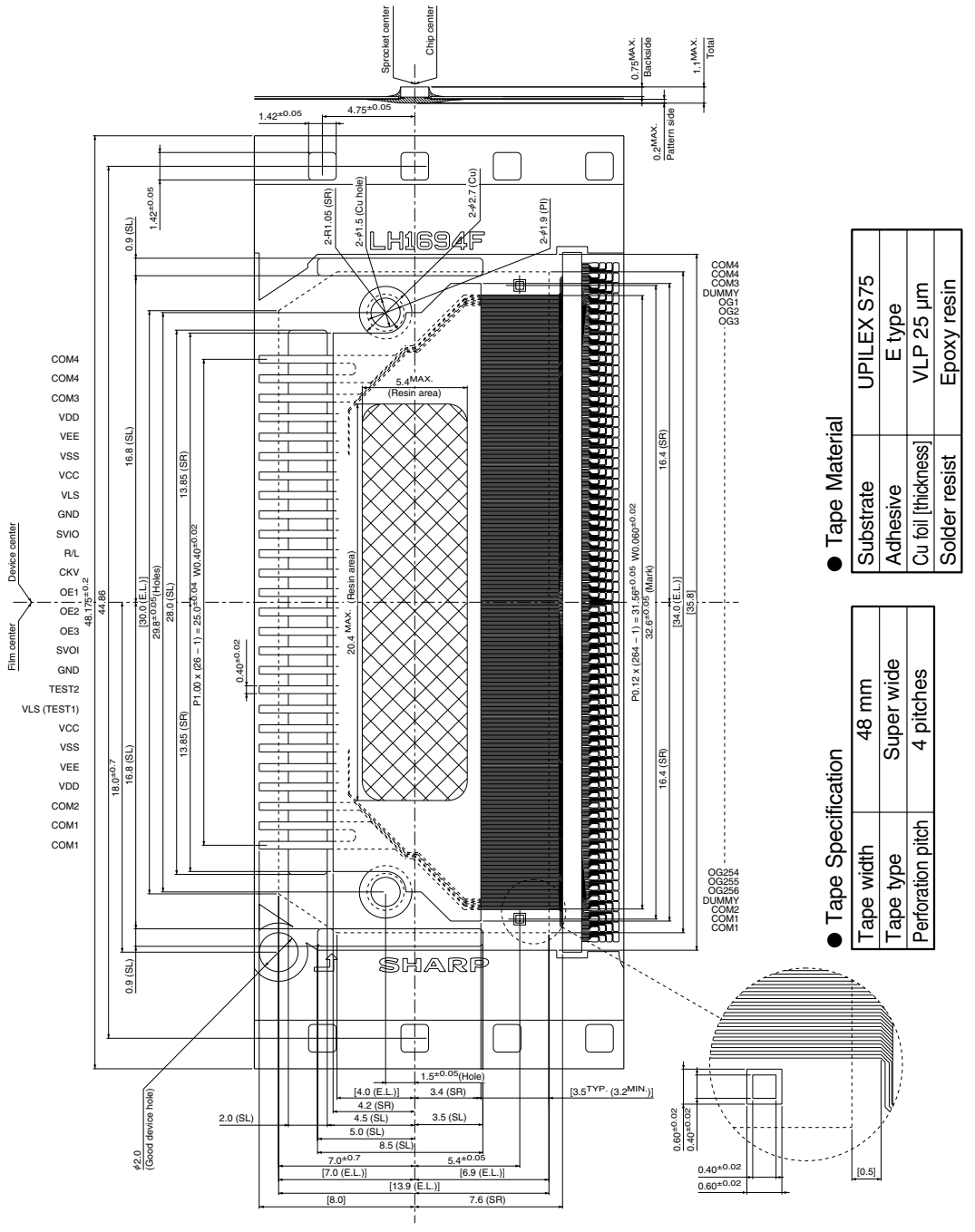
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f_{CKV}		CKV			100	kHz
"H" clock pulse width	t_{CLVH}			1.0			µs
"L" clock pulse width	t_{CKVL}			1.0			µs
Clock rise time	t_{RCKV}					100	ns
Clock fall time	t_{FCKV}					100	ns
Data setup time	t_{SU}		CKV, SVIO, SVOI	100			ns
Data hold time	t_H			300			ns
Pulse rise time	t_{RSPV}		SVIO, SVOI			100	ns
Pulse fall time	t_{FSPV}					100	ns
OE enable time	t_{OEW}		OE_1-OE_3	1.0			µs
Output transfer delay time 1	t_{DO}	C_L = 300 pF	OG_1-OG_{256}			1.0	µs
Output rise time	t_R					1.0	µs
Output fall time	t_F					1.0	µs
Output transfer delay time 2	t_{DOE}					1.0	µs
Output transfer delay time 3	t_{DSV}	C_L = 50 pF	SVIO, SVOI			1.0	µs

Timing Chart



PACKAGE

(Unit : mm)



● Tape Material

Substrate	UPILEX S75
Adhesive	E type
Cu foil [thickness]	VLP 25 µm
Solder resist	Epoxy resin

● Tape Specification

Tape width	48 mm
Tape type	Super wide
Perforation pitch	4 pitches

LH1694F

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