LH28F040SUTD-Z4

4M (512K × 8) Flash Memory

FEATURES

- 512K × 8 Bit Configuration
- 5 V Write/Erase Operation (5 V V_{PP}, 3.3 V_{CC})
  – V_{CC} for Write/Erase at as low as 2.9 V
- Min. 2.7 V Read Capability
  – 190 ns Maximum Access Time (V_{CC} = 2.7 V)
- 2 Banks Enable the Simultaneous Read/Write/Erase Operation
- 32 Independently Lockable Blocks (16K)
- 100,000 Erase Cycles per Block
- Automated Byte Write/Block Erase
  – Command User Interface
  – Status Register
- System Performance Enhancement
  – Erase Suspend for Read
  – Two-Byte Write
  – Bank Erase
- Data Protection
  – Hardware Erase/Write Lockout during Power Transitions
  – Software Erase/Write Lockout
- Independently Lockable for Write/Erase on Each Block (Lock Block and Protect Set/Reset)
- 20 µA (Maximum) I_{CC} in CMOS Standby
- State-of-the-Art 0.55 µm ETOX™ Flash Technology
- 40-Pin, 1.2 mm × 10 mm × 20 mm TSOP (Type I) Package

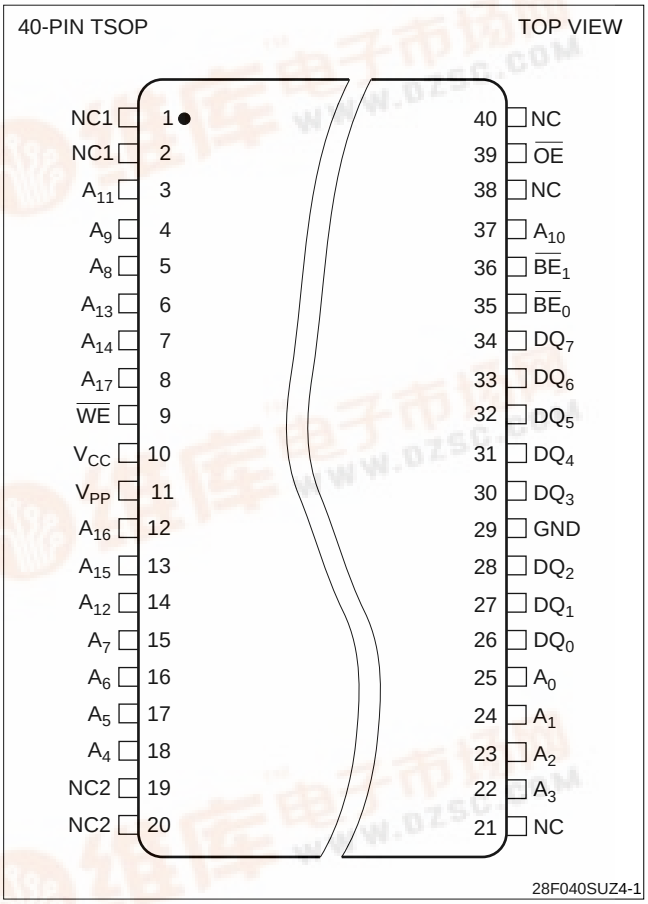


Figure 1. TSOP Configuration

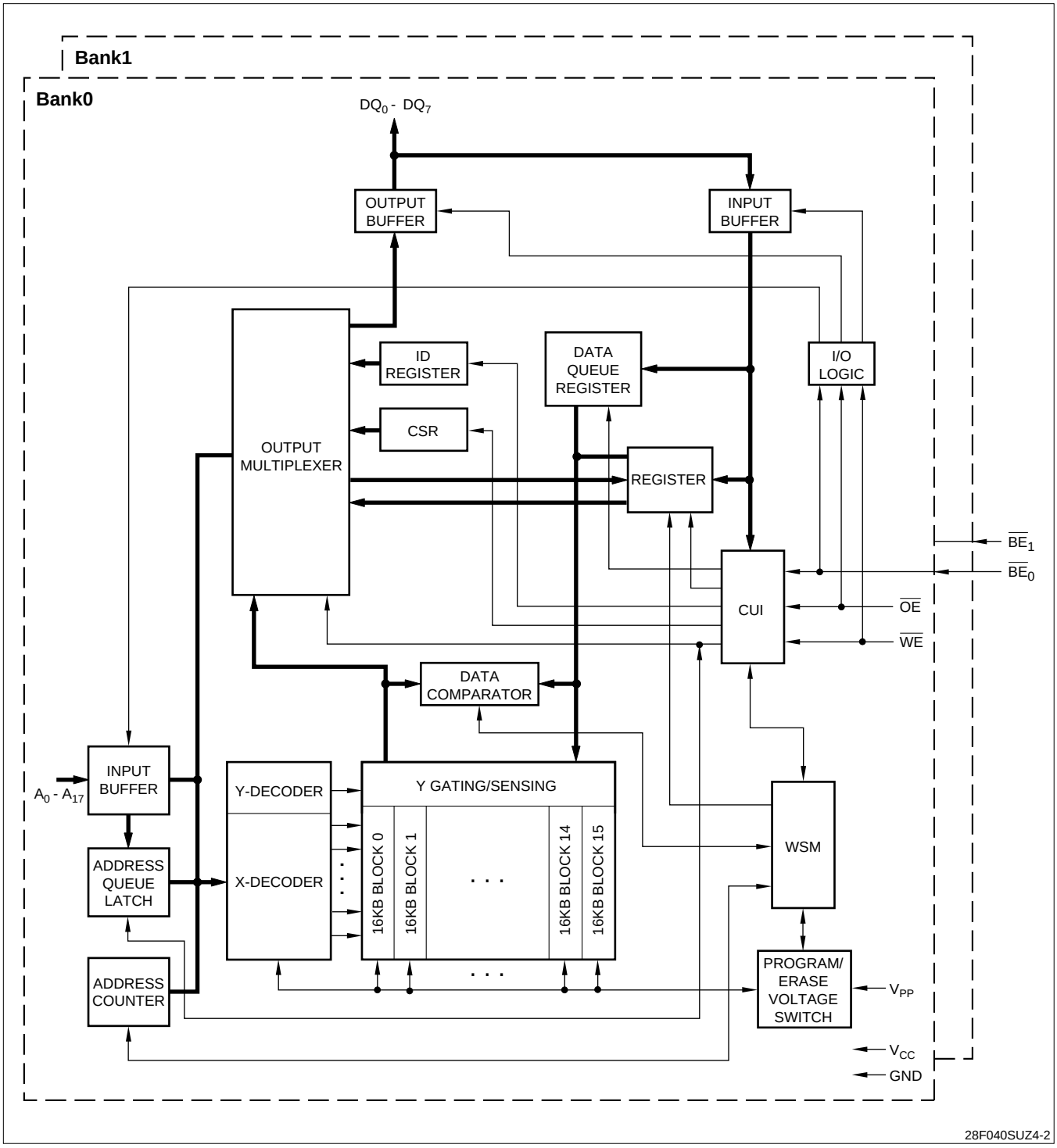


Figure 2. LH28F040SUTD-Z4 Block Diagram

PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A_0 - A_{13}	INPUT	**BYTE-SELECT ADDRESSES:** Select a byte within one 16K block. These addresses are latched during Data Writes.
A_{14} - A_{17}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 16K Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ_0 - DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
$\overline{BE}_0$, $\overline{BE}_1$	INPUT	**BANK ENABLE INPUTS**: Activate the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ must be low to select the device. When $\overline{BE}_0$ is low, bank0 is active. When $\overline{BE}_1$ is low, bank1 is active. Both $\overline{BE}_0$ and $\overline{BE}_1$ must not be low at the same time.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when $\overline{OE}$ is high.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. $\overline{WE}$ is active low, and latches both address and data (command or array) on its rising edge.
V_{PP}	SUPPLY	**ERASE/WRITE POWER SUPPLY (5.0 V ±0.5 V):** For erasing memory array blocks or writing bytes into the flash array.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3 V ±0.3 V):** Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECTION**
NC1, NC2		**OPEN PIN:** But NC1 (between pin1 and pin2) and also NC2 (pin19 and pin20) are connected inside package.

INTRODUCTION

Sharp's LH28F040SUTD-Z4 4M Flash Memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, 3.3V low power operation and very high read/write performance, the LH28040SU-Z4 is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F040SUTD-Z4 is a very high density, highest performance non-volatile read/write solution for solid-state storage applications. Its independently lockable 32 symmetrical blocked architecture (16K each) extended cycling, low power operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for high density memory cards, Resident Flash Arrays and PCMCIA-ATA Flash Drives. The LH28F040SUTD-Z4's 5.0 V/3.3 V power supply operation enables the design of memory cards which can be read in 3.3 V system and written in 5.0 V/3.3 V systems. Its x8 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.55 µm ETOX™ process technology, the LH28F040SUTD-Z4 is the most cost-effective, high-density 3.3 V flash memory.

LH28F040SUTD-Z4 divides 4M into two areas. Each area can read/write/erase independently. For example, while you write and erase on one area, you can simultaneously read the data from the other area. This enables users to reduce the number of components in their system.

DESCRIPTION

The LH28F040SUTD-Z4 is a high performance 4M (4,194,304 bit) block erasable non-volatile random access memory organized as 256K × 8 × 2 banks. The LH28F040SUTD-Z4 includes thirty-two 16K (16,384) blocks. A chip memory map is shown in Figure 3.

The two banks, the one selected by $\overline{BE}_0$ (bank0) and the other selected by $\overline{BE}_1$ (bank1) can be controlled independently. For example, while erase the data in bank0, the data in bank1 can be read out.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Among the significant enhancements of the LH28F040SUTD-Z4:

- 3 V Read, 5 V Write/Erase Operation (5 V V_{PP}, 3 V V_{CC})
- Low Power Capability (2.7 V V_{CC} Read)
- Improved Write/Erase Performance (Two-Byte Serial Write, Bank Erase)
- Dedicated Block Write/Erase Protection
- Command-Controlled Memory Protection Set/Reset Capability

The LH28F040SUTD-Z4 will be available in a 40-pin, 1.2 mm thick × 10 mm × 20 mm TSOP (Type I) package. This form factor and pinout allow for very high board layout densities.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows Byte Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the LH28F008SA 8M Flash memory.

A Superset of commands have been added to the basic LH28F008SA command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Software Locking of Memory Blocks
- Memory Protection Set/Reset Capability
- Two-Byte Serial Writes in 8-bit Systems
- Bank Erase All Unlocked Blocks

Writing of memory data is performed typically within 20 µs. A Block Erase operation erases one of the 32 blocks in typically 1.5 seconds, independent of the other blocks.

LH28F040SUTD-Z4 allows to erase all unlocked blocks for each bank selected by $\overline{BE}_0$ or $\overline{BE}_1$. It is desirable in case of which you have to implement Erase operation maximum 32 times.

LH28F040SUTD-Z4 enables Two-Byte serial Write which is operated by three times command input. This feature can improve system write performance by up to typically 17 µs per byte.

All operations are started by a sequence of Write commands to the device. Status Register (described in detail later) provide information on the progress of the requested operation.

Same as the LH28F008SA, LH28F040SUTD-Z4 requires an operation to complete before the next operation can be requested, also it allows to suspend block erase to read data from any other block, and allow to resume erase operation.

The LH28F040SUTD-Z4 provides user-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable OS or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the LH28F040SUTD-Z4 has a software controlled master Write Protect circuit which prevents any modifications to memory blocks whose lock-bits are set.

When the device power-up, Write Protect Set/Confirm command must be written both in bank0 and bank1. Otherwise, all lock bits in the device remain being locked, can't perform the Write to each block and single Block Erase. Write Protect Set/Confirm command must be written to reflect the actual lock status. However, when the device power-on, Erase All Unlocked Blocks can be used. If used, Erase is performed with reflecting actual lock status, and after that Write and Block Erase can be used.

The LH28F040SUTD-Z4 contains Status Register to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA Flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F040SUTD-Z4 from a LH28F008SA based design.

The LH28F040SUTD-Z4 is specified for a maximum access time of 150 ns (t_{ACC}) at 3.3 V operation (3.0 to 3.6 V) over the commercial temperature range (-20 to +70°C). A corresponding maximum access time of 190 ns (t_{ACC}) at 2.7 V (-20 to +70°C) is achieved for reduced power consumption applications.

The LH28F040SUTD-Z4 incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I_{CC} current is 2 mA at 3.3 V.

A bank reset mode of operation is enabled when whole $\overline{BE}_0$ (or $\overline{BE}_1$), $\overline{WE}$ and $\overline{OE}$ hold low more than 5 µs. In this mode, all operations are aborted, the internal control circuit is reset and CSR register is cleared. When the device power up, this bank reset operation must be executed for each bank to initialize the control circuit. If $\overline{BE}_X$ (either $\overline{BE}_0$ or $\overline{BE}_1$ which is in low state) and or $\overline{WE}$ and or $\overline{OE}$ and or goes high, chip reset mode will be finished. It needs more than 750 ns from one of the $\overline{BE}_X$, $\overline{WE}$ or $\overline{OE}$ goes high until output data are valid. It is impossible to reset the whole chip at once, the bank reset must be executed separately for bank0 and bank1.

A CMOS Standby mode of operation is enabled when $\overline{BE}_X$ transitions high with all input control pins at CMOS levels. In this mode, the device draws an I_{CC} standby current of 20 µA.

Please do not execute reprogramming 0 for the bit which has already been programmed 0. Overwrite operation may generate unerasable bit. In case of reprogramming 0 to the data which has been programmed 1.

- Program 0 for the bit in which you want to change data from 1 to 0.
- Program 1 for the bit which has already been programmed 0.

For example, changing data from 10111101 to 10111100 requires 11111110 programming.

MEMORY MAP

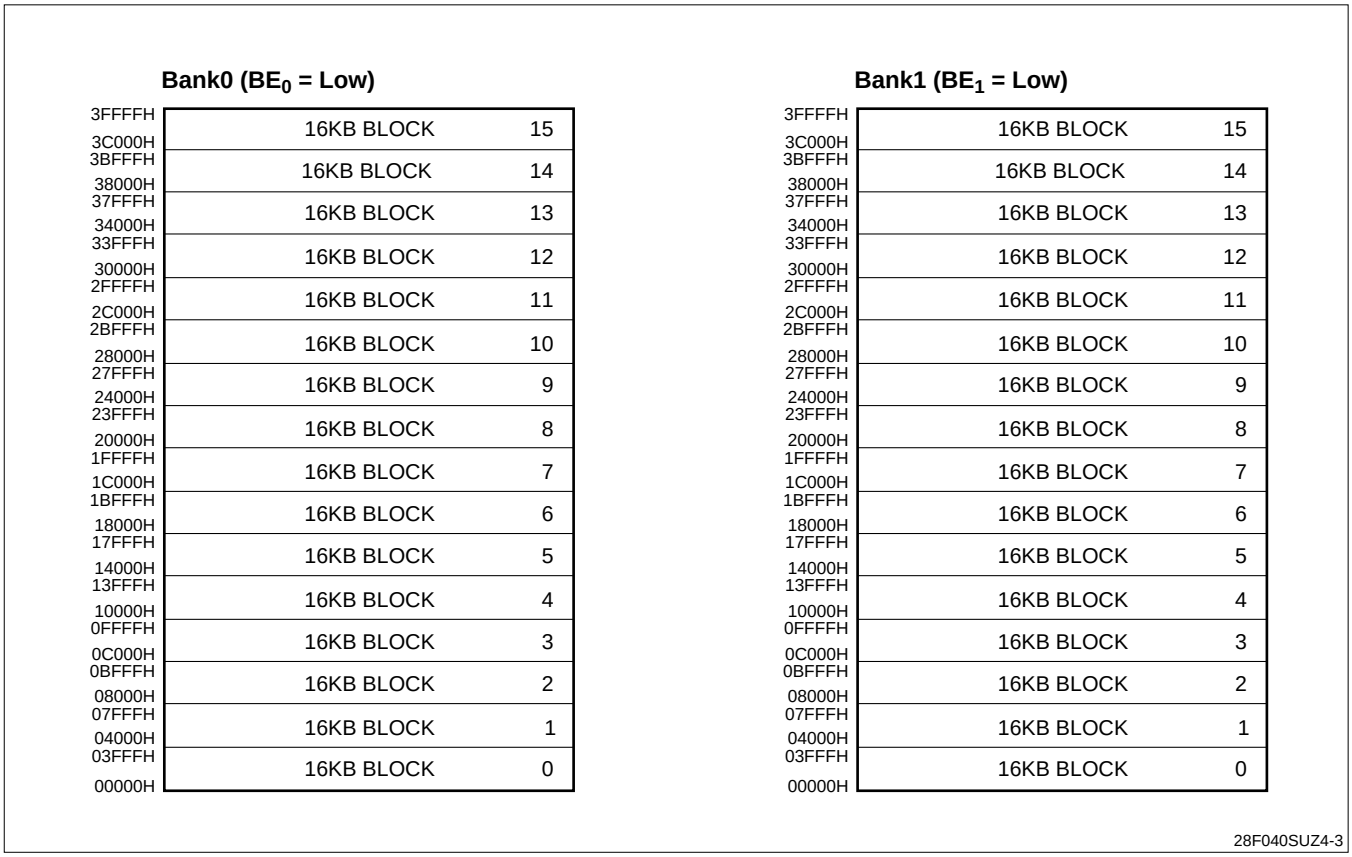


Figure 3. Memory Map

BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

Bus Operations

MODE		$\overline{BE}_0$	$\overline{BE}_1$	$\overline{OE}$	$\overline{WE}$	A_0	DQ_0 - DQ_7	NOTE
Read	Bank 0	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	D_{OUT}	1
	Bank 1	V_{IH}	V_{IL}					
Output Disable		X	X	V_{IH}	V_{IH}	X	High-Z	1
Standby		V_{IH}	V_{IH}	X	X	X	High-Z	1
Manufacturer ID	Bank 0	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	B0H	2
	Bank 1	V_{IH}	V_{IL}					
Device ID	Bank 0	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	31H	2
	Bank 1	V_{IH}	V_{IL}					
Write	Bank 0	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	D_{IN}	1, 3
	Bank1	V_{IH}	V_{IL}					

NOTES:
1. X can be V_{IH} or V_{IL} for address or control pins, which is either V_{OL} or V_{OH}.
2. A_0 at V_{IL} provide manufacturer ID codes. A_0 at V_{IH} provide device ID codes. All other addresses are set to zero.
3. Commands for different Erase operations, Data Write operations, and Lock-Block operations can only be successfully completed when $V_{PP} = V_{PPH}$.
4. Both $\overline{BE}_0$ and $\overline{BE}_1$ must not be low at the same time.

LH28F008SA-Compatible Mode Command Bus Definitions

Following is the commands to be applied to each bank.

COMMAND	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTE
	OPER.	ADDRESS	DATA	OPER.	ADDRESS	DATA	
Read Array	Write	X	FFH	Read	AA	AD	
Intelligent Identifier	Write	X	90H	Read	IA	ID	1
Read Compatible Status Register	Write	X	70H	Read	X	CSRD	2
Clear Status Register	Write	X	50H				3
Byte Write	Write	X	40H	Write	WA	WD	
Alternate Byte Write	Write	X	10H	Write	WA	WD	
Block Erase/Confirm	Write	X	20H	Write	BA	D0H	4
Erase Suspend/Resume	Write	X	B0H	Write	X	D0H	4

ADDRESS
AA = Array Address
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
WD = Write Data

NOTES:
1. Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters Data Write, Erase or Suspend operations.
3. Clears CSR.3, CSR.4, and CSR.5. See Status register definitions.
4. While device performs Block Erase, if you issue Erase Suspend command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase (ESS = 0, WSMS = 1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase Suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase complete.

LH28F040SUTD-Z4 Performance Enhancement Command Bus Definitions

Following is the commands to be applied to each bank.

COMMAND	FIRST BUS CYCLE			SECOND BUS CYCLE			THIRD BUS CYCLE			NOTE
	OPER.	ADD.	DATA	OPER.	ADD.	DATA	OPER.	ADD.	DATA	
Protect Set/Confirm	Write	X	57H	Write	0FFH	D0H				1, 2, 6
Protect Reset/Confirm	Write	X	47H	Write	0FFH	D0H				3, 6
Lock Block/Confirm	Write	X	77H	Write	BA	D0H				1, 2, 4
Bank Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H				1, 2
Two-Byte Write	Write	X	FBH	Write	A10	WD (L, H)	Write	WA	WD (H, L)	1, 2, 5

ADDRESS
BA = Block Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
WD (L, H) = Write Data (Low, High)
WD (H, L) = Write Data (High, Low)

NOTES:
1. After initial device power-up, or reset is completed, the block lock status bit default to the locked state independent of the data in the corresponding lock bits. In order to upload the lock bit status, it requires to write Protect Set/Confirm command.
2. To reflect the actual lock-bit status, the Protect Set/Confirm command must be written after Lock Block/Confirm command.
3. When Protect Reset/Confirm command is written, all blocks can be written and erased regardless of the state of the lock-bits.
4. The Lock Block/Confirm command must be written after Protect Reset/Confirm command was written.
5. A_0 is automatically complemented to load second byte of data A_0 value determines which WD is supplied first: A_0 = 0 looks at the WDL, A_0 = 1 looks at the WDH.
6. Second bus cycle address of Protect Set/Confirm and Protect Reset/Confirm command is 0FFH. Specifically A_9 - A_8 = 0, A_7 - A_0 = 1, others are don't care.

Compatible Status Register

Following is the commands to be applied to each bank.

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
2 = Busy

CSR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

CSR.5 = ERASE STATUS (ES)
1 = Error in Block Erasure
0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS (DWS)
1 = Error in Data Write
0 = Data Write Successful

CSR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

NOTES:
1. $\overline{RY}/\overline{BY}$ output or WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.
2. If DWS and ES are set to '1' during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.
3. The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data-Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.
4. CSR.2 - CSR.0 = Reserved for further enhancements. These bits are reserved for future use and should be masked out when polling the CSR.

4M DUAL WORK FLASH MEMORY SOFTWARE ALGORITHMS

Overview

With the advanced Command User Interface, its Performance Enhancement commands and Status Registers, the software code required to perform a given operation may become more intensive but it will result in much higher write/erase performance compared with current flash memory architectures.

The software flowcharts describing how a given operation proceeds are shown here. Figures 4 through 6 depict flowcharts using the 2nd generation flash device in the LH28F008SA-compatible mode. Figures 7 through 12 depict flowcharts using the 2nd generation flash device's performance enhancement commands mode.

When the device power-up or reset is completed, Set Write Protect command must be written to both the bank selected by $\overline{BE}_0$ and $\overline{BE}_1$ in order to reflect actual block lock status.

When the device power-up or reset is completed, all blocks come up locked. Therefore, Byte Write, Two Byte Serial Write and Block Erase can not be performed in each block. However, at that time, Erase All Unlocked Block is performed normally, if used, and reflect actual lock status, also the unlocked block data is erased. When the device power-up or reset is completed, Set Write Protect command must be written to reflect actual block lock status.

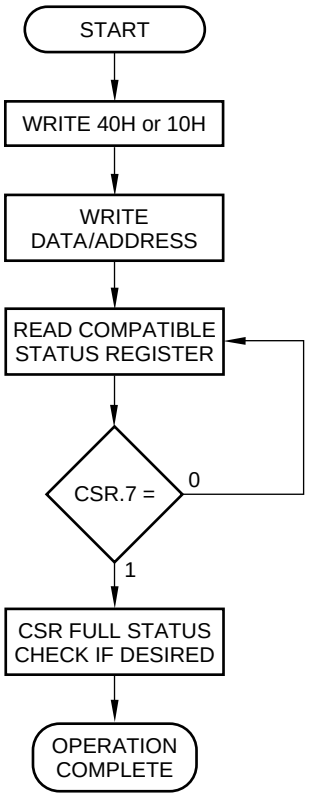
Reset Write Protect command must be written before Write Block Lock command. To reflect actual block lock status, Set Write Protect command is succeeded.

The Compatible Status Register (CSR) used to determine which blocks are locked. In order to see Lock Status of certain block, a Byte Write command (WA = Block Address, WD = FHH) is written to the CUI, after issuing Set Write Protect command. If CSR.7, CSR.5 and CSR.4 (WSMS, ES and DWS) are set to '1's, the block is locked. If CSR.7 is set to '1', the block is not locked.

Reset Write Protect command enables Write/Erase operation to each block.

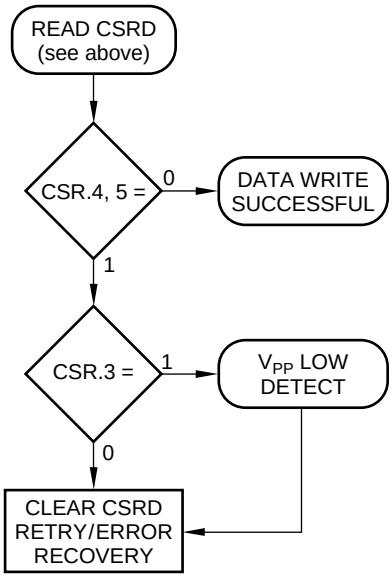
In the case of Block Erase is performed, the block lock information is also erased. Block Lock command and Set Write Protect command must be written to prohibit Write/Erase operation to each block.

There are unassigned commands. It is not recommended that the customer use any command other than the valid commands specified in "Command Bus Definitions". Sharp reserved the right to redefine these codes for future functions.



BUS OPERATION	COMMAND	COMMENTS
Write	Byte Write	D = 40H or 10H A = X
Write		D = WD A = WA
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent Byte Writes. CSR Full Status Check can be done after each Byte Write, or after a sequence of Byte Writes. Write FFH after the last operation to reset device to read array mode. See Command Bus Cycle notes for description of codes.		

CSR FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check CSR.4, 5 1 = Data Write Unsuccessful 0 = Data Write Successful
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK
CSR.3, 4, 5 should be cleared, if set, before further attempts are initiated.		

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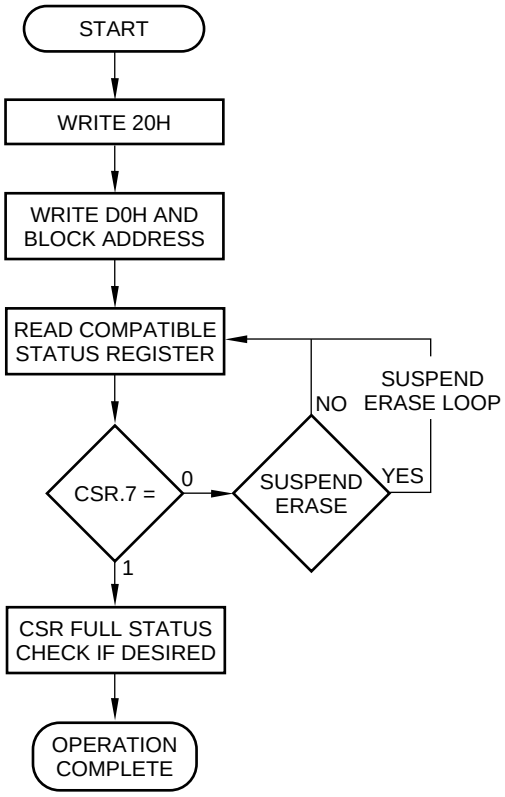
Figure 4. Byte Writes with Compatible Status Register



BUS OPERATION	COMMAND	COMMENTS
Write	Block Erase	D = 20H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or OE to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

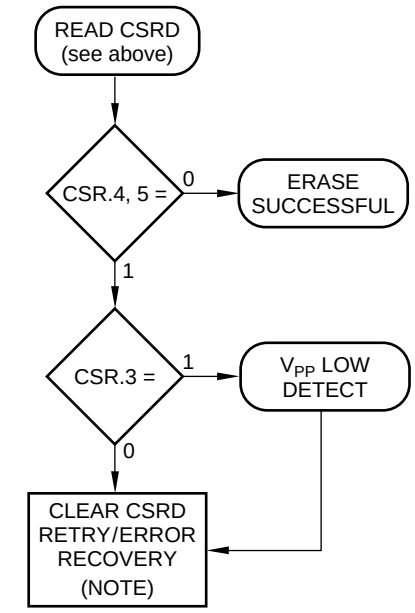
Repeat for subsequent Block Erasures.

CSR Full Status Check can be done after each Block Erase, or after a sequence of Block Erasures.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

CSR FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check CSR.4, 5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

CSR.3, 4, 5 should be cleared, if set, before further attempts are initiated.

NOTE:

If CSR.3 (VPPS) is set to '1', after clearing CSR.3/4/5,

1. Issue Reset WP command.
2. Retry Single Block Erase command.
3. Set WP command is issued, if necessary.

If CSR.3 (VPPS) is set to '0', after clearing CSR.3/4/5,

1. Retry Single Block Erase command.

Where power off or chip reset during erase operation,

1. Clear CSR.3/4/5 and issue Reset WP command,
2. Retry Single Block Erase command.
3. Set WP command is issued, if necessary.

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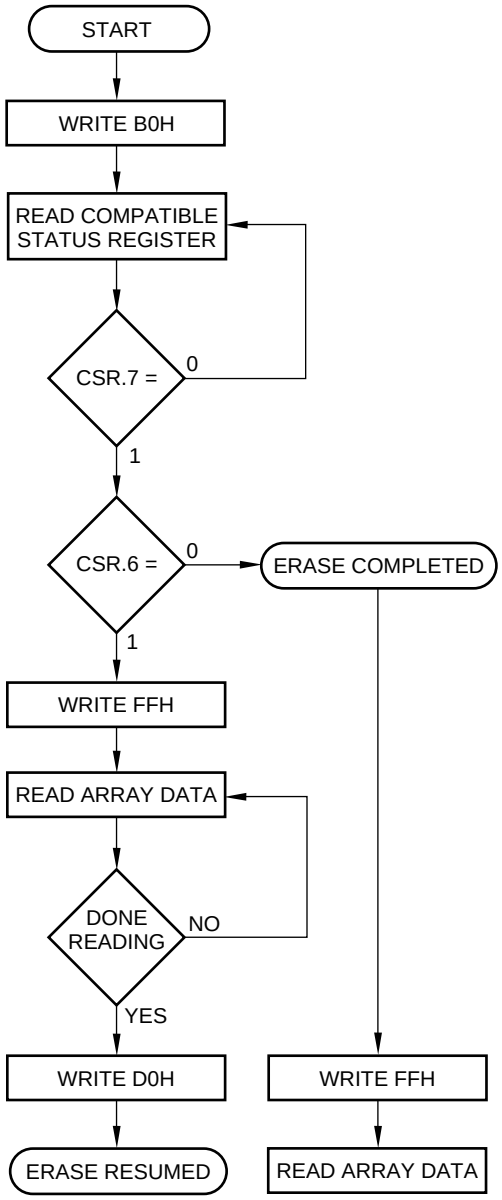
Figure 5. Block Erase with Compatible Status Register



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Suspend	D = B0H A = X
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check CSR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	D = FFH A = X
Read		Q = AD Read must be from block other than the one suspended.
Write	Erase Resume	D = D0H A = X
See Command Bus Cycle notes for description of codes.		

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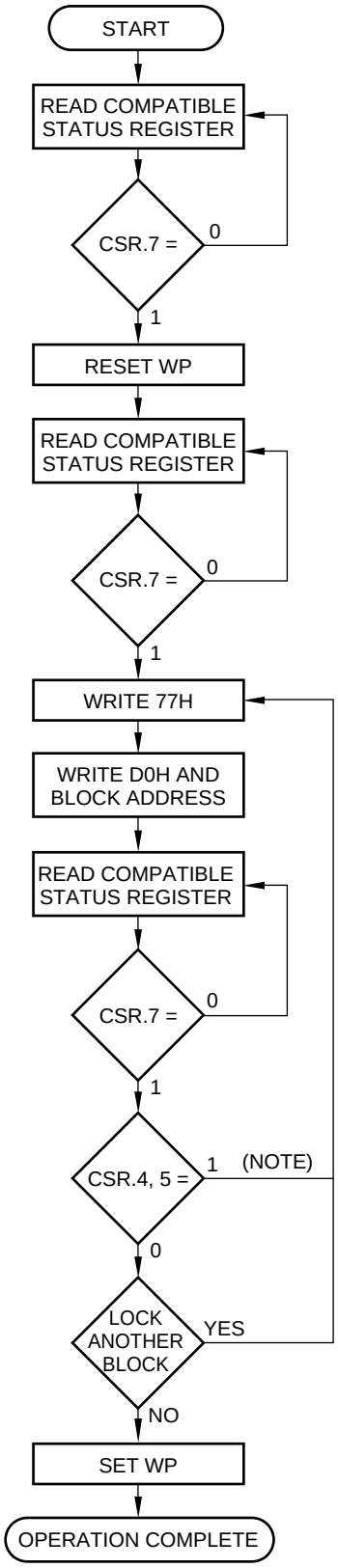
Figure 6. Erase Suspend to Read Array with Compatible Status Register



BUS OPERATION	COMMAND	COMMENTS
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Reset Write Protect	After Write D = 47H A = X, Write D = D0H A = 0FFH
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Lock Block	D = 77H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$, or $\overline{OE}$ to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Set Write Protect	After Write D = 57H A = X, Write D = D0H A = 0FFH

NOTE:

See CSR Full Status Check for Data-Write operation.

If CSR.4, 5 is set, as it is command sequence error, should be cleared before further attempts are initiated.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Definitions for description of codes.

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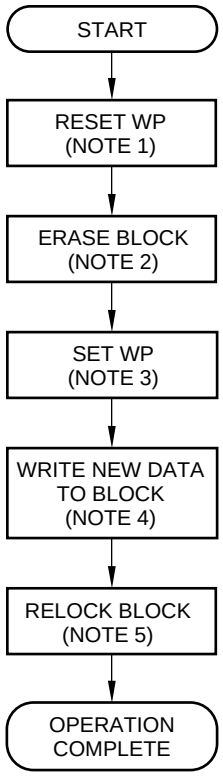
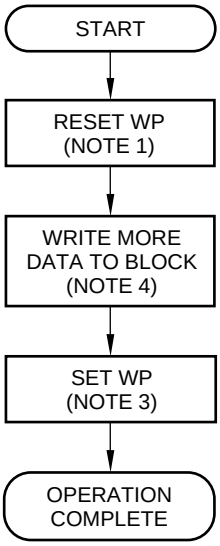
Figure 7. Block Locking Scheme



FLOW TO REWRITE DATA



FLOW TO ADD DATA

NOTES:
1. Use Reset-Write-Protect flowchart. Enable Write/Erase operation to all blocks.
2. Use Block-Erase flowchart. Erasing a block clears any previously established lockout for that block.
3. Use Set-Write-Protect flowchart. This step re-implements protection to locked blocks.
4. Use Byte-Write or 2-Byte-Write flowchart sequences to write data.
5. Use Block-Lock flowchart to write lock bit if desired.

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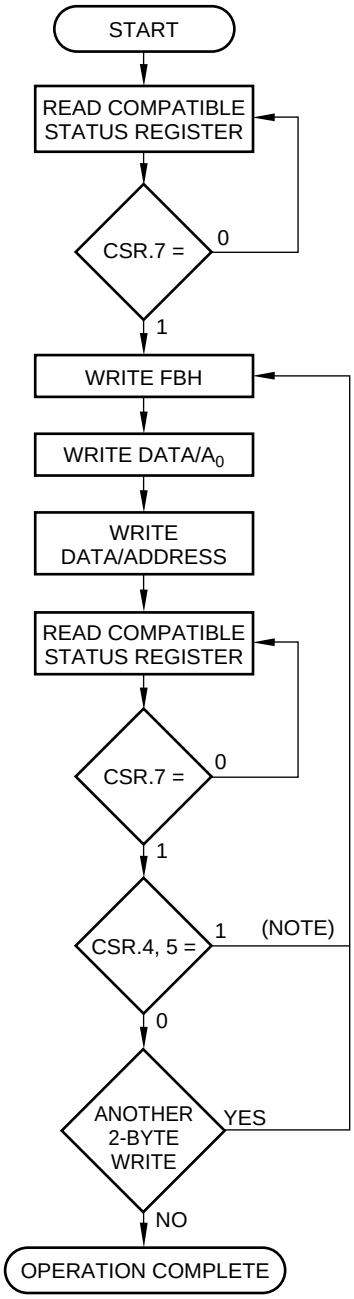
Figure 8. Updating Data in a Locked Block



BUS OPERATION	COMMAND	COMMENTS
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	2-Byte Write	D = FBH A = X
Write		D = WD A_0 = 0 loads low byte of Data Register. A_0 = 1 loads high byte of Data Register. Other Addresses = X
Write		D = WD A = WA Internally, A_0 is automatically complemented to load the alternate byte location of the Data Register.
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ to update CSRD. 1 = WSM Ready 0 = WSM Busy

NOTE:
If CSR.4, 5 is set, as it is command sequence error, should be cleared before further attempts are initiated.

CSR Full Status Check can be done after each 2-Byte Write, or after a sequence of 2-Byte Writes.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

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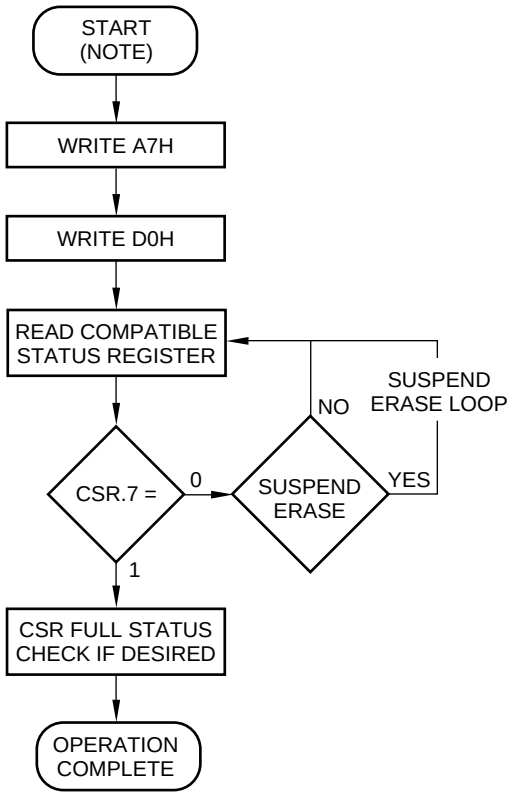
Figure 9. Two-Byte Serial Writes with Compatible Status Registers



BUS OPERATION	COMMAND	COMMENTS
Write	Erase All Unlocked Blocks	D = A7H A = X
Write	Confirm	D = D0H A = X
Read		Q = CSRD Toggle $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

CSR Full Status Check can be done after Erase All Unlocked Block, or after a sequence of Erasures.

Write FFH after the last operation to reset device to read array mode.

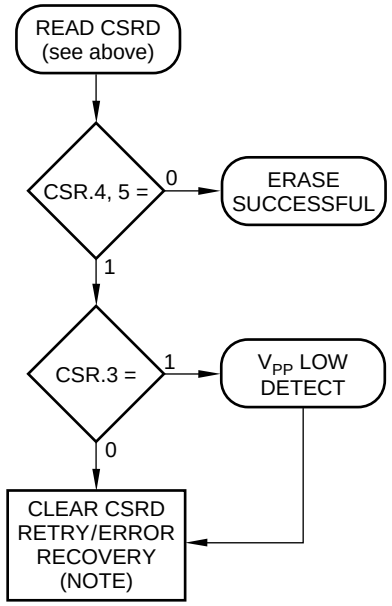
See Command Bus Cycle notes for description of codes.

NOTE:

Where power off or reset during erase operation,

1. Clear CSR.3/4/5 and issue Reset WP command,
2. Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence.
3. Set WP command is issued, if necessary.

CSR FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check CSR.4, 5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

CSR.3, 4, 5 should be cleared, if set, before further attempts are initiated.

NOTE:

If CSR.3 (VPPS) is set to '1', after clearing CSR.3/4/5,

1. Issue Reset WP command,
2. Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence.
3. Set WP command is issued, if necessary.

If CSR.3 (VPPS) is set to '0', after clearing CSR.3/4/5,

1. Retry Erase All Unlocked Block Erase command.

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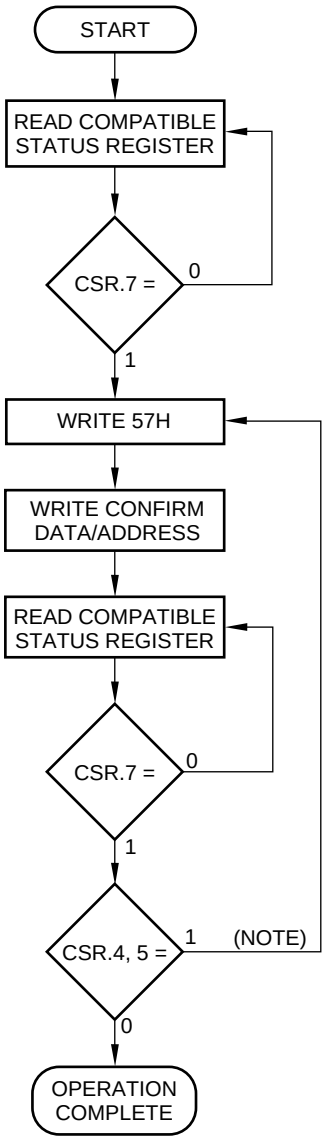
Figure 10. Bank Erase All Unlocked Blocks with Compatible Status Registers



BUS OPERATION	COMMAND	COMMENTS
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Write	Set Write Protect	D = 57H A = X
Write	Set Confirm	D = D0H A = 0FFH (A_9 - A_8 = 0, A_7 - A_0 = 1, Others = X)
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Read		Check CSR.4, 5 1 = Unsuccesful 0 = Successful

NOTE:
If CSR.4, 5 is set, as it is command sequence error, should be cleared before further attempts are initiated.

Upon device power-up or reset is complete, Set Write Protect command must be written to reflect the actual lock-bit status.

Write FFH after the last operation to reset device to Read Array Mode.

See Command Bus Cycle notes for description of codes.

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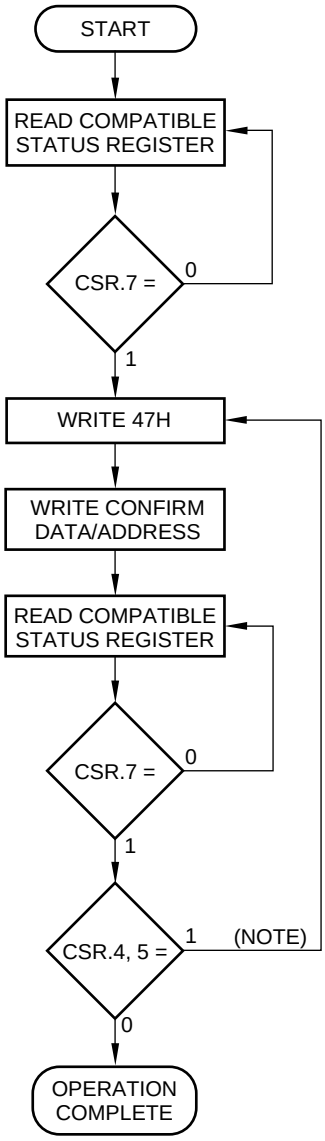
Figure 11. Set Write Protect



BUS OPERATION	COMMAND	COMMENTS
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Write	Reset Write Protect	D = 47H A = X
Write	Reset Confirm	D = D0H A = 0FFH (A_9 - A_8 = 0, A_7 - A_0 = 1, Others = X)
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Read		Check CSR.4, 5 1 = Unsuccesful 0 = Successful

NOTE:
If CSR.4, 5 is set, as it is command sequence error, should be cleared before further attempts are initiated.

Reset Write Protect command enables Write/Erase operation to all blocks.

Write FFH after the last operation to reset device to Read Array Mode.

See Command Bus Cycle notes for description of codes.

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Figure 12. Reset Write Protect

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Temperature under bias ..... -20°C to +80°C

Storage temperature ..... -65°C to +125°C

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
T_A	Operating Temperature, Commercial	0	70.0	°C	Ambient Temperature	1
V_{CC}	V_{CC} with Respect to GND	-0.2	7.0	V		2
V_{PP}	V_{PP} Supply Voltage with Respect to GND	-0.2	7.0	V		2
V	Voltage on any Pin (Except V_{CC}, V_{PP}) with Respect to GND	-0.5	V_{CC} + 0.5	V		2
I	Current into any Non-Supply Pin		±30	mA		
I_{OUT}	Output Short Circuit Current		100.0	mA		3

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is -0.5 V on input/output pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Capacitance

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTE
C_{IN}	Capacitance Looking into an Address/Control Pin	14	20	pF	T_A = 25°C, f = 1.0 MHz	1, 2
C_{OUT}	Capacitance Looking into an Output Pin	18	24	pF	T_A = 25°C, f = 1.0 MHz	1
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications		50	pF	For V_{CC} = 3.3 V ±0.3 V	1
	Equivalent Testing Load Circuit V_{CC} ± 10%		2.5	ns	50 Ω transmission line delay	

NOTE:
1. Sampled, not 100% tested.
2. $\overline{BE}_0$ and $\overline{BE}_1$ have half the value of this.

Timing Nomenclature

For 3.3 V systems use 1.5 V cross point definitions.
Each timing parameter consists of 5 characters. Some common examples are defined below:

t_{CE} t_{ELQV} time (t) from $\overline{BE}$ (E) going low (L) to the outputs (Q) becoming valid (V)

t_{OE} t_{GLQV} time (t) from $\overline{OE}$ (G) going low (L) to the outputs (Q) becoming valid (V)

t_{ACC} t_{AVQV} time (t) from address (A) valid (V) to the outputs (Q) becoming valid (V)

t_{AS} t_{AVWH} time (t) from address (A) valid (V) to $\overline{WE}$ (W) going high (H)

t_{DH} t_{WHDX} time (t) from $\overline{WE}$ (W) going high (H) to when the data (D) can become undefined (X)

	PIN CHARACTERS		PIN STATES
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	$\overline{BE}$ (Byte Enable)[1]	X	Driven, but not necessarily valid
G	$\overline{OE}$ (Output Enable)	Z	High Impedance
W	$\overline{WE}$ (Write Enable)		
V	Any Voltage Level		
3 V	V_{CC} at 3.0 V Min.		

NOTE:
1. $\overline{BE}_X$ means either $\overline{BE}_0$ or $\overline{BE}_1$.

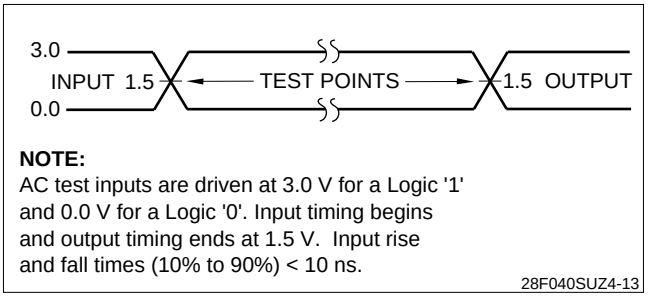


Figure 13. Transient Input/Output Reference Waveform (V_{CC} = 3.3 V)

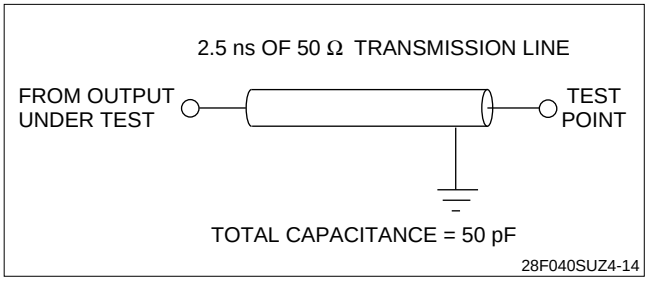


Figure 14. Transient Equivalent Testing Load Circuit (V_{CC} = 3.3 V)

DC Characteristics

V_{CC} = 3.3 V ± 0.3 V, T_A = -20°C to +70°C

Following is the current consumption of one bank. For the current consumption of one device total, please refer to Note 5.

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{IL}	Input Load Current			±2	µA	$V_{CC} = V_{CC}$ MAX., $V_{IN} = V_{CC}$ or GND	1
I_{LO}	Output Leakage Current			±20	µA	$V_{CC} = V_{CC}$ MAX., $V_{IN} = V_{CC}$ or GND	1
I_{CCS}	V_{CC} Standby Current	5		10	µA	$V_{CC} = V_{CC}$ MAX., $\overline{BE}_0$, $\overline{BE}_1 = V_{CC}$ ±0.2 V	1, 4, 5
		0.3		4	mA	$V_{CC} = V_{CC}$ MAX., $\overline{BE}_0$, $\overline{BE}_1 = V_{IH}$	
I_{CCR}[1]	V_{CC} Read Current (10 MHz Operation)			35	mA	$V_{CC} = V_{CC}$ MAX., CMOS: $\overline{BE}_0$, $\overline{BE}_1$ = GND ±0.2 V Inputs = GND ±0.2 V or V_{CC} ±0.2 V, TTL: $\overline{BE}_0$, $\overline{BE}_1 = V_{IL}$, Inputs = V_{IL} or V_{IH}, f = 10 MHz, I_{OUT} = 0 mA	1, 3, 4, 5
I_{CCR}[2]	V_{CC} Read Current (5 MHz Operation)	10		20	mA	$V_{CC} = V_{CC}$ MAX., CMOS: $\overline{BE}_0$, $\overline{BE}_1$ = GND ±0.2 V Inputs = GND ±0.2 V or V_{CC} ±0.2 V, TTL: $\overline{BE}_0$, $\overline{BE}_1 = V_{IL}$, Inputs = V_{IL} or V_{IH}, f = 5 MHz, I_{OUT} = 0 mA	1, 3, 4, 5
I_{CCW}	V_{CC} Write Current	8		12	mA	Byte/Two-Byte Serial Write in Progress	1, 5
I_{CCE}	V_{CC} Block Erase Current	6		12	mA	Block Erase in Progress	1, 5
I_{CCES}	V_{CC} Erase Suspend Current	3		6	mA	$\overline{BE}_0$, $\overline{BE}_1 = V_{IH}$ Block Erase Suspended	1, 2, 5
I_{PPS}	V_{PP} Standby Current	±1		±10	µA	$V_{PP} \leq V_{CC}$	1, 5

DC Characteristics (Continued)

V_{CC} = 3.3 V ± 0.3 V, T_A = -20°C to +70°C

SYMBOL	PARAMETER	TYPE	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{PPR}	V_{PP} Read Current	65		200	µA	$V_{PP} > V_{CC}$	1, 5
I_{PPW}	V_{PP} Write Current	15		35	mA	$V_{PP} = V_{PPH}$, Byte/Two-Byte Serial Write in Progress	1, 5
I_{PPE}	V_{PP} Erase Current	20		40	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress	1, 5
I_{PPES}	V_{PP} Erase Suspend Current	65		200	µA	$V_{PP} = V_{PPH}$, Block Erase Suspended	1, 5
V_{IL}	Input Low Voltage		-0.3	0.8	V		
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V		
V_{OL}	Output Low Voltage			0.4	V	$V_{CC} = V_{CC}$ MIN. and I_{OL} = 4 mA	
V_{OH}^1	Output High Voltage		2.4		V	I_{OH} = -2 mA $V_{CC} = V_{CC}$ MIN.	
V_{OH}^2			V_{CC} - 0.2		V	I_{OH} = 100 µA $V_{CC} = V_{CC}$ MIN.	
V_{PPL}	V_{PP} during Normal Operations		0.0	5.5	V		
V_{PPH}	V_{PP} during Write/Erase Operations	5.0	4.5	5.5	V		
V_{LKO}	V_{CC} Erase/Write Lock Voltage		1.4		V		

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3 V, V_{PP} = 5.0 V, T = 25°C.
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Automatic Power Saving (APS) reduces I_{CCR} to less than 2 mA in Static operation.
4. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL Inputs are either V_{IL} or V_{IH}.
5. These are the values of the current which is consumed within one bank area. The value for the bank0 and bank1 should be added in order to calculate the value for the whole chip. If the bank0 is in write state and bank1 is in read state, the $I_{CC} = I_{CCW} + I_{CCR}$. If both banks are in standby mode, the value for the device is 2 times the value in the above table.

AC Characteristics - Read Only Operations[1]

V_{CC} = 3.3 V ± 0.3 V, T_A = -20°C to +70°C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Read Cycle Time	150		ns	
t_{AVGL}	Address Setup to $\overline{OE}$ Going Low	0		ns	3
t_{AVQV}	Address to Output Delay		150	ns	
t_{ELQV}	$\overline{BE}_0$, $\overline{BE}_1$ to Output Delay		150	ns	2
t_{GLQV}	$\overline{OE}$ to Output Delay		50	ns	2
t_{ELQX}	$\overline{BE}_0$, $\overline{BE}_1$ to Output in Low Z	0		ns	3
t_{EHQZ}	$\overline{BE}_0$, $\overline{BE}_1$ to Output in High Z		55	ns	3
t_{GLQX}	$\overline{OE}$ to Output in Low Z	0		ns	3
t_{GHQZ}	$\overline{OE}$ to Output in High Z		40	ns	3
t_{OH}	Output Hold from Address, $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ change, whichever occurs first	0		ns	3

AC Characteristics - Read Only Operations[1] (Continued)

V_{CC} = 2.85 V ± 0.15 V, T_A = -20°C to +70°C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Read Cycle Time	190		ns	
t_{AVGL}	Address Setup to $\overline{OE}$ Going Low	0		ns	3
t_{AVQV}	Address to Output Delay		190	ns	
t_{ELQV}	$\overline{BE}_0$, $\overline{BE}_1$ to Output Delay		190	ns	2
t_{GLQV}	$\overline{OE}$ to Output Delay		65	ns	2
t_{ELQX}	$\overline{BE}_0$, $\overline{BE}_1$ to Output in Low Z	0		ns	3
t_{EHQZ}	$\overline{BE}_0$, $\overline{BE}_1$ to Output in High Z		70	ns	3
t_{GLQX}	$\overline{OE}$ to Output in Low Z	0		ns	3
t_{GHQZ}	$\overline{OE}$ to Output in High Z		55	ns	3
t_{OH}	Output Hold from Address, $\overline{BE}_0$, $\overline{BE}_1$ or $\overline{OE}$ change, whichever occurs first	0		ns	3

NOTES:
1. See AC Input/Output Reference Waveforms for timing measurements, Figure 4.
2. $\overline{OE}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{BE}_0$, $\overline{BE}_1$ without impact on t_{ELQV}.
3. Sampled, not 100% tested.

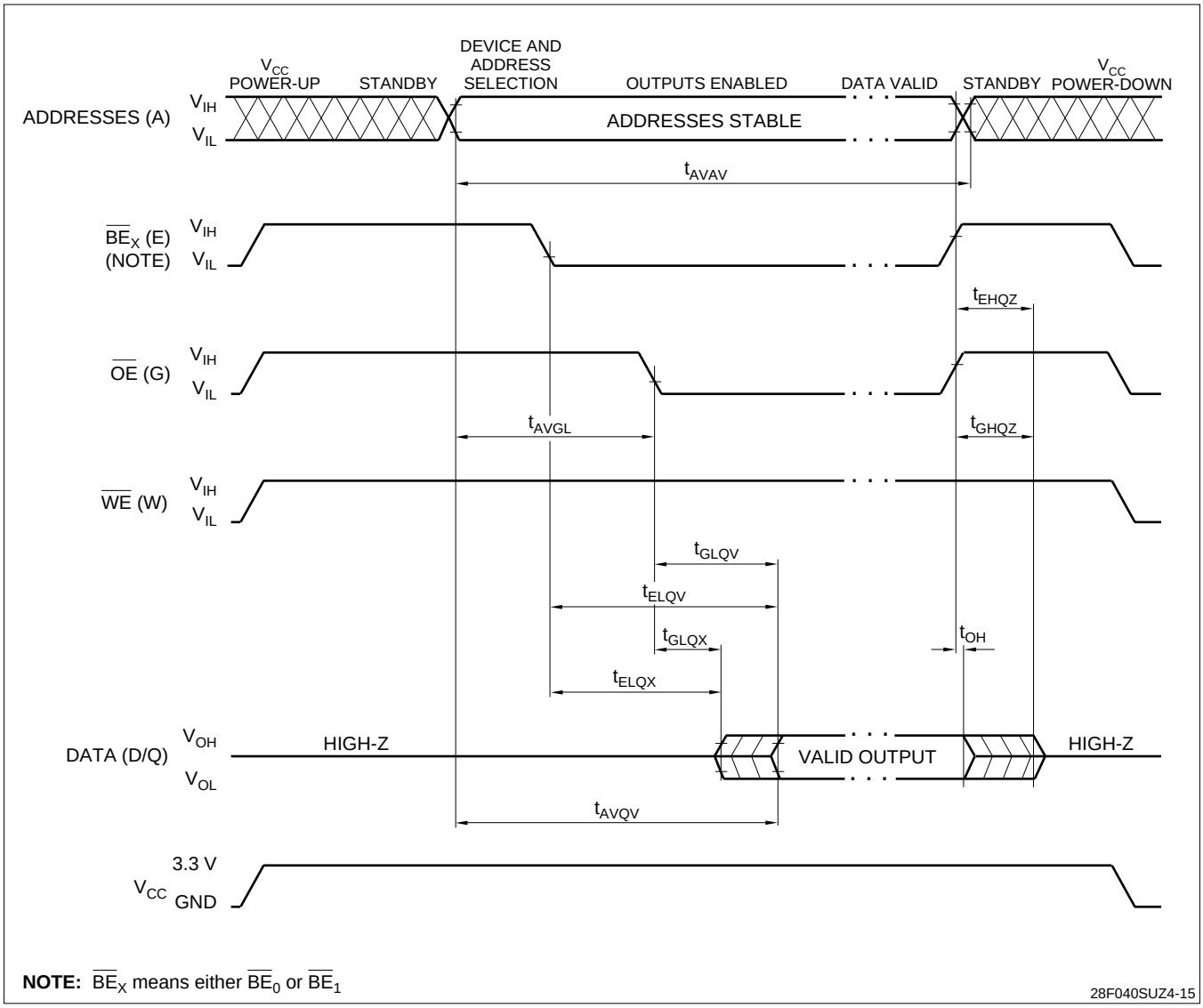


Figure 15. Read Timing Waveforms

POWER-UP AND RESET TIMINGS

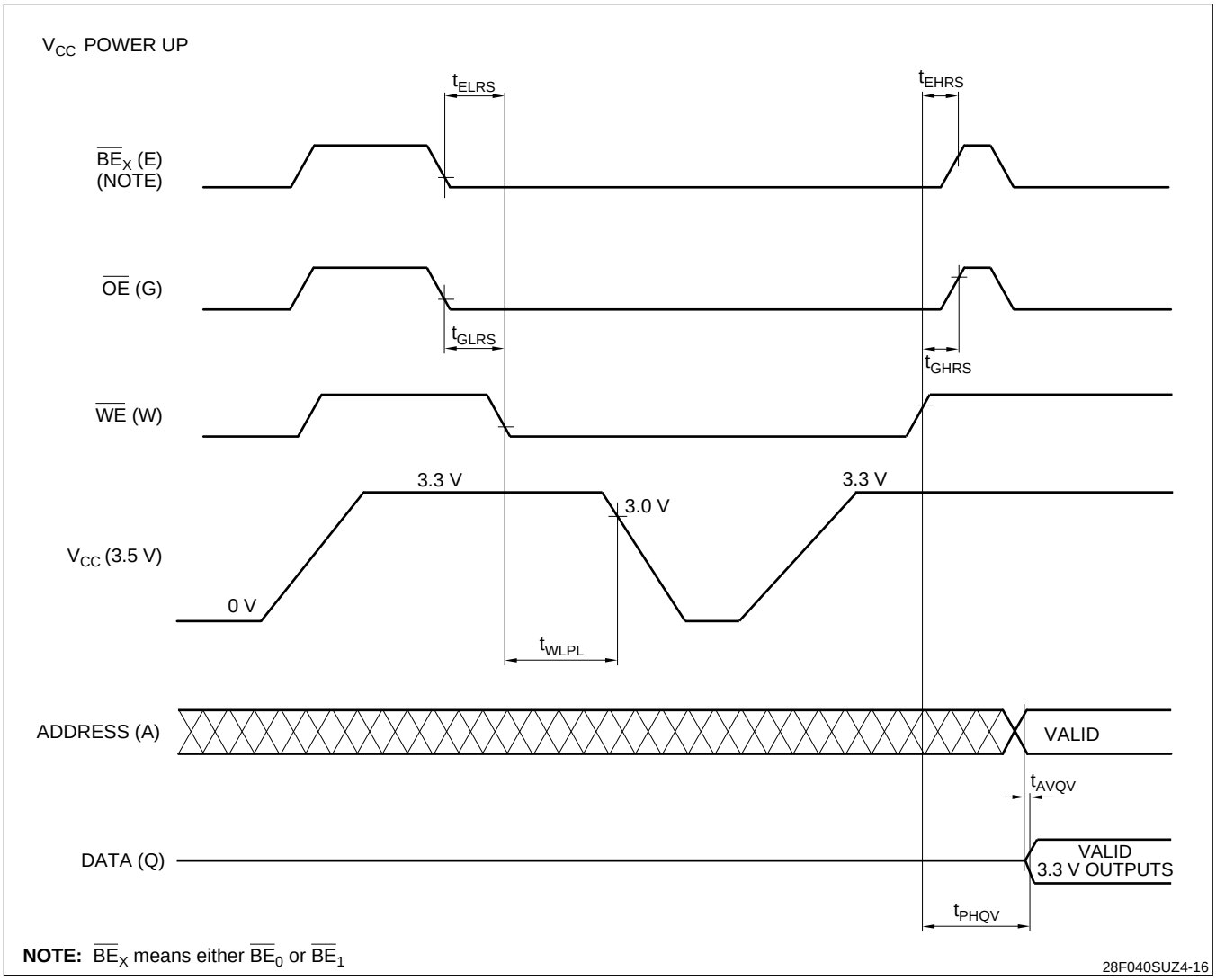


Figure 16. V_{CC} Power-Up and $\overline{RP}$ Reset Waveforms

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{WLPL}	$\overline{WE}$ Low to V_{CC} at 3.0 V MIN.	5		µs	1
t_{AVQV}	Address Valid to Data Valid for V_{CC} = 3.3 V ± 0.3 V		150	ns	2
t_{PHQV}	$\overline{WE}$ High to Data Valid for V_{CC} = 3.3 V ± 0.3 V		500	ns	2
t_{ELRS}	$\overline{BE}_0$ and $\overline{BE}_1$ Setup to WE Going Low	100		ns	
t_{GLRS}	$\overline{OE}$ Setup to $\overline{WE}$ Going Low	100		ns	
t_{EHRS}	$\overline{BE}_0$ and $\overline{BE}_1$ Hold from $\overline{WE}$ Going High	100		ns	
t_{GHRS}	$\overline{OE}$ Hold from $\overline{WE}$ Going High	100		ns	

NOTES:
$\overline{BE}_0$, $\overline{BE}_1$ and $\overline{OE}$ must be set high once after power-up. $\overline{BE}_0$ and $\overline{BE}_1$ must not be set low at the same time.

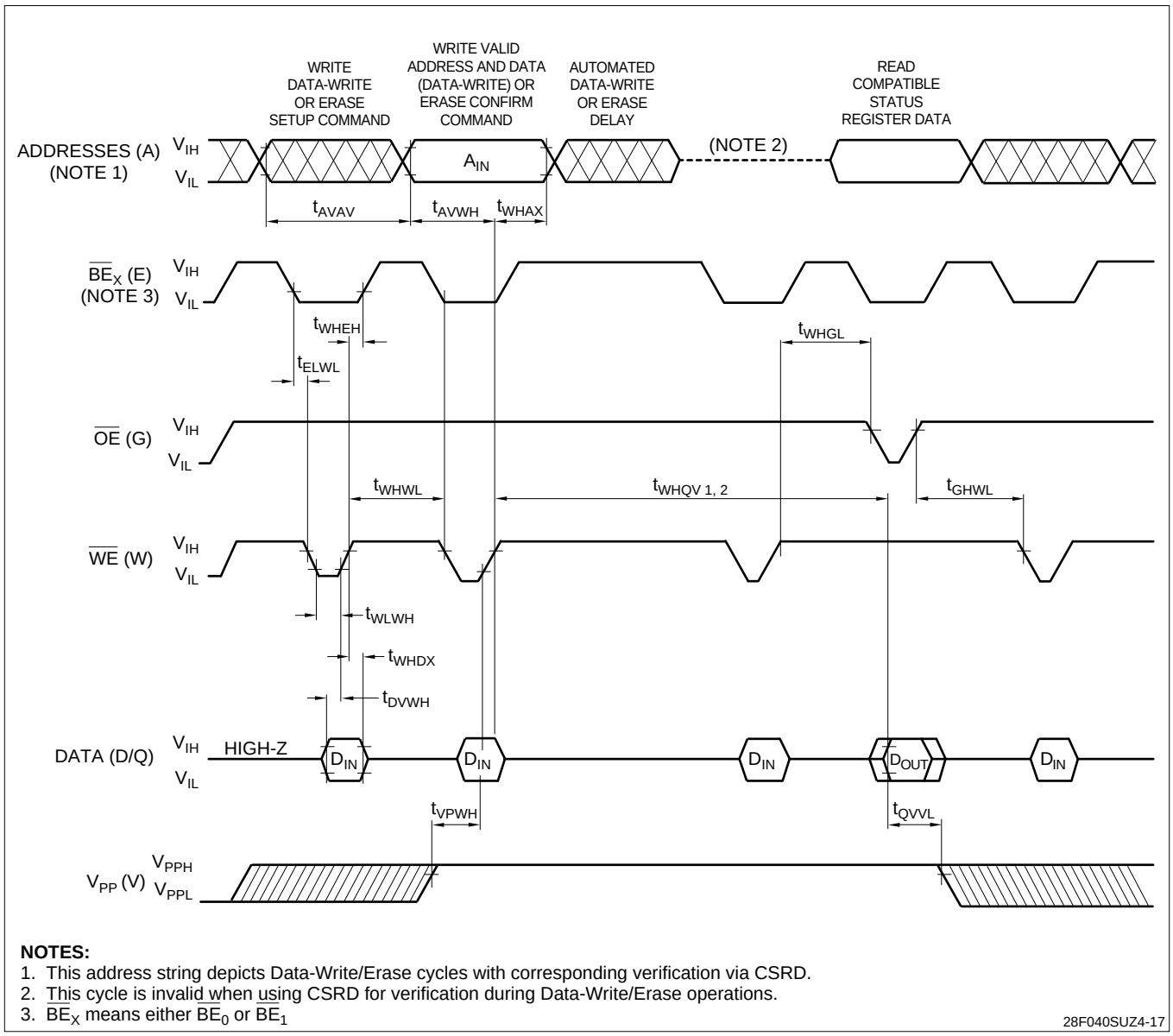
1. Chip reset is enabled when the low state of all $\overline{BE}_0$ (or $\overline{BE}_1$), $\overline{OE}$ and $\overline{WE}$ exceeds 5 µs. Especially when you will power on the chip, execute an above chip reset sequence for a protection from noise. All $\overline{BE}_0$ (or $\overline{BE}_1$), $\overline{OE}$ and $\overline{WE}$ must not be low, except for the purpose of chip reset.
2. These values are shown for 3.3 V V_{CC} operation. Refer to the AC Characteristics Read Only Operations also.

AC Characteristics for $\overline{WE}$ - Controlled Command Write Operations[1]

V_{CC} = 3.25 V ± 0.35 V, T_A = -20°C to +70°C

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Write Cycle Time		150		ns	
t_{VPWH}	V_{PP} Set up to $\overline{WE}$ Going High		100		ns	3
t_{ELWL}	$\overline{BE}_0$ and $\overline{BE}_1$ Setup to $\overline{WE}$ Going Low		0		ns	
t_{AVWH}	Address Setup to $\overline{WE}$ Going High		110		ns	2, 6
t_{DVWH}	Data Setup to $\overline{WE}$ Going High		110		ns	2, 6
t_{WLWH}	$\overline{WE}$ Pulse Width		110		ns	
t_{WHDX}	Data Hold from $\overline{WE}$ High		10		ns	2
t_{WHAX}	Address Hold from $\overline{WE}$ High		10		ns	2
t_{WHEH}	$\overline{BE}_0$ and $\overline{BE}_1$ Hold from $\overline{WE}$ High		10		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width High		75		ns	
t_{GHWL}	Read Recovery before Write		0		ns	
t_{WHGL}	Write Recovery before Read		120		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data		0		µs	
$t_{WHQV}{}^1$	Duration of Byte Write Operation	20	8	250	µs	4, 5, 7
$t_{WHQV}{}^2$	Duration of Block Erase Operation		0.3		s	4

NOTES:
1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of $\overline{WE}$ for all Command Write operations.
7. The maximum value of byte write time is the maximum write time inside the chip. It is not the time until the whole writing procedure is completed properly. It is necessary to check CSR to see if the writing procedure is properly completed.



NOTES:
1. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
2. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
3. $\overline{BE}_X$ means either $\overline{BE}_0$ or $\overline{BE}_1$

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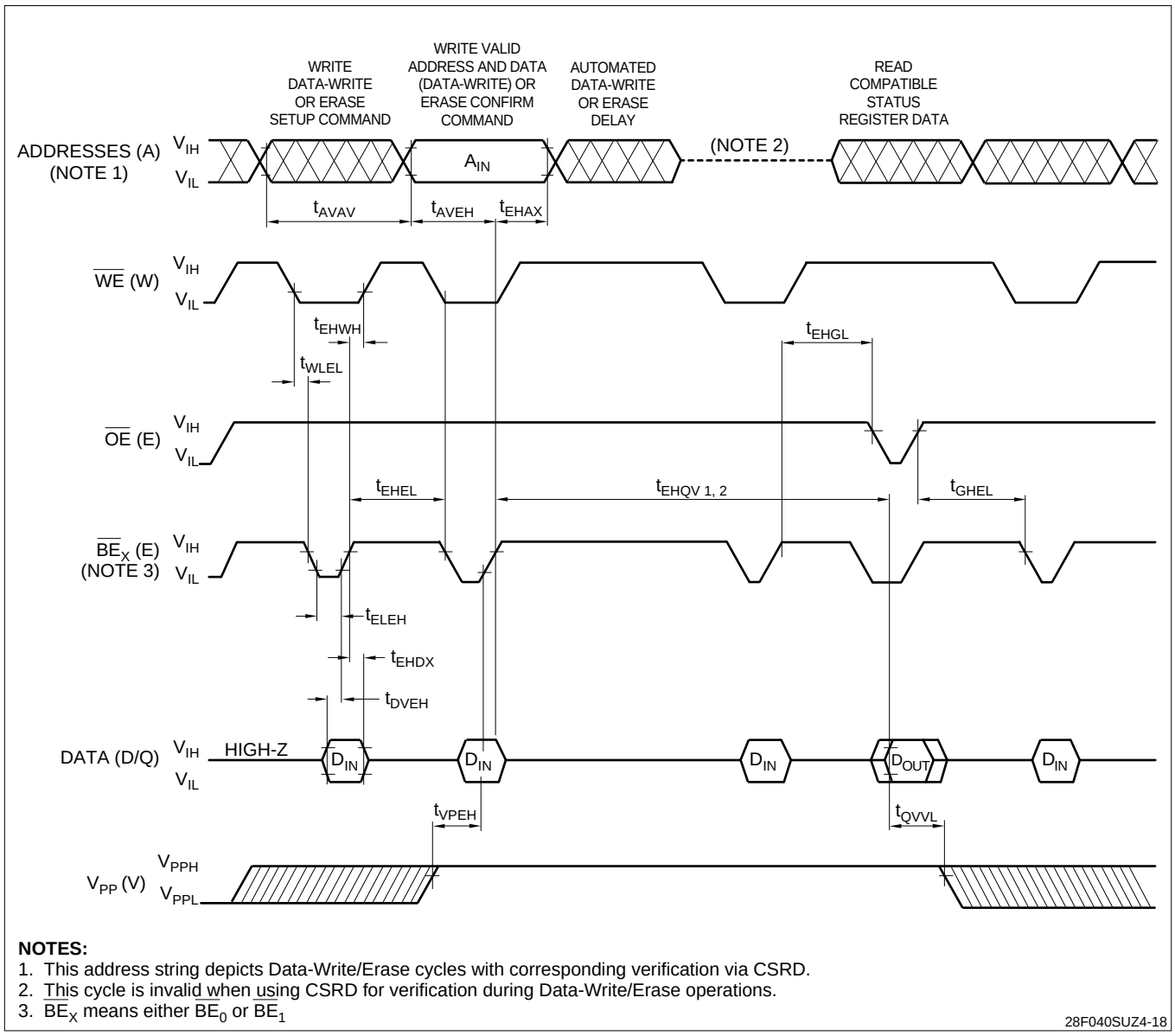
Figure 17. Waveforms for Command Write Operations

AC Characteristics for $\overline{BE}$ - Controlled Command Write Operations[2]

V_{CC} = 3.25 V ± 0.35 V, T_A = -20°C to +70°C

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Write Cycle Time		150		ns	
t_{VPEH}	V_{PP} Set up to $\overline{BE}_0$ or $\overline{BE}_1$ Going High		100		ns	3
t_{WLEL}	$\overline{WE}$ Setup to $\overline{BE}_0$ or $\overline{BE}_1$ Going Low		0		ns	
t_{AVEH}	Address Setup to $\overline{BE}_0$ or $\overline{BE}_1$ Going High		110		ns	2, 6
t_{DVEH}	Data Setup to $\overline{BE}_0$ or $\overline{BE}_1$ Going High		110		ns	2, 6
t_{ELEH}	$\overline{BE}_0$ or $\overline{BE}_1$ Pulse Width		110		ns	
t_{EHDX}	Data Hold from $\overline{BE}_0$ or $\overline{BE}_1$ High		10		ns	2
t_{EHAX}	Address Hold from $\overline{BE}_0$ or $\overline{BE}_1$ High		10		ns	2
t_{EHWH}	$\overline{WE}$ Hold from $\overline{BE}_0$ or $\overline{BE}_1$ High		10		ns	
t_{EHEL}	$\overline{BE}_0$ or $\overline{BE}_1$ Pulse Width High		75		ns	
t_{GHEL}	Read Recovery before Write		0		ns	
t_{EHGL}	Write Recovery before Read		120		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data		0		µs	
t_{EHQV}^1	Duration of Byte Write Operation	20	8	250	µs	4, 5, 7
t_{EHQV}^2	Duration of Block Erase Operation		0.3		s	4

NOTES:
1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Byte Write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of $\overline{BE}_0$ or $\overline{BE}_1$ for all Command Write operations.
7. The MAX. value of byte write time is the maximum wrtie time inside the chip. It is not the time until the whole writing procedure is completed properly. It is necessary to check CSR to see if the writing procedure is properly completed.



NOTES:
1. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
2. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
3. $\overline{BE}_X$ means either $\overline{BE}_0$ or $\overline{BE}_1$

28F040SUZ4-18

Figure 18. Alternate AC Waveforms for Command Write Operations

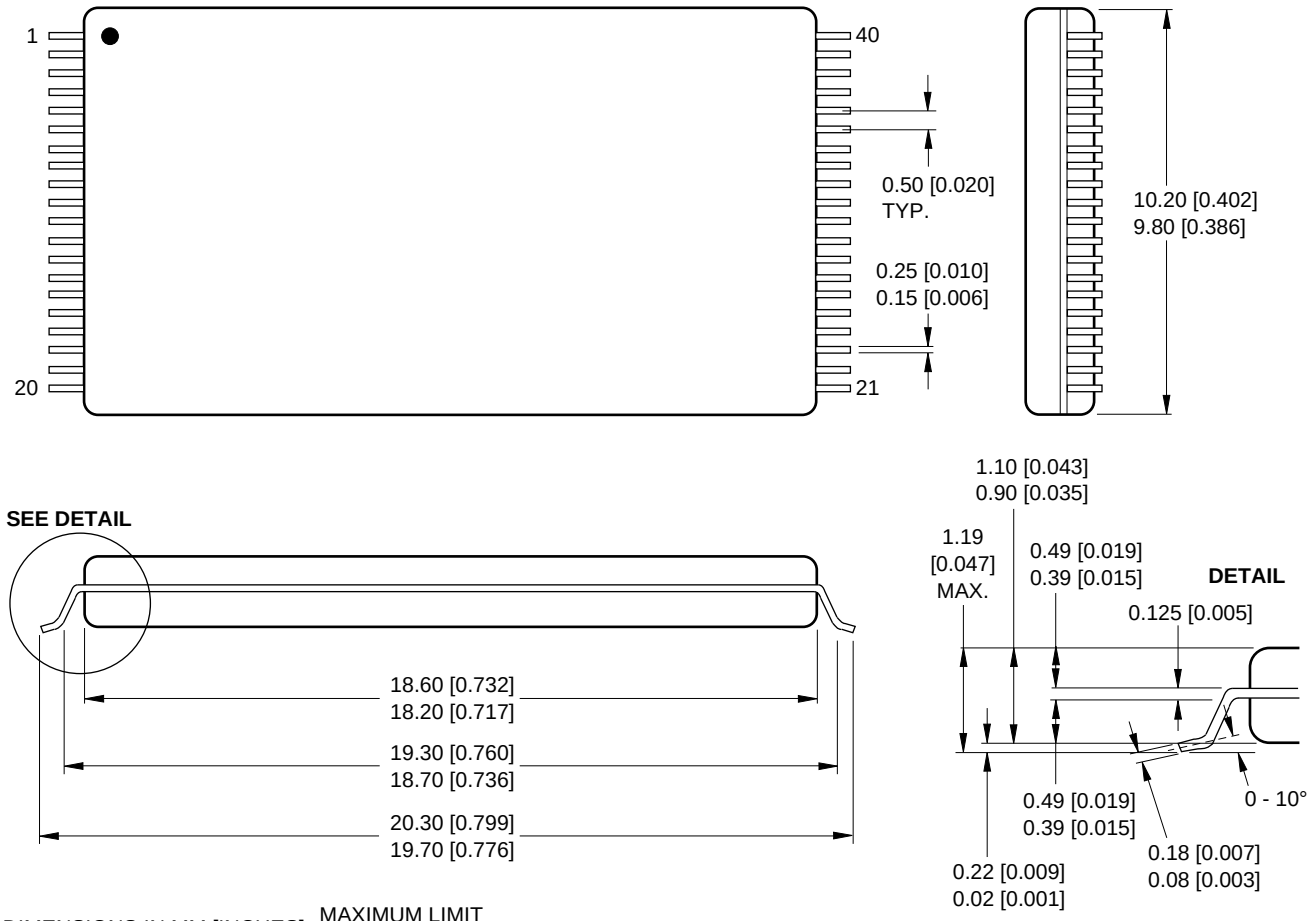
Erase and Byte Write Performance

V_{CC} = 3.25 V ± 0.35 V, T_A = -20°C to +70°C

SYMBOL	PARAMETER	TYP.(1)	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
t_{WHRH}^1	Byte Write Time	20		250	µs		2, 3
t_{WHRH}^2	Two-Byte Serial Write Time	34			µs		2
t_{WHRH}^3	16KB Block Write Time	0.33		1.0	s	Byte Write Mode	2
t_{WHRH}^4	16KB Block Write Time	0.28		1.0	s	Two-Byte Serial Write Mode	2
	Block Erase Time (16KB)	0.8		10	s		2
	2M Bit Bank Erase Time	9 - 15			s		2, 4

NOTES:
1. 25°C, V_{PP} = 5.0 V
2. Excludes System-Level Overhead. It actually indicates the time from input write/erase command until bit7 of status register becomes ready (WSMS = 0).
3. The MAX. value of byte write time is the maximum write time inside the chip. It is not the time until the whole writing procedure is completed properly. It is necessary to check CSR to see if the writing procedure is properly completed.
4. Depends on the number of protected blocks.

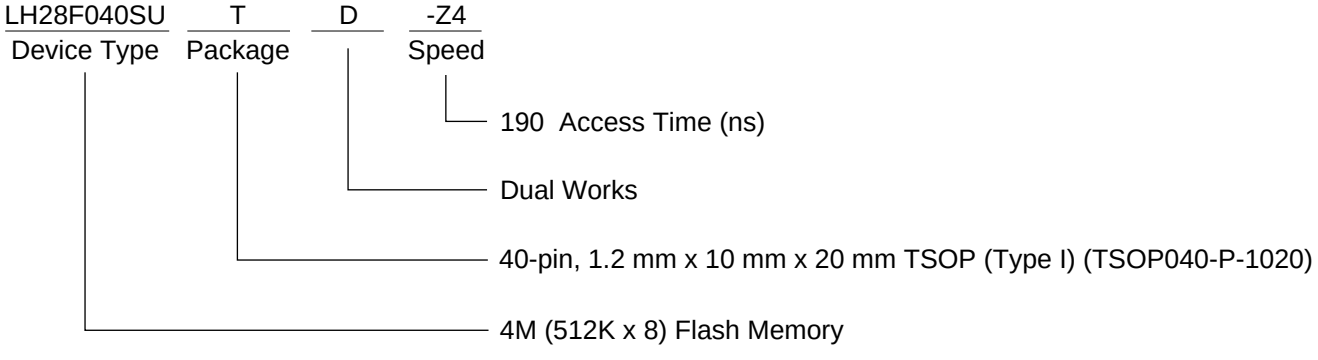
40TSOP (TSOP040-P-1020)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40TSOP

ORDERING INFORMATION



Example: LH28F040SUT-Z4 (4M (512K x 8) Flash Memory, 190 ns, 40-pin TSOP)

28F040SUZ4-19

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