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PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH28F320BJE-PTTL90

Flash Memory

32M (2M × 16/4M × 8)

(Model No.: LHF32J02)

Spec No.: EL124011

Issue Date: April 17, 2000

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LH28F320BJE-PTTL90
32M-BIT (2Mbit ×16 / 4Mbit ×8)
Boot Block Flash MEMORY

- Low Voltage Operation
  - $V_{CC}=V_{CCW}=2.7V\text{-}3.6V$ Single Voltage
- OTP(One Time Program) Block
  - 3963 word + 4 word Program only array
- User-Configurable ×8 or ×16 Operation
- High-Performance Read Access Time
  - 90ns($V_{CC}=2.7V\text{-}3.6V$)
- Operating Temperature
  - 0°C to +70°C
- Low Power Management
  - Typ. 4µA ($V_{CC}=3.0V$) Standby Current
  - Automatic Power Savings Mode Decreases I_{CCR} in Static Mode
  - Typ. 120µA ($V_{CC}=3.0V$, $T_A=+25°C$, f=32kHz) Read Current
- Optimized Array Blocking Architecture
  - Two 4K-word (8K-byte) Boot Blocks
  - Six 4K-word (8K-byte) Parameter Blocks
  - Sixty-three 32K-word (64K-byte) Main Blocks
  - Top Boot Location
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with $V_{CCW}\leq V_{CCWLK}$
  - Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration Lockout during Power Transitions
  - Block Locking with Command and WP#
  - Permanent Locking
- Automated Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration
  - Command User Interface (CUI)
  - Status Register (SR)
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP
- ETOX^{TM*} Nonvolatile Flash Technology
- CMOS Process (P-type silicon substrate)
- Not designed or rated as radiation hardened

SHARP's LH28F320BJE-PTTL90 Flash memory is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications.

LH28F320BJE-PTTL90 can operate at $V_{CC}=2.7V\text{-}3.6V$ and $V_{CCW}=2.7V\text{-}3.6V$ or 11.7V-12.3V. Its low voltage operation capability realize battery life and suits for cellular phone application.

Its Boot, Parameter and Main-blocked architecture, low voltage and extended cycling provide for highly flexible component suitable for portable terminals and personal computers. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications.

For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F320BJE-PTTL90 offers four levels of protection: absolute protection with $V_{CCW}\leq V_{CCWLK}$, selective hardware block locking or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F320BJE-PTTL90 is manufactured on SHARP's 0.25µm ETOX^{TM*} process technology. It come in industry-standard package: the 48-lead TSOP, ideal for board constrained applications.

*ETOX is a trademark of Intel Corporation.

1 INTRODUCTION

This datasheet contains LH28F320BJE-PTTL90 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4 and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 Features

Key enhancements of LH28F320BJE-PTTL90 boot block Flash memory are:

- Single low voltage operation
- Low power consumption
- Enhanced Suspend Capabilities
- Boot Block Architecture

Please note following:

- V_{CCWLK} has been lowered to 1.0V to support 2.7V-3.6V block erase, full chip erase, word/byte write and lock-bit configuration operations. The V_{CCW} voltage transitions to GND is recommended for designs that switch V_{CCW} off during read operation.

1.2 Product Overview

The LH28F320BJE-PTTL90 is a high-performance 32M-bit Boot Block Flash memory organized as 2M-word of 16 bits or 4M-byte of 8 bits. The 2M-word/4M-byte of data is arranged in two 4K-word/8K-byte boot blocks, six 4K-word/8K-byte parameter blocks and sixty-three 32K-word/64K-byte main blocks which are individually erasable, lockable and unlockable in-system. The memory map is shown in Figure 3.

The dedicated V_{CCW} pin gives complete data protection when $V_{CCW} \leq V_{CCWLK}$.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, word/byte write and lock-bit configuration operations.

A block erase operation erases one of the device's 32K-word/64K-byte blocks typically within 1.2s (3V V_{CC}, 3V V_{CCW}), 4K-word/8K-byte blocks typically within 0.6s (3V V_{CC}, 3V V_{CCW}) independent of other blocks. Each block can be independently erased minimum 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word/byte increments of the device's 32K-word blocks typically within 33μs (3V V_{CC}, 3V V_{CCW}), 64K-byte blocks typically within 31μs (3V V_{CC}, 3V V_{CCW}), 4K-word blocks typically within 36μs (3V V_{CC}, 3V V_{CCW}), 8K-byte blocks typically within 32μs (3V V_{CC}, 3V V_{CCW}). Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, seventy-one block lock-bits, a permanent lock-bit and WP# pin, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and word/byte write operations, while the permanent lock-bit gates block lock-bit modification and locked block alternation. Lock-bit configuration operations (Set Block Lock-Bit, Set Permanent Lock-Bit and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, full chip erase, word/byte write or lock-bit configuration operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase, full chip erase, word/byte write or lock-bit configuration. RY/BY#-high Z indicates that the WSM is ready for a new command, block erase is suspended (and word/byte write is inactive), word/byte write is suspended, or the device is in reset mode.

The access time is 90ns (t_{AVQV}) over the operating temperature range (0°C to +70°C) and V_{CC} supply voltage range of 2.7V-3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 4µA (CMOS) at 3.0V V_{CC}.

When CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, reset mode is enabled which minimizes power consumption and provides write protection. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programed "1".

- ·Program "0" for the bit in which you want to change data from "1" to "0".
- ·Program "1" for the bit which has already been programmed "0".

For example, changing data from "10111101" to "10111100" requires "11111110" programming.

1.3 Product Description

1.3.1 Package Pinout

LH28F320BJE-PTTL90 Boot Block Flash memory is available in 48-lead TSOP package (see Figure 2).

1.3.2 Block Organization

This product features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times. For the address locations of the blocks, see the memory map in Figure 3.

Boot Blocks: The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. This boot block 4K words (4,096words) features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the V_{CCW}, RP#, WP# pins and block lock-bit.

Parameter Blocks: The boot block architecture includes parameter blocks to facilitate storage of frequently update small parameters that would normally require an EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each boot block component contains six parameter blocks of 4K words (4,096 words) each. The protection of the parameter block is controlled using a combination of the V_{CCW}, RP# and block lock-bit.

Main Blocks: The reminder is divided into main blocks for data or code storage. Each 32M-bit device contains sixty-three 32K words (32,768 words) blocks. The protection of the main block is controlled using a combination of the V_{CCW}, RP# and block lock-bit.

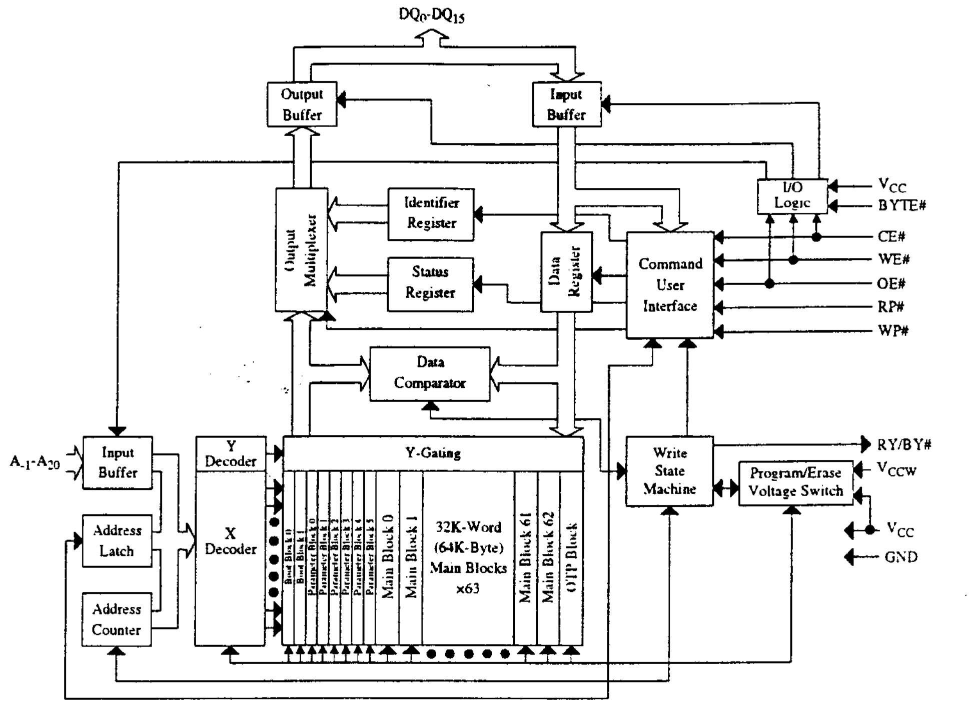

DQ0-DQ15
Output Buffer
Input Buffer
I/O Logic
VCC
BYTE#
Identifier Register
Output Multiplexer
Status Register
Data Register
Command User Interface
CE#
WE#
OE#
RP#
WP#
Data Comparator
A-1-A20
Input Buffer
Address Latch
Address Counter
Y Decoder
X Decoder
Y-Gating
Boot Block 0
Boot Block 1
Parameter Block 0
Parameter Block 1
Parameter Block 2
Parameter Block 3
Parameter Block 4
Parameter Block 5
Main Block 0
Main Block 1
32K-Word (64K-Byte) Main Blocks x63
Main Block 61
Main Block 62
OTP Block
Write State Machine
Program/Erase Voltage Switch
RY/BY#
VCCW
VCC
GND

Figure 1. Block Diagram

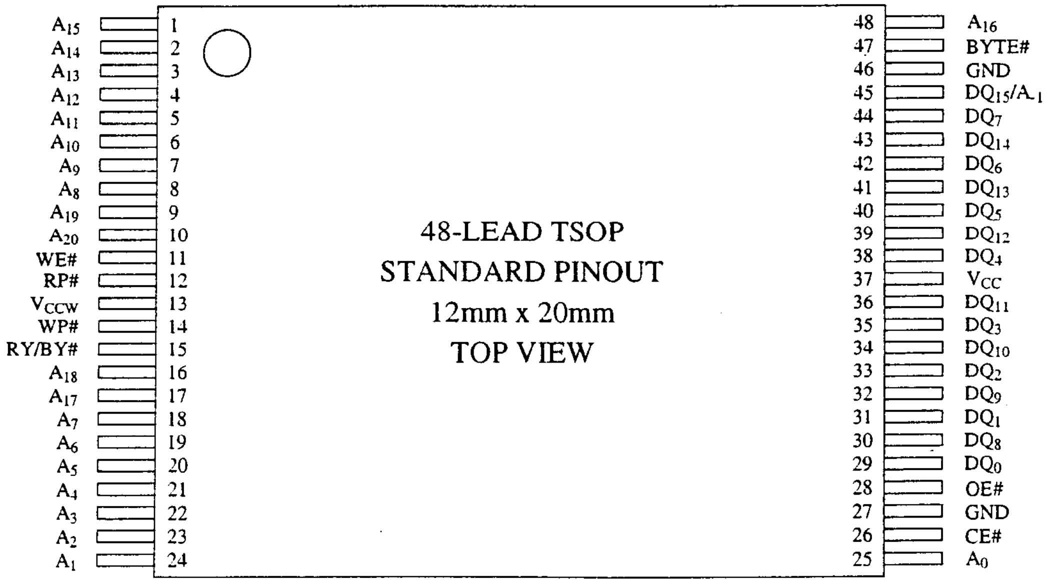

48-LEAD TSOP
STANDARD PINOUT
12mm x 20mm
TOP VIEW
A15 1
A14 2
A13 3
A12 4
A11 5
A10 6
A9 7
A8 8
A19 9
A20 10
WE# 11
RP# 12
VCCW 13
WP# 14
RY/BY# 15
A18 16
A17 17
A7 18
A6 19
A5 20
A4 21
A3 22
A2 23
A1 24
48 A16
47 BYTE#
46 GND
45 DQ15/A-1
44 DQ7
43 DQ14
42 DQ6
41 DQ13
40 DQ5
39 DQ12
38 DQ4
37 VCC
36 DQ11
35 DQ3
34 DQ10
33 DQ2
32 DQ9
31 DQ1
30 DQ8
29 DQ0
28 OE#
27 GND
26 CE#
25 A0

Figure 2. TSOP 48-Lead Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_{-1} A_0-A_{20}	INPUT	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A_{-1}: Lower address input while BYTE# is V_{IL}. A_{-1} pin changes DQ_{15} pin while BYTE# is V_{IH}. A_{15}-A_{20}: Main Block Address. A_{12}-A_{20}: Boot and Parameter Block Address.
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ_8-DQ_{15} pins are not used while byte mode (BYTE#=V_{IL}). Then, DQ_{15} pin changes A_{-1} address input.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	RESET: Resets the device internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from reset mode sets the device to read array mode. RP# must be V_{IL} during power-up.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL}, boot blocks cannot be written or erased. When WP# is V_{IH}, locked boot blocks can not be written or erased. WP# is not affected parameter and main blocks.
BYTE#	INPUT	BYTE ENABLE: BYTE# V_{IL} places device in byte mode (×8). All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. BYTE# V_{IH} places the device in word mode (×16), and turns off the A_{-1} input buffer.
RY/BY#	OPEN DRAIN OUTPUT	READY/BUSY#: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, full chip erase, word/byte write or lock-bit configuration). RY/BY#-high Z indicates that the WSM is ready for new commands, block erase is suspended, and word/byte write is inactive, word/byte write is suspended, or the device is in reset mode.
V_{CCW}	SUPPLY	BLOCK ERASE, FULL CHIP ERASE, WORD/BYTE WRITE OR LOCK-BIT CONFIGURATION POWER SUPPLY: For erasing array blocks, writing words/bytes or configuring lock-bits. With $V_{CCW} \leq V_{CCWLK}$, memory contents cannot be altered. Block erase, full chip erase, word/byte write and lock-bit configuration with an invalid V_{CCW} (see 6.2.3 DC Characteristics) produce spurious results and should not be attempted. Applying 12V±0.3V to V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{CCW} may be connected to 12V±0.3V for a total of 80 hours maximum.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY: Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see 6.2.3 DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.

Top Boot

$[A_{20}$-$A_0]$			$[A_{20}$-$A_{-1}]$
1FFFFF 1FF000	4KW/8KB Boot Block	0	3FFFFF 3FE000
1FEFFF 1FE000	4KW/8KB Boot Block	1	3FDFFF 3FC000
1FDFFF 1FD000	4KW/8KB Parameter Block	0	3FBFFF 3FA000
1FCFFF 1FC000	4KW/8KB Parameter Block	1	3F9FFF 3F8000
1FBFFF 1FB000	4KW/8KB Parameter Block	2	3F7FFF 3F6000
1FAFFF 1FA000	4KW/8KB Parameter Block	3	3F5FFF 3F4000
1F9FFF 1F9000	4KW/8KB Parameter Block	4	3F3FFF 3F2000
1F8FFF 1F8000	4KW/8KB Parameter Block	5	3F1FFF 3F0000
1F7FFF 1F0000	32KW/64KB Main Block	0	3EFFFF 3E0000
1EFFFF 1E8000	32KW/64KB Main Block	1	3DFFFF 3D0000
1E7FFF 1E0000	32KW/64KB Main Block	2	3CFFFF 3C0000
1DFFFF 1D8000	32KW/64KB Main Block	3	3BFFFF 3B0000
1D7FFF 1D0000	32KW/64KB Main Block	4	3AFFFF 3A0000
1CFFFF 1C8000	32KW/64KB Main Block	5	39FFFF 390000
1C7FFF 1C0000	32KW/64KB Main Block	6	38FFFF 380000
1BFFFF 1B8000	32KW/64KB Main Block	7	37FFFF 370000
1B7FFF 1B0000	32KW/64KB Main Block	8	36FFFF 360000
1AFFFF 1A8000	32KW/64KB Main Block	9	35FFFF 350000
1A7FFF 1A0000	32KW/64KB Main Block	10	34FFFF 340000
19FFFF 198000	32KW/64KB Main Block	11	33FFFF 330000
197FFF 190000	32KW/64KB Main Block	12	32FFFF 320000
18FFFF 188000	32KW/64KB Main Block	13	31FFFF 310000
187FFF 180000	32KW/64KB Main Block	14	30FFFF 300000
17FFFF 178000	32KW/64KB Main Block	15	2FFFFF 2F0000
177FFF 170000	32KW/64KB Main Block	16	2EFFFF 2E0000
16FFFF 168000	32KW/64KB Main Block	17	2DFFFF 2D0000
167FFF 160000	32KW/64KB Main Block	18	2CFFFF 2C0000
15FFFF 158000	32KW/64KB Main Block	19	2BFFFF 2B0000
157FFF 150000	32KW/64KB Main Block	20	2AFFFF 2A0000
14FFFF 148000	32KW/64KB Main Block	21	29FFFF 290000
147FFF 140000	32KW/64KB Main Block	22	28FFFF 280000
13FFFF 138000	32KW/64KB Main Block	23	27FFFF 270000
137FFF 130000	32KW/64KB Main Block	24	26FFFF 260000
12FFFF 128000	32KW/64KB Main Block	25	25FFFF 250000
127FFF 120000	32KW/64KB Main Block	26	24FFFF 240000
11FFFF 118000	32KW/64KB Main Block	27	23FFFF 230000
117FFF 110000	32KW/64KB Main Block	28	22FFFF 220000
10FFFF 108000	32KW/64KB Main Block	29	21FFFF 210000
107FFF 100000	32KW/64KB Main Block	30	20FFFF 200000

$[A_{20}$-$A_0]$			$[A_{20}$-$A_{-1}]$
0FFFFF 0F8000	32KW/64KB Main Block	31	1FFFFF 1F0000
0F7FFF 0F0000	32KW/64KB Main Block	32	1EFFFF 1E0000
0EFFFF 0E8000	32KW/64KB Main Block	33	1DFFFF 1D0000
0E7FFF 0E0000	32KW/64KB Main Block	34	1CFFFF 1C0000
0DFFFF 0D8000	32KW/64KB Main Block	35	1BFFFF 1B0000
0D7FFF 0D0000	32KW/64KB Main Block	36	1AFFFF 1A0000
0CFFFF 0C8000	32KW/64KB Main Block	37	19FFFF 190000
0C7FFF 0C0000	32KW/64KB Main Block	38	18FFFF 180000
0BFFFF 0B8000	32KW/64KB Main Block	39	17FFFF 170000
0B7FFF 0B0000	32KW/64KB Main Block	40	16FFFF 160000
0AFFFF 0A8000	32KW/64KB Main Block	41	15FFFF 150000
0A7FFF 0A0000	32KW/64KB Main Block	42	14FFFF 140000
09FFFF 098000	32KW/64KB Main Block	43	13FFFF 130000
097FFF 090000	32KW/64KB Main Block	44	12FFFF 120000
08FFFF 088000	32KW/64KB Main Block	45	11FFFF 110000
087FFF 080000	32KW/64KB Main Block	46	10FFFF 100000
07FFFF 078000	32KW/64KB Main Block	47	0FFFFF 0F0000
077FFF 070000	32KW/64KB Main Block	48	0EFFFF 0E0000
06FFFF 068000	32KW/64KB Main Block	49	0DFFFF 0D0000
067FFF 060000	32KW/64KB Main Block	50	0CFFFF 0C0000
05FFFF 058000	32KW/64KB Main Block	51	0BFFFF 0B0000
057FFF 050000	32KW/64KB Main Block	52	0AFFFF 0A0000
04FFFF 048000	32KW/64KB Main Block	53	09FFFF 090000
047FFF 040000	32KW/64KB Main Block	54	08FFFF 080000
03FFFF 038000	32KW/64KB Main Block	55	07FFFF 070000
037FFF 030000	32KW/64KB Main Block	56	06FFFF 060000
02FFFF 028000	32KW/64KB Main Block	57	05FFFF 050000
027FFF 020000	32KW/64KB Main Block	58	04FFFF 040000
01FFFF 018000	32KW/64KB Main Block	59	03FFFF 030000
017FFF 010000	32KW/64KB Main Block	60	02FFFF 020000
00FFFF 008000	32KW/64KB Main Block	61	01FFFF 010000
007FFF 000000	32KW/64KB Main Block	62	00FFFF 000000

Figure 3. Memory Map

2 PRINCIPLES OF OPERATION

The LH28F320BJE-PTTL90 Flash memory includes an on-chip WSM to manage block erase, full chip erase, word/byte write and lock-bit configuration functions. It allows for: fixed power supplies during block erase, full chip erase, word/byte write and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from reset mode (see section 3 Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{CCW} voltage. High voltage on V_{CCW} enables successful block erase, full chip erase, word/byte write and lock-bit configurations. All functions associated with altering memory contents–block erase, full chip erase, word/byte write, lock-bit configuration, status and identifier codes–are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, word/byte write and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, word/byte write and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word/byte write suspend allows system software to suspend a word/byte write to read data from any other flash memory array location.

2.1 Data Protection

When $V_{CCW} \leq V_{CCWLK}$, memory contents cannot be altered. The CUI, with two-step block erase, full chip erase, word/byte write or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{CCW}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and word/byte write operations. Refer to Table 5 for write protection alternatives.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes or status register independent of the V_{CCW} voltage. RP# can be at V_{IH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from reset mode, the device automatically resets to read array mode. Six control pins dictate the data flow in and out of the component: CE#, OE#, BYTE#, WE#, RP# and WP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. BYTE# is the device I/O interface mde control. WE# must be at V_{IH}, RP# must be at V_{IH}, and BYTE# and WP# must be at V_{IL} or V_{IH}. Figure 16, 17 illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0-DQ_{15}) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, full chip erase, word/byte write or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Reset

RP# at V_{IL} initiates the reset mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100ns. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, word/byte write or lock-bit configuration modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, word/byte write or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block and the permanent lock configuration code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and permanent lock configuration codes identify locked and unlocked blocks and permanent lock-bit setting.

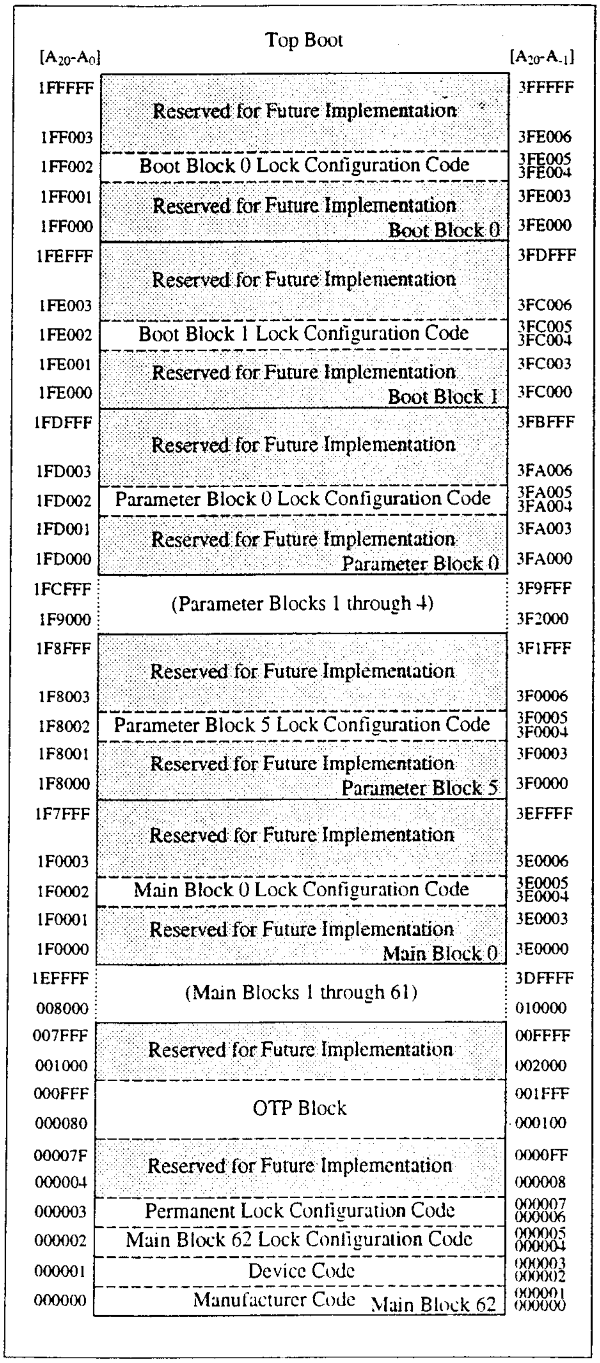

Top Boot
[A20-A0]
[A20-A-1]
1FFFFF
3FFFFF
Reserved for Future Implementation
1FF003
3FE006
1FF002
Boot Block 0 Lock Configuration Code
3FE005
3FE004
1FF001
Reserved for Future Implementation
3FE003
1FF000
Boot Block 0
3FE000
1FEFFF
3FDFFF
Reserved for Future Implementation
1FE003
3FC006
1FE002
Boot Block 1 Lock Configuration Code
3FC005
3FC004
1FE001
Reserved for Future Implementation
3FC003
1FE000
Boot Block 1
3FC000
1FDFFF
3FBFFF
Reserved for Future Implementation
1FD003
3FA006
1FD002
Parameter Block 0 Lock Configuration Code
3FA005
3FA004
1FD001
Reserved for Future Implementation
3FA003
1FD000
Parameter Block 0
3FA000
1FCFFF
(Parameter Blocks 1 through 4)
3F9FFF
1F9000
3F2000
1F8FFF
3F1FFF
Reserved for Future Implementation
1F8003
3F0006
1F8002
Parameter Block 5 Lock Configuration Code
3F0005
3F0004
1F8001
Reserved for Future Implementation
3F0003
1F8000
Parameter Block 5
3F0000
1F7FFF
3EFFFF
Reserved for Future Implementation
1F0003
3E0006
1F0002
Main Block 0 Lock Configuration Code
3E0005
3E0004
1F0001
Reserved for Future Implementation
3E0003
1F0000
Main Block 0
3E0000
1EFFFF
(Main Blocks 1 through 61)
3DFFFF
008000
010000
007FFF
Reserved for Future Implementation
00FFFF
001000
002000
000FFF
OTP Block
001FFF
000080
000100
00007F
Reserved for Future Implementation
0000FF
000004
000008
000003
Permanent Lock Configuration Code
000007
000006
000002
Main Block 62 Lock Configuration Code
000005
000004
000001
Device Code
000003
000002
000000
Manufacturer Code
Main Block 62
000001
000000

Figure 4. Device Identifier Code Memory Map

3.6 OTP(One Time Program) Block

The OTP block is a special block that can not be erased. The block is divided into two parts. One is a factory program area where a unique number can be written according to customer requirements in SHARP factory. This factory program area is "READ ONLY" (Already locked). The other is a customer program area that can be used by customers. This customer program area can be locked. After locking, this customer program area is protected permanently.

The OTP block is read in Configuration Read Mode by writing Read Identifier Codes command(90H). To return to Read Array Mode, write Read Array command(FFH).

The OTP block is programmed by writing OTP Program command(C0H). First write OTP Program command and then write data with address to the device (See Figure 5). If OTP program is failed, SR.4(WORD/BYTE WRITE AND SET LOCK-BIT STATUS) bit is set to "1". And if this OTP block is locked, SR.1(DEVICE PROTECT STATUS) bit is set to "1" too.

The OTP block is also locked by writing OTP Program command(C0H). First write OTP Program command and then write data "FFFDH" with address "80H" to the device. Address "80H" of OTP block is OTP lock information. Bit 0 of address "80H" means factory program area lock status("1" is "NOT LOCKED", "0" is "LOCKED"). Bit 1 of address "80H" means customer program area lock status. The OTP lock information can not be cleared, after once it is set.

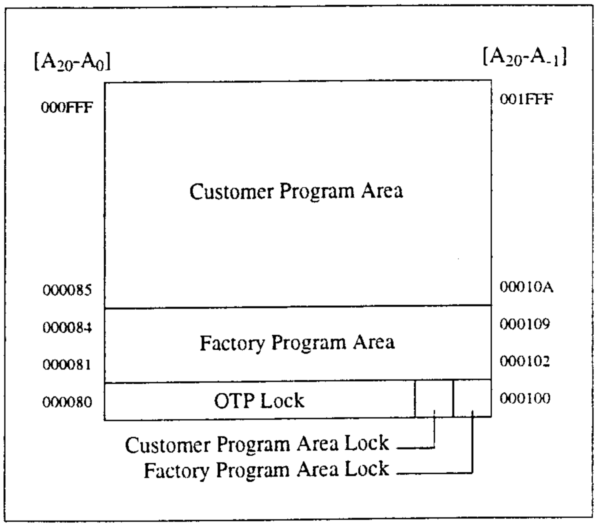

[A20-A0]
[A20-A-1]
000FFF
001FFF
Customer Program Area
000085
00010A
000084
000109
Factory Program Area
000081
000102
000080
OTP Lock
000100
Customer Program Area Lock
Factory Program Area Lock

Figure 5. OTP Block Address Map

3.7 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$, the CUI additionally controls block erase, full chip erase, word/byte write and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Full Chip Erase command requires appropriate command data and an address within the device. The Word/Byte Write command requires the command and address of the location to be written. Set Permanent and Block Lock-Bit commands require the command and address within the device (Permanent Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 18 and 19 illustrate WE# and CE# controlled write operations.

4 COMMAND DEFINITIONS

When the V_{CCW} voltage $\leq V_{CCWLK}$, Read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{CCWH1/2}$ on V_{CCW} enables successful block erase, full chip erase, word/byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

Table 2.1. Bus Operations (BYTE#=V_{IH})$^{(1,2)}$

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{CCW}	DQ_{0-15}	RY/BY#$^{(3)}$
Read	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z	X
Reset	4	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4, 5	X	Note 5	High Z
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

Table 2.2. Bus Operations (BYTE#=V_{IL})$^{(1,2)}$

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{CCW}	DQ_{0-7}	RY/BY#$^{(3)}$
Read	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z	X
Reset	4	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4, 5	X	Note 5	High Z
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:

1. Refer to DC Characteristics. When $V_{CCW} \leq V_{CCWLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{CCWLK} or $V_{CCWH1/2}$ for V_{CCW}. See DC Characteristics for V_{CCWLK} voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase, full chip erase, word/byte write or lock-bit configuration algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with word/byte write inactive), word/byte write suspend mode or reset mode.
4. RP# at GND±0.2V ensures the lowest power consumption.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase, full chip erase, word/byte write or lock-bit configuration are reliably executed when $V_{CCW}=V_{CCWH1/2}$ and V_{CC}=2.7V-3.6V.
7. Refer to Table 3 for valid D_{IN} during a write operation.
8. Never hold OE# low and WE# low at the same timing.

Table 3. Command Definitions(10)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	X	20H	Write	BA	D0H
Full Chip Erase	2		Write	X	30H	Write	X	D0H
Word/Byte Write	2	5,6	Write	X	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1	5	Write	X	B0H			
Block Erase and Word/Byte Write Resume	1	5	Write	X	D0H			
Set Block Lock-Bit	2	8	Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	2	7,8	Write	X	60H	Write	X	D0H
Set Permanent Lock-Bit	2	9	Write	X	60H	Write	X	F1H
OTP Program	2		Write	X	C0H	Write	OA	OD

NOTES:

1. BUS operations are defined in Table 2.1 and Table 2.2.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 4.
   BA=Address within the block being erased.
   WA=Address of memory location to be written.
   OA=Address of OTP block to be written: see Figure 5.
3. ID=Data read from identifier codes.
   SRD=Data read from status register. See Table 6 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   OD=Data to be written at location OA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock configuration and permanent lock configuration codes. See Section 4.2 for read identifier code data.
5. If WP# is V_{IL}, boot blocks are locked without block lock-bits state. If WP# is V_{IH}, boot blocks are locked by block lock-bits. The parameter and main blocks are locked by block lock-bits without WP# state.
6. Either 40H or 10H are recognized by the WSM as the word/byte write setup.
7. The clear block lock-bits operation simultaneously clears all block lock-bits.
8. If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
9. Once the permanent lock-bit is set, permanent lock-bit reset is unable.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from reset mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, word/byte write or lock-bit configuration the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word/Byte Write Suspend command. The Read Array command functions independently of the V_{CCW} voltage and RP# can be V_{IH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and permanent lock configuration codes (see Table 4 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{CCW} voltage and RP# can be V_{IH}. Following the Read Identifier Codes command, the following information can be read:

Table 4. Identifier Codes

Code	Address[2] [A_{20}-A_0]	Data[3] [DQ_7-DQ_0]
Manufacture Code	00000H	B0H
Device Code	00001H	E2H
Block Lock Configuration	BA[1]+2	▨
•Block is Unlocked		DQ_0=0
•Block is Locked		DQ_0=1
•Reserved for Future Use		DQ_{1-7}
Permanent Lock Configuration	00003H	▨
•Device is Unlocked		DQ_0=0
•Device is Locked		DQ_0=1
•Reserved for Future Use		DQ_{1-7}

NOTE:

1. BA selects the specific block lock configuration code to be read. See Figure 4 for the device identifier code memory map.
2. A_{-1} don't care in byte mode.
3. DQ_{15}-DQ_8 outputs 00H in word mode.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, word/byte write or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{CCW} voltage. RP# can be V_{IH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words/bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{CCW} Voltage. RP# can be V_{IH}. This command is not functional during block erase or word/byte write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH/FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleard the corresponding block lock-bit. If block erase is attempted when the excepting above conditions, SR.1 and SR.5 will be set to "1".

4.6 Full Chip Erase Command

This command followed by a confirm command erases all of the unlocked blocks. A full chip erase setup (30H) is first written, followed by a full chip erase confirm (D0H). After a confirm command is written, device erases the all unlocked blocks block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect full chip erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Full chip erase operation start from lower address block, finish the higher address block. Full chip erase can not be suspended.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". Successful full chip erase requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleard the corresponding block lock-bit. If all blocks are locked, SR.1 and SR.5 will be set to "1".

4.7 Word/Byte Write Command

Word/Byte write is executed by a two-cycle command sequence. Word/Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect the completion of the word/byte write event by analyzing the RY/BY# pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{CCW} \leq V_{CCWLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleard the corresponding block lock-bit. If word/byte write is attempted when the excepting above conditions, SR.1 and SR.4 will be set to "1".

4.8 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word/byte write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to High Z. Specification t_{WHRZ2} defines the block erase suspend latency.

When Block Erase Suspend command write to the CUI, if block erase was finished, the device places read array mode. Therefore, after Block Erase Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.6 should be checked for places the device in suspend mode.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word/Byte Write Suspend command (see Section 4.9), a word/byte write operation can also be suspended. During a word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 9). V_{CCW} must remain at $V_{CCWH1/2}$ (the same V_{CCW} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH}. WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for block erase). Block erase cannot resume until word/byte write operations initiated during block erase suspend have completed.

If the period of from Block Erase Resume command write to the CUI till Block Erase Suspend command write to the CUI be short and done again and again, erase time be prolonged.

4.9 Word/Byte Write Suspend Command

The Word/Byte Write Suspend command allows word/byte write interruption to read data in other flash memory locations. Once the word/byte write process starts, writing the Word/Byte Write Suspend command requests that the WSM suspend the Word/Byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word/byte write operation has been suspended (both will be set to "1"). RY/BY# will also transition to High Z. Specification t_{WHRZ1} defines the word/byte write suspend latency.

When Word/Byte Write Suspend command write to the CUI, if word/byte write was finished, the device places read array mode. Therefore, after Word/Byte Write Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.2 should be checked for places the device in suspend mode.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word/byte write is suspended are Read Status Register and Word/Byte Write Resume. After Word/Byte Write Resume command is written to the flash memory, the WSM will continue the word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Word/Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 10). V_{CCW} must remain at $V_{CCWH1/2}$ (the same V_{CCW} level used for word/byte write) while in word/byte write suspend mode. RP# must also remain at V_{IH}. WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for word/byte write).

If the period of from Word/Byte Write Resume command write to the CUI till Word/Byte Write Suspend command write to the CUI be short and done again and again, write time be prolonged.

4.10 Set Block and Permanent Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits, a permanent lock-bit and WP# pin. The block lock-bits and WP# pin gates program and erase operations while the permanent lock-bit gates block-lock bit modification. With the permanent lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Permanent Lock-Bit command, sets the permanent lock-bit. After the permanent lock-bit is set, block lock-bits and locked block contents cannot altered. See Table 5 for a summary of hardware and software write protection options.

Set block lock-bit and permanent lock-bit are executed by a two-cycle command sequence. The set block or permanent lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set permanent lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect the completion of the set lock-bit event by analyzing the RY/BY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Permanent Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the permanent lock-bit be cleared. If it is attempted with the permanent lock-bit set, SR.1 and SR.4 will be set to "1" and the operation will fail.

4.11 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the permanent lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the permanent lock-bit is set, block lock-bits cannot cleared. See Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 12). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/BY# Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. If a clear block lock-bits operation is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the permanent lock-bit is not set. If it is attempted with the permanent lock-bit set, SR.1 and SR.5 will be set to "1" and the operation will fail.

If a clear block lock-bits operation is aborted due to V_{CCW} or V_{CC} transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the permanent lock-bit is set, it cannot be cleared.

4.12 OTP Program Command

OTP program is executed by a two-cycle command sequence. OTP program command(C0H) is written, followed by a second write cycle that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the OTP program and program verify algorithms internally. After the OTP program command sequence is completed, the device automatically outputs status register data when read (see Figure 13). The CPU can detect the completion of the OTP program by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When OTP program is completed, status register bit SR.4 should be checked. If OTP program error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read status register mode until it receives other commands.

Reliable OTP program can be executed only when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this voltage, memory contents are protected against OTP programs. If OTP program is attempted while $V_{CCW} \le V_{CCWLK}$, status register bits SR.3 and SR.4 is set to "1". If OTP write is attempted when the OTP Lock-bit is set, SR.1 and SR.4 is set to "1".

4.13 Block Locking by the WP#

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

The lockable two boot blocks are locked when WP#=V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. If WP# is V_{IH} and block lock-bit is not set, boot block can be programmed or erased normally (Unless V_{CCW} is below V_{CCWLK}). WP# is valid only two boot blocks, other blocks are not affected.

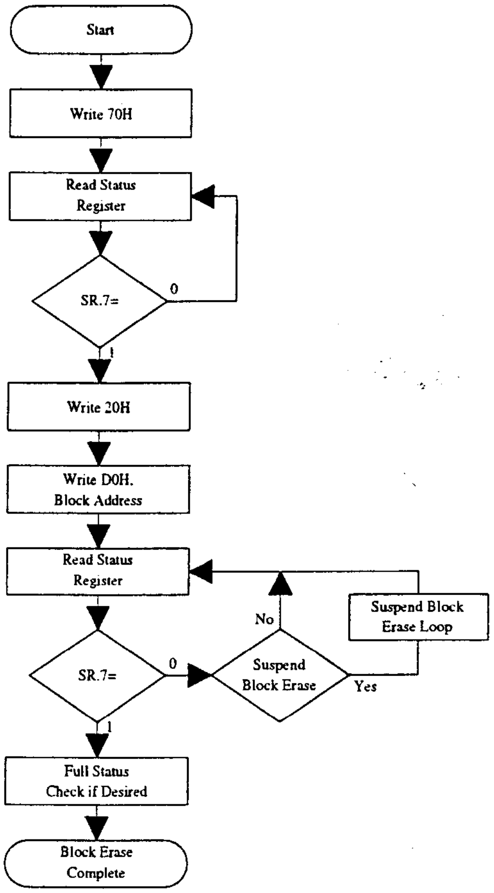
Table 5. Write Protection Alternatives

Operation	V_{CCW}	RP#	Permanent Lock-Bit	Block Lock-bit	WP#	Effect
Block Erase or Word/Byte Write	$\le V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	0	V_{IL}	2 Boot Blocks Locked.
					V_{IH}	Block Erase and Word/Byte Write Enabled.
				1	V_{IL}	Block Erase and Word/Byte Write Disabled.
					V_{IH}	Block Erase and Word/Byte Write Disabled.
Full Chip Erase	$\le V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	X	V_{IL}	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are NOT Erased.
					V_{IH}	All Unlocked Blocks are Erased, Locked Blocks are NOT Erased.
Set Block Lock-Bit	$\le V_{CCWLK}$	X	X	X	X	Set Block Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V_{IH}	0	X	X	Set Block Lock-Bit Enabled.
			1	X	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	$\le V_{CCWLK}$	X	X	X	X	Clear Block Lock-Bits Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V_{IH}	0	X	X	Clear Block Lock-Bits Enabled.
			1	X	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	$\le V_{CCWLK}$	X	X	X	X	Set Permanent Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V_{IH}	X	X	X	Set Permanent Lock-Bit Enabled.

Table 6. Status Register Definition

WSMS	BESS	ECBLBS	WBWSLBS	VCCWS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check RY/BY# or SR.7 to determine block erase, full chip erase, word/byte write or lock-bit configuration completion. SR.6-0 are invalid while SR.7="0".
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1 = Error in Block Erase, Full Chip Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Full Chip Erase or Clear Block Lock-Bits	If both SR.5 and SR.4 are "1"s after a block erase, full chip erase or lock-bit configuration attempt, an improper command sequence was entered.
SR.4 = WORD/BYTE WRITE AND SET LOCK-BIT STATUS (WBWSLBS) 1 = Error in Word/Byte Write or Set Block/Permanent Lock-Bit 0 = Successful Word/Byte Write or Set Block/Permanent Lock-Bit	
SR.3 = V_{CCW} STATUS (VCCWS) 1 = V_{CCW} Low Detect, Operation Abort 0 = V_{CCW} OK	SR.3 does not provide a continuous indication of V_{CCW} level. The WSM interrogates and indicates the V_{CCW} level only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{CCW} \neq V_{CCWH1/2}$.
SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Lock-Bit, Permanent Lock-Bit and/or WP# Lock Detected, Operation Abort 0 = Unlock	SR.1 does not provide a continuous indication of permanent and block lock-bit and WP# values. The WSM interrogates the permanent lock-bit, block lock-bit and WP# only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or WP# is V_{IL}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.


Start
Write 70H
Read Status Register
SR.7=
0
1
Write 20H
Write D0H, Block Address
Read Status Register
SR.7=
0
1
Suspend Block Erase
No
Yes
Suspend Block Erase Loop
Full Status Check if Desired
Block Erase Complete

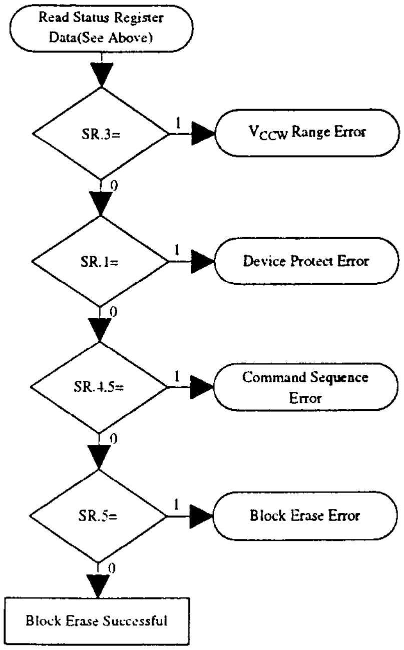
Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Erase Setup	Data=20H Addr=X
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.

Full status check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

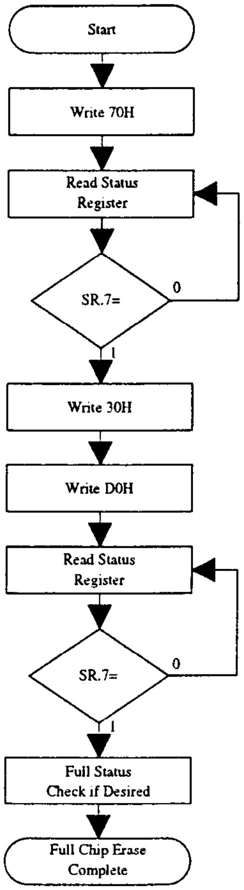

Read Status Register Data(See Above)
SR.3=
1
0
V_{CCW} Range Error
SR.1=
1
0
Device Protect Error
SR.4,5=
1
0
Command Sequence Error
SR.5=
1
0
Block Erase Error
Block Erase Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

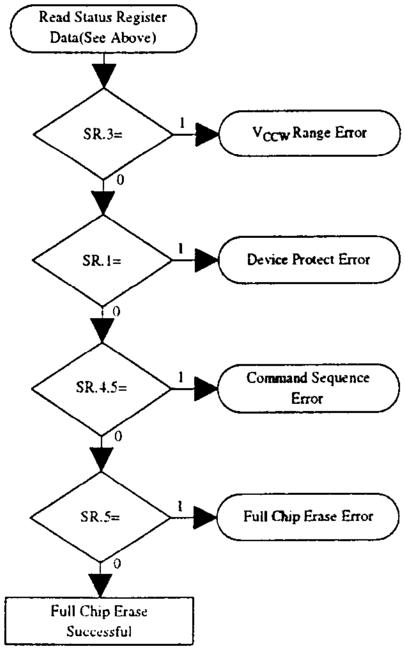
Figure 6. Automated Block Erase Flowchart


Start
Write 70H
Read Status Register
SR.7=
0
1
Write 30H
Write D0H
Read Status Register
SR.7=
0
1
Full Status Check if Desired
Full Chip Erase Complete

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Full Chip Erase Setup	Data=30H Addr=X
Write	Full Chip Erase Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Full status check can be done after each full chip erase.
Write FFH after the last operation to place device in read array mode.

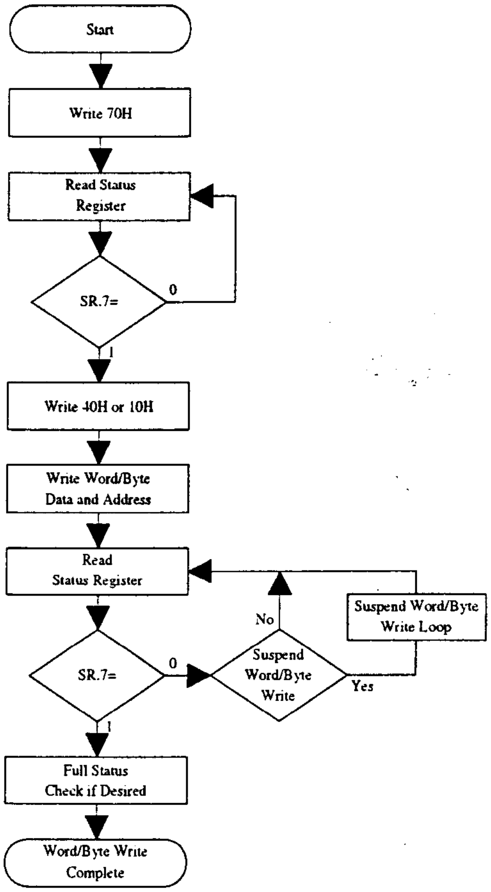
FULL STATUS CHECK PROCEDURE


Read Status Register Data(See Above)
SR.3=
1
V_{CCW} Range Error
0
SR.1=
1
Device Protect Error
0
SR.4,5=
1
Command Sequence Error
0
SR.5=
1
Full Chip Erase Error
0
Full Chip Erase Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect (All Blocks are locked)
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Full Chip Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 7. Automated Full Chip Erase Flowchart


Start
Write 70H
Read Status Register
SR.7=
0
1
Write 40H or 10H
Write Word/Byte Data and Address
Read Status Register
Suspend Word/Byte Write Loop
No
SR.7=
0
Suspend Word/Byte Write
Yes
1
Full Status Check if Desired
Word/Byte Write Complete

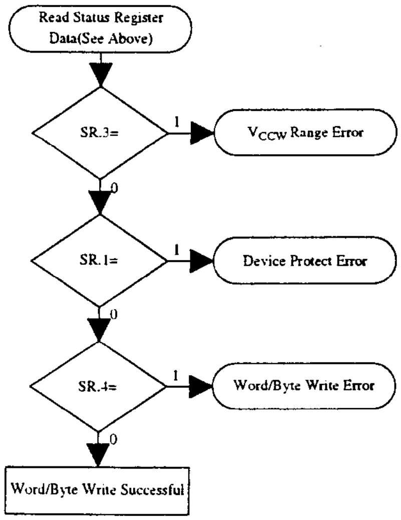
Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Setup Word/Byte Write	Data=40H or 10H Addr=X
Write	Word/Byte Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent word/byte writes.

SR full status check can be done after each word/byte write, or after a sequence of word/byte writes.

Write FFH after the last word/byte write operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

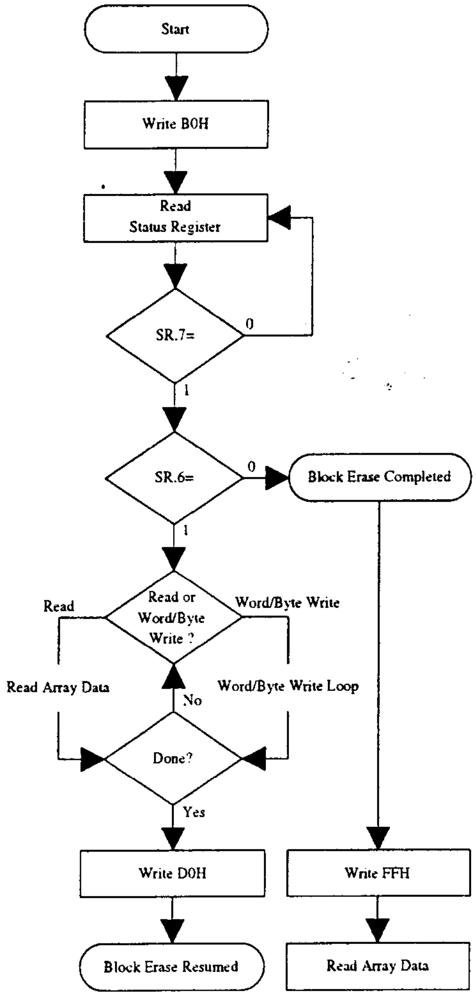

Read Status Register Data(See Above)
SR.3=
1
V_CCW Range Error
0
SR.1=
1
Device Protect Error
0
SR.4=
1
Word/Byte Write Error
0
Word/Byte Write Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.

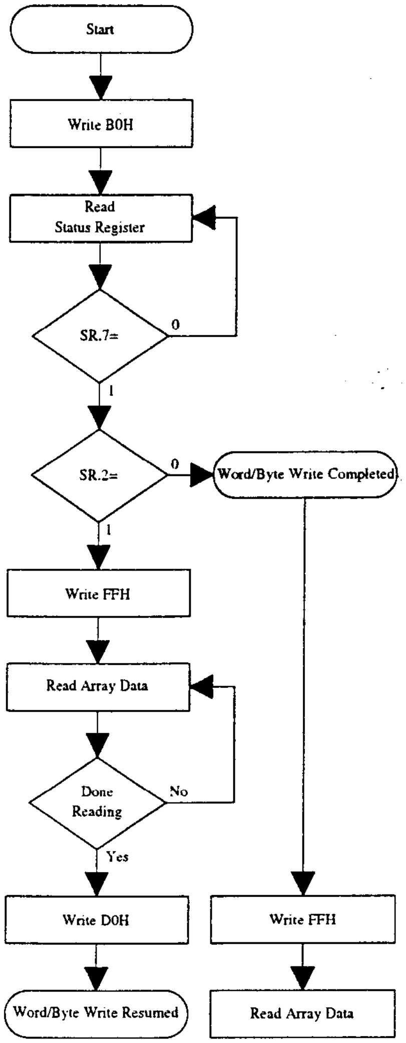
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 8. Automated Word/Byte Write Flowchart


Start
Write B0H
Read
Status Register
SR.7=
0
1
SR.6=
0
Block Erase Completed
1
Read or
Word/Byte
Write ?
Read
Word/Byte Write
Read Array Data
Word/Byte Write Loop
No
Done?
Yes
Write D0H
Write FFH
Block Erase Resumed
Read Array Data

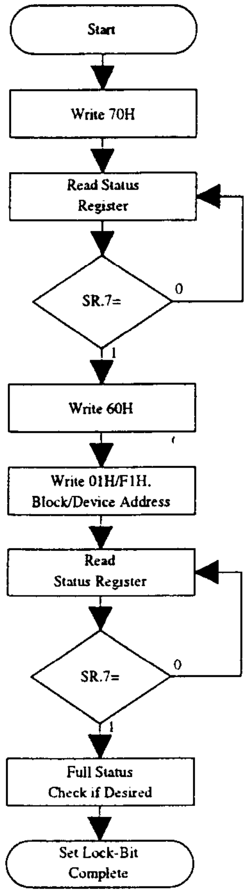
Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 9. Block Erase Suspend/Resume Flowchart


Start
Write B0H
Read Status Register
SR.7=
0
1
SR.2=
0
Word/Byte Write Completed
1
Write FFH
Read Array Data
Done Reading
No
Yes
Write D0H
Word/Byte Write Resumed
Write FFH
Read Array Data

Bus Operation	Command	Comments
Write	Word/Byte Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Word/Byte Write Suspended 0=Word/Byte Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Word/Byte Write Resume	Data=D0H Addr=X

Figure 10. Word/Byte Write Suspend/Resume Flowchart


Start
Write 70H
Read Status Register
SR.7=
0
1
Write 60H
Write 01H/F1H, Block/Device Address
Read Status Register
SR.7=
0
1
Full Status Check if Desired
Set Lock-Bit Complete

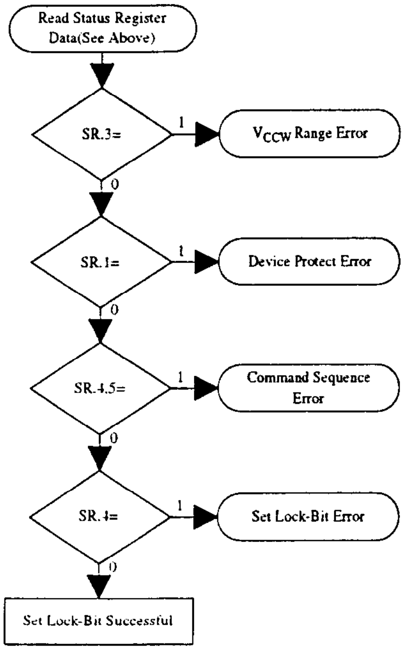
Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Set Block/Permanent Lock-Bit Setup	Data=60H Addr=X
Write	Set Block or Permanent Lock-Bit Confirm	Data=01H(Block), F1H(Permanent) Addr=Block Address(Block), Device Address(Permanent)
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent lock-bit set operations.

Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations.

Write FFH after the last lock-bit set operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

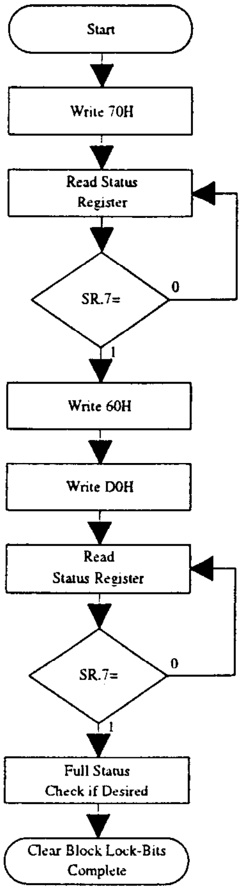

Read Status Register Data(See Above)
SR.3=
1
V_{CCW} Range Error
0
SR.1=
1
Device Protect Error
0
SR.4,5=
1
Command Sequence Error
0
SR.4=
1
Set Lock-Bit Error
0
Set Lock-Bit Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect Permanent Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Set Lock-Bit Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

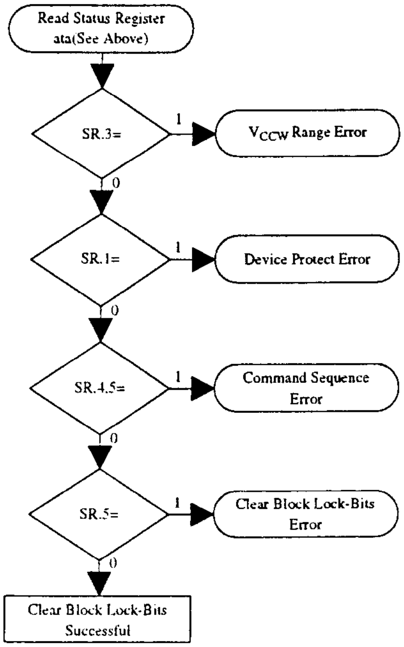
Figure 11. Set Block and Permanent Lock-Bit Flowchart


Start
Write 70H
Read Status Register
SR.7=
0
1
Write 60H
Write D0H
Read Status Register
SR.7=
0
1
Full Status Check if Desired
Clear Block Lock-Bits Complete

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Clear Block Lock-Bits Setup	Data=60H Addr=X
Write	Clear Block Lock-Bits Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.

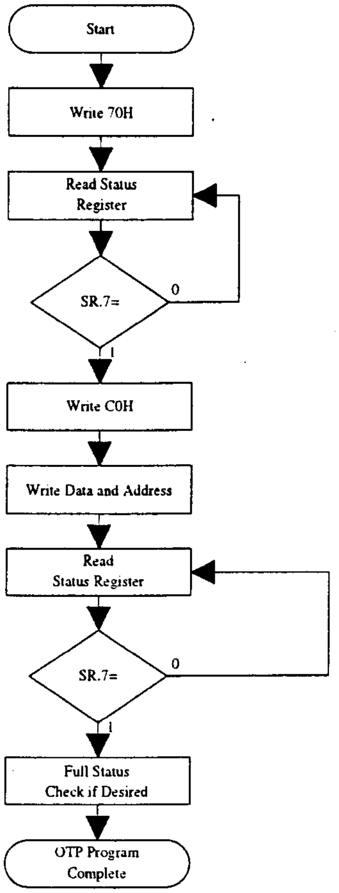
FULL STATUS CHECK PROCEDURE


Read Status Register ata(See Above)
SR.3=
1
0
V_{CCW} Range Error
SR.1=
1
0
Device Protect Error
SR.4,5=
1
0
Command Sequence Error
SR.5=
1
0
Clear Block Lock-Bits Error
Clear Block Lock-Bits Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect Permanent Lock-Bit is Set
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Clear Block Lock-Bits Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command.
If error is detected, clear the Status Register before attempting retry or other error recovery.

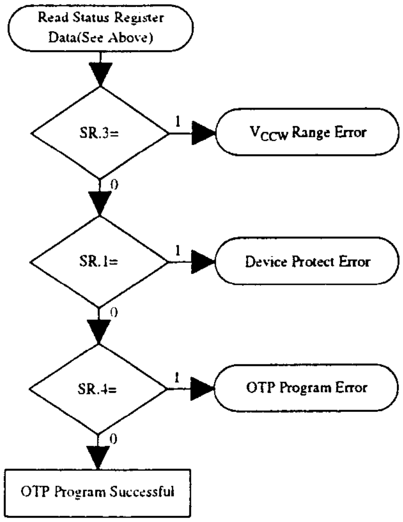
Figure 12. Clear Block Lock-Bits Flowchart


Start
Write 70H
Read Status Register
SR.7=
0
1
Write C0H
Write Data and Address
Read Status Register
SR.7=
0
1
Full Status Check if Desired
OTP Program Complete

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Setup OTP Program	Data=C0H Addr=X
Write	OTP Program	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent OTP programs.
SR full status check can be done after each OTP program, or after a sequence of OTP programs.
Write FFH after the last OTP program operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE


Read Status Register Data(See Above)
SR.3=
1
V_{CCW} Range Error
0
SR.1=
1
Device Protect Error
0
SR.4=
1
OTP Program Error
0
OTP Program Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 13. Automated OTP Program Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/BY# and WSM Polling

RY/BY# is an open drain output that should be connected to V_{CC} by a pull up resistor to provides a hardware method of detecting block erase, full chip erase, word/byte write and lock-bit configuration completion. It transitions low after block erase, full chip erase, word/byte write or lock-bit configuration commands and returns to V_{OH} (while RY/BY# is pull up) when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/BY# is also High Z when the device is in block erase suspend (with word/byte write inactive), word/byte write suspend or reset modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1µF ceramic capacitor connected between its V_{CC} and GND and between its V_{CCW} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{CCW} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{CCW} Power supply trace. The V_{CCW} pin supplies the memory cell current for word/byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{CCW} supply traces and decoupling will decrease V_{CCW} voltage spikes and overshoots.

5.5 V_{CC}, V_{CCW}, RP# Transitions

Block erase, full chip erase, word/byte write and lock-bit configuration are not guaranteed if V_{CCW} falls outside of a valid $V_{CCWH1/2}$ range, V_{CC} falls outside of a valid 2.7V-3.6V range, or RP#$\neq V_{IH}$. If V_{CCW} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase, full chip erase, word/byte write or lock-bit configuration, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter reset mode. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{CCW} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from reset mode or after V_{CC} transitions below V_{LKO}.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erase, full chip erase, word/byte write or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{CCW} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{CCW} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP#=V_{IL} regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

5.8 Data Protection Method

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto WE# signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block

When a lock bit is set, the corresponding block (includes the 2 boot blocks) is protected against overwriting. By setting a WP# to low, only the 2 boot blocks can be protected against overwriting. By using this feature, the flash memory space can be divided into the program section (locked section) and data section (unlocked section). The permanent lock bit can be used to prevent false block bit setting. For further information on setting/resetting lock-bit, refer to the specification. (See chapter 4.10 and 4.11.)

2) Data protection through V_{CCW}

When the level of V_{CCW} is lower than V_{CCWLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected. For the lockout voltage, refer to the specification. (See chapter 6.2.3.)

3) Data protection through RP#

When the RP# is kept low during read mode, the flash memory will be deep-power-down mode, then write protecting all blocks. When the RP# is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks. For the details of RP# control, refer to the specification. (See chapter 5.6 and 6.2.7.)

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Operating Temperature
- During Read, Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration .... 0°C to +70°C(1)

Storage Temperature
During under Bias .... -10°C to +80°C
During non Bias .... -65°C to +125°C

Voltage On Any Pin
(except V_{CC} and V_{CCW}) .... -0.5V to V_{CC}+0.5V(2)

V_{CC} Supply Voltage................................ -0.2V to +4.6V(2)

V_{CCW} Supply Voltage......................... -0.2V to +13.0V(2,3)

Output Short Circuit Current................................ 100mA(4)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{CCW} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins are V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Maximum DC voltage on V_{CCW} may overshoot to +13.0V for periods <20ns. Applying 12V±0.3V to V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{CCW} may be connected to 12V±0.3V for a total of 80 hours maximum.
4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T_A	Operating Temperature	0	+70	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage (2.7V-3.6V)	2.7	3.6	V	

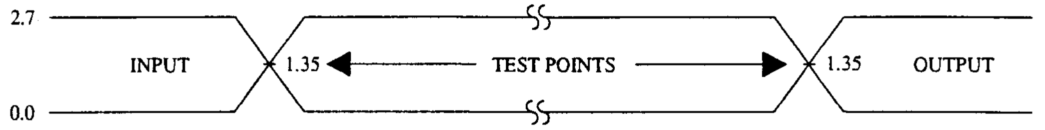
6.2.1 CAPACITANCE(1)

T_A=+25°C, f=1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance	7	10	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT}=0.0V

NOTE:
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS


2.7
0.0
INPUT
1.35
TEST POINTS
1.35
OUTPUT

AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 14. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

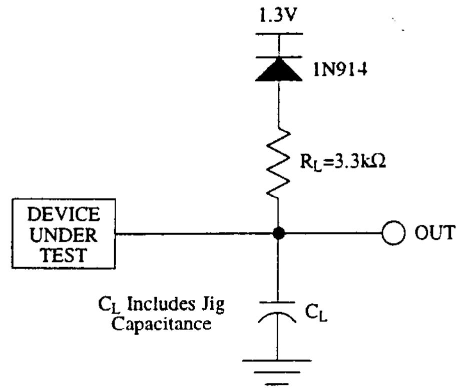

1.3V
1N914
R_L=3.3kΩ
DEVICE UNDER TEST
OUT
C_L Includes Jig Capacitance
C_L

Figure 15. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=2.7V-3.6V	50

6.2.3 DC CHARACTERISTICS

DC Characteristics

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V		Unit	Test Conditions
			Typ.	Max.		
I_{LI}	Input Load Current	1		±0.5	µA	V_{CC}=V_{CC}Max. V_{IN}=V_{CC} or GND
I_{LO}	Output Leakage Current	1		±0.5	µA	V_{CC}=V_{CC}Max. V_{OUT}=V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,3	4	20	µA	V_{CC}=V_{CC}Max. CE#=RP#=V_{CC}±0.2V
I_{CCAS}	V_{CC} Auto Power-Save Current	1,5	4	20	µA	V_{CC}=V_{CC}Max. CE#=GND±0.2V
I_{CCD}	V_{CC} Reset Power-Down Current	1	4	20	µA	RP#=GND±0.2V I_{OUT}(RY/BY#)=0mA
I_{CCR}	V_{CC} Read Current	1	15	30	mA	V_{CC}=V_{CC}Max., CE#=GND f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Word/Byte Write or Set Lock-Bit Current	1,6	5	17	mA	V_{CCW}=2.7V-3.6V
			5	12	mA	V_{CCW}=11.7V-12.3V
I_{CCE}	V_{CC} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	1,6	4	17	mA	V_{CCW}=2.7V-3.6V
			4	12	mA	V_{CCW}=11.7V-12.3V
I_{CCWS} I_{CCES}	V_{CC} Word/Byte Write or Block Erase Suspend Current	1,2	1	6	mA	CE#=V_{IH}
I_{CCWS}	V_{CCW} Standby or Read Current	1	±2	±15	µA	V_{CCW}≤V_{CC}
I_{CCWR}			10	200	µA	V_{CCW}>V_{CC}
I_{CCWAS}	V_{CCW} Auto Power-Save Current	1,5	0.1	5	µA	V_{CC}=V_{CC}Max. CE#=GND±0.2V
I_{CCWD}	V_{CCW} Reset Power-Down Current	1	0.1	5	µA	RP#=GND±0.2V
I_{CCWW}	V_{CCW} Word/Byte Write or Set Lock-Bit Current	1,6	12	40	mA	V_{CCW}=2.7V-3.6V
				30	mA	V_{CCW}=11.7V-12.3V
I_{CCWE}	V_{CCW} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	1,6	8	25	mA	V_{CCW}=2.7V-3.6V
				20	mA	V_{CCW}=11.7V-12.3V
I_{CCWWS} I_{CCWES}	V_{CCW} Word/Byte Write or Block Erase Suspend Current	1	10	200	µA	V_{CCW}=$V_{CCWH1/2}$

DC Characteristics (Continued)

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V		Unit	Test Conditions
			Min.	Max.		
V_{IL}	Input Low Voltage	6	-0.5	0.4	V	
V_{IH}	Input High Voltage	6	V_{CC} -0.4	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	3,6		0.4	V	V_{CC}=V_{CC} Min. I_{OL}=2.0mA
V_{OH}	Output High Voltage	6	V_{CC} -0.4		V	V_{CC}=V_{CC} Min. I_{OH}=-100μA
V_{CCWLK}	V_{CCW} Lockout during Normal Operations	4,6		1.0	V	
V_{CCWH1}	V_{CCW} during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration Operations		2.7	3.6	V	
V_{CCWH2}	V_{CCW} during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration Operations	7	11.7	12.3	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word/byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/BY#.
4. Block erases, full chip erase, word/byte writes and lock-bit configurations are inhibited when $V_{CCW} \leq V_{CCWLK}$, and not guaranteed in the range between V_{CCWLK}(max.) and V_{CCWH1}(min.), between V_{CCWH1}(max.) and V_{CCWH2}(min.) and above V_{CCWH2}(max.).
5. The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300ns while read mode.
6. Sampled, not 100% tested.
7. Applying 12V±0.3V to V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{CCW} may be connected to 12V±0.3V for a total of 80 hours maximum.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=0°C to +70°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		90		ns
t_{AVQV}	Address to Output Delay			90	ns
t_{ELQV}	CE# to Output Delay	2		90	ns
t_{PHQV}	RP# High to Output Delay			600	ns
t_{GLQV}	OE# to Output Delay	2		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		40	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		15	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FVQV}	BYTE# to Output Delay	3		90	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		25	ns
t_{ELFV}	CE# to BYTE# High or Low	3,4		5	ns

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. If BYTE# transfer during reading cycle, exist the regulations separately.

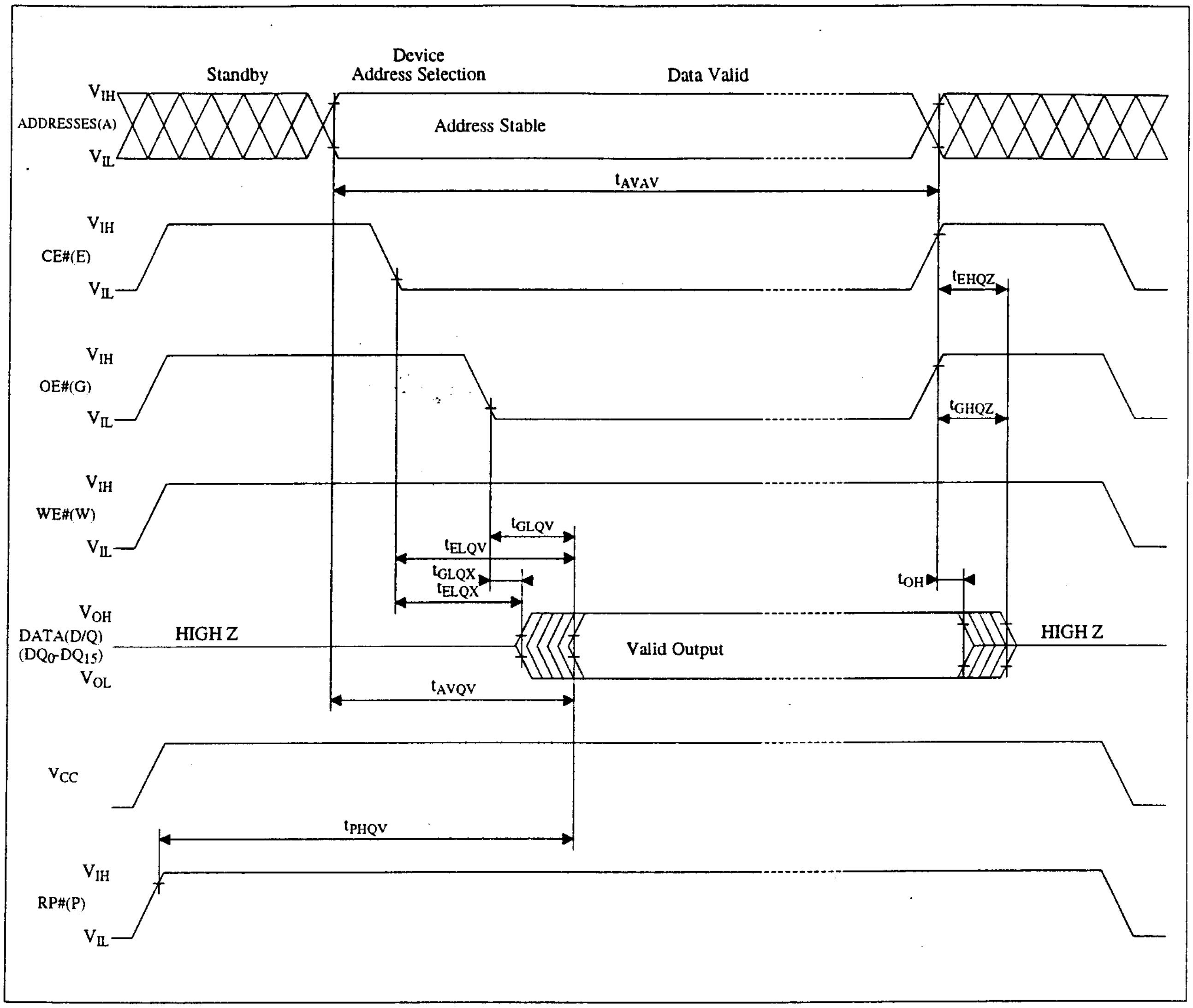

Standby
Device Address Selection
Data Valid
V_{IH}
ADDRESSES(A)
V_{IL}
Address Stable
t_{AVAV}
V_{IH}
CE#(E)
V_{IL}
t_{EHQZ}
V_{IH}
OE#(G)
V_{IL}
t_{GHQZ}
V_{IH}
WE#(W)
V_{IL}
t_{GLQV}
t_{ELQV}
t_{GLQX}
t_{ELQX}
t_{OH}
V_{OH}
DATA(D/Q) (DQ_0-DQ_{15})
V_{OL}
HIGH Z
Valid Output
HIGH Z
t_{AVQV}
V_{CC}
t_{PHQV}
V_{IH}
RP#(P)
V_{IL}

Figure 16. AC Waveform for Read Operations

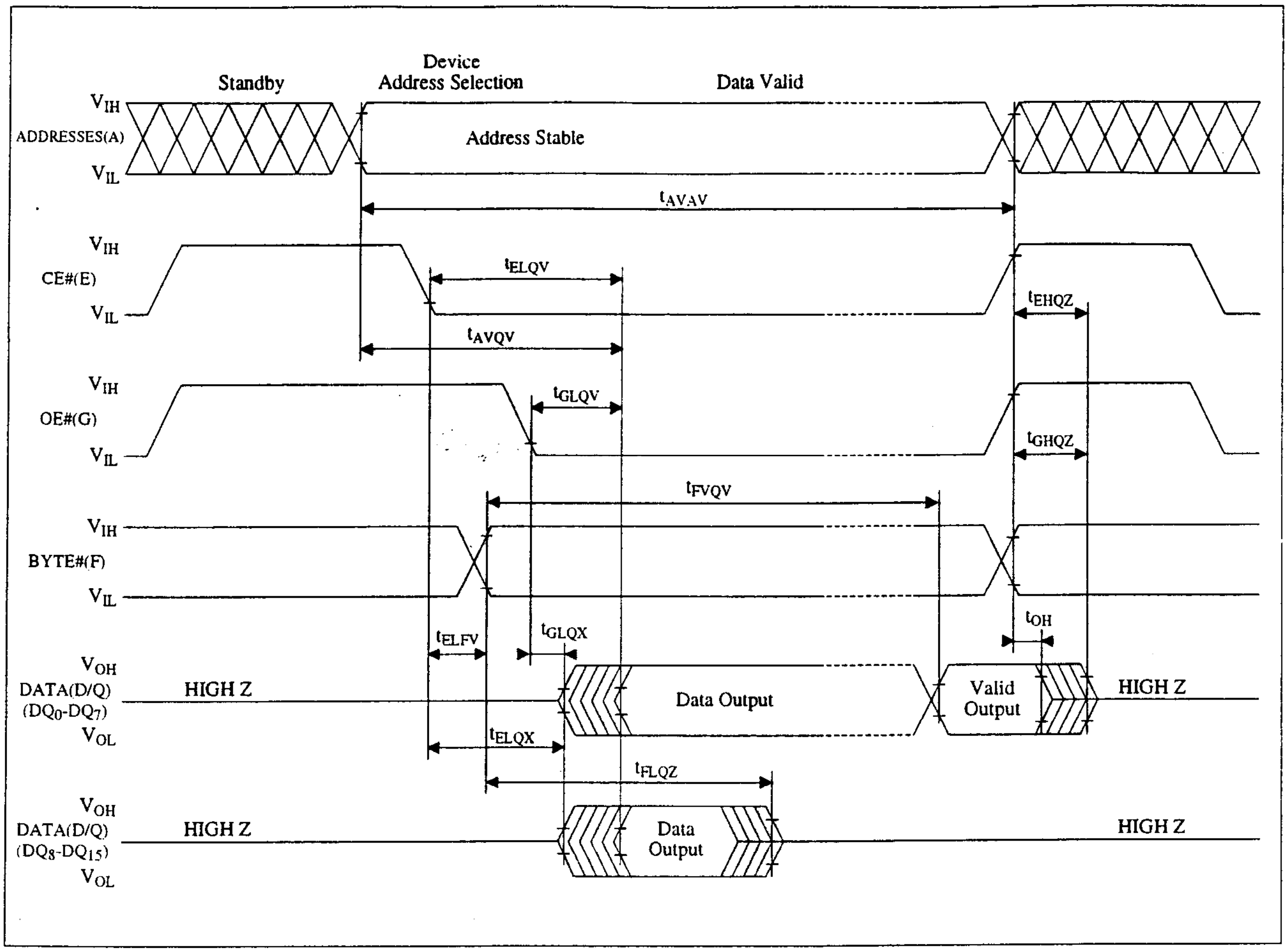

Standby
Device Address Selection
Data Valid
V_{IH}
ADDRESSES(A)
V_{IL}
Address Stable
t_{AVAV}
V_{IH}
CE#(E)
V_{IL}
t_{ELQV}
t_{EHQZ}
t_{AVQV}
V_{IH}
OE#(G)
V_{IL}
t_{GLQV}
t_{GHQZ}
t_{FVQV}
V_{IH}
BYTE#(F)
V_{IL}
t_{OH}
t_{ELFV}
t_{GLQX}
V_{OH}
DATA(D/Q)
(DQ_0-DQ_7)
V_{OL}
HIGH Z
Data Output
Valid Output
HIGH Z
t_{ELQX}
t_{FLQZ}
V_{OH}
DATA(D/Q)
(DQ_8-DQ_{15})
V_{OL}
HIGH Z
Data Output
HIGH Z

Figure 17. BYTE# timing Waveform

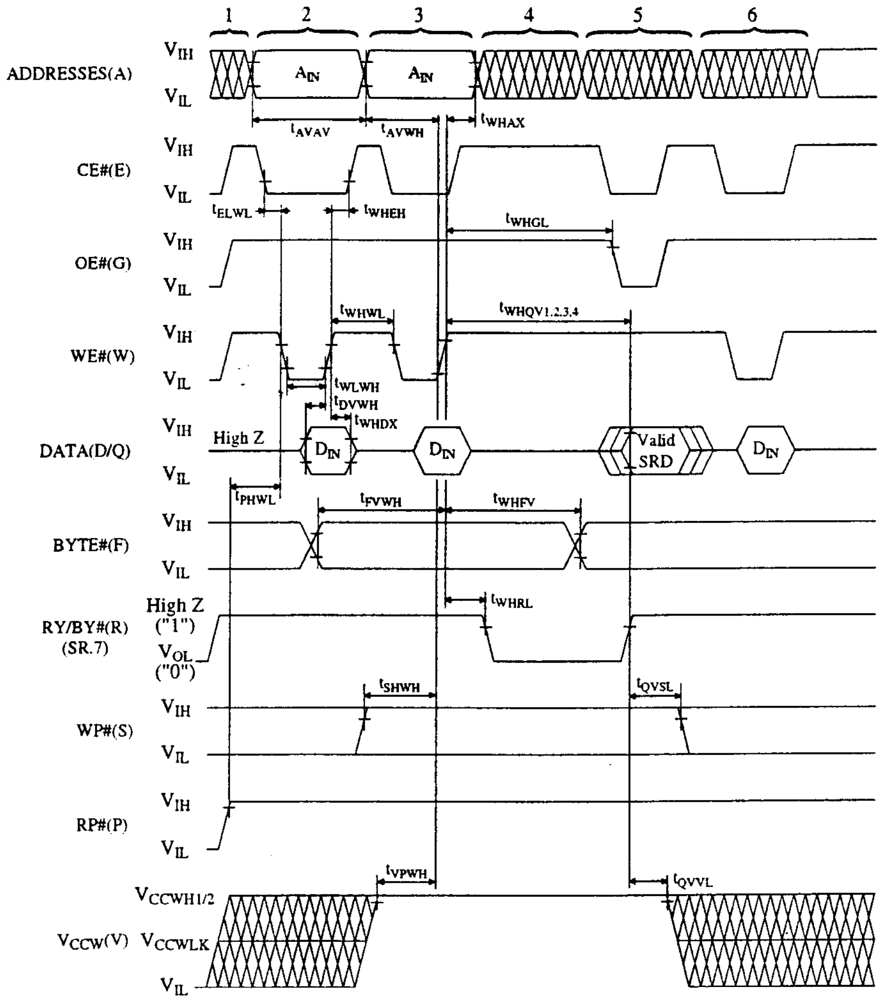
6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=0°C to +70°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		ns
t_{WLWH}	WE# Pulse Width		50		ns
t_{SHWH}	WP#V_{IH} Setup to WE# Going High	2	100		ns
t_{VPWH}	V_{CCW} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High		0		ns
t_{WHAX}	Address Hold from WE# High		0		ns
t_{WHEH}	CE# Hold from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low or SR.7 Going "0"			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{CCW} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{FVWH}	BYTE# Setup to WE# Going High	5	50		ns
t_{WHFV}	BYTE# Hold from WE# High	5	90		ns

NOTES:

1. Read timing characteristics during block erase, full chip erase, word/byte write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, word/byte write or lock-bit configuration.
4. V_{CCW} should be held at $V_{CCWH1/2}$ until determination of block erase, full chip erase, word/byte write or lock-bit configuration success (SR.1/3/4/5=0).
5. If BYTE# switch during reading cycle, exist the regulations separately.


1
2
3
4
5
6
ADDRESSES(A)
VIH
VIL
AIN
AIN
tAVAV
tAVWH
tWHAX
CE#(E)
VIH
VIL
tELWL
tWHEH
tWHGL
OE#(G)
VIH
VIL
tWHWL
tWHQV1,2,3,4
WE#(W)
VIH
VIL
tWLWH
tDVWH
tWHDX
DATA(D/Q)
VIH
VIL
High Z
DIN
DIN
Valid SRD
DIN
tPHWL
tFVWH
tWHFV
BYTE#(F)
VIH
VIL
tWHRL
RY/BY#(R)
(SR.7)
High Z
("1")
VOL
("0")
tSHWH
tQVSL
WP#(S)
VIH
VIL
RP#(P)
VIH
VIL
tVPWH
tQVVL
VCCWH1/2
VCCW(V)
VCCWLK
VIL

NOTES:

1. V_{CC} power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 18. AC Waveform for WE#-Controlled Write Operations

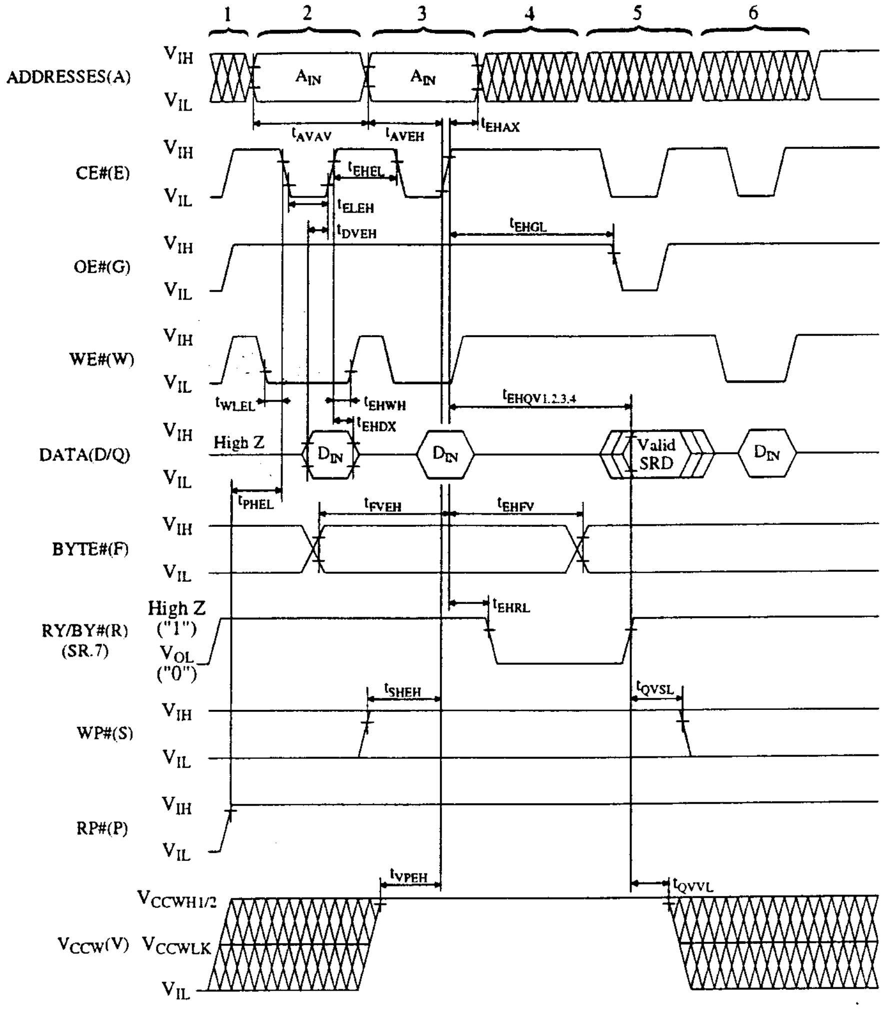
6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES(1)

V_{CC}=2.7V-3.6V, T_A=0°C to +70°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		65		ns
t_{SHEH}	WP#V_{IH} Setup to CE# Going High	2	100		ns
t_{VPEH}	V_{CCW} Setup to CE# Going High	2	100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High		0		ns
t_{EHAX}	Address Hold from CE# High		0		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low or SR.7 Going "0"			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{CCW} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{FVEH}	BYTE# Setup to CE# Going High	5	50		ns
t_{EHFV}	BYTE# Hold from CE# High	5	90		ns

NOTES:

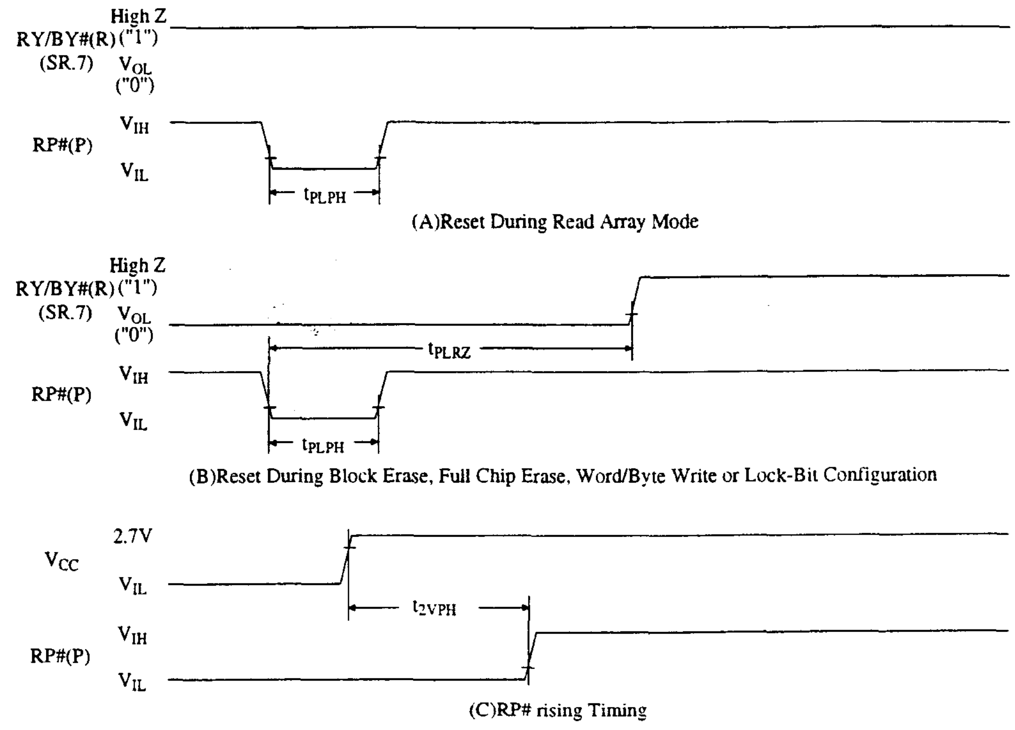
1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, word/byte write or lock-bit configuration.
4. V_{CCW} should be held at $V_{CCWH1/2}$ until determination of block erase, full chip erase, word/byte write or lock-bit configuration success (SR.1/3/4/5=0).
5. If BYTE# switch during reading cycle, exist the regulations separately.


1
2
3
4
5
6
ADDRESSES(A)
V_{IH}
V_{IL}
A_{IN}
A_{IN}
t_{AVAV}
t_{AVEH}
t_{EHAX}
CE#(E)
t_{EHEL}
t_{ELEH}
t_{DVEH}
t_{EHGL}
OE#(G)
WE#(W)
t_{WLEL}
t_{EHWH}
t_{EHDX}
$t_{EHQV1,2,3,4}$
DATA(D/Q)
High Z
D_{IN}
D_{IN}
Valid SRD
D_{IN}
t_{PHEL}
t_{FVEH}
t_{EHFV}
BYTE#(F)
t_{EHRL}
RY/BY#(R)
(SR.7)
High Z ("1")
V_{OL} ("0")
t_{SHEH}
t_{QVSL}
WP#(S)
RP#(P)
t_{VPEH}
t_{QVVL}
$V_{CCWH1/2}$
V_{CCW}(V)
V_{CCWLK}

NOTES:
1. V_{CC} power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 19. AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS


High Z
RY/BY#(R) ("1")
(SR.7) VOL
("0")
VIH
RP#(P)
VIL
tPLPH
High Z
RY/BY#(R) ("1")
(SR.7) VOL
("0")
tPLRZ
VIH
RP#(P)
VIL
tPLPH
2.7V
VCC
VIL
t2VPH
VIH
RP#(P)
VIL

(A)Reset During Read Array Mode

(B)Reset During Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration

(C)RP# rising Timing

Figure 20. AC Waveform for Reset Operation

Reset AC Specifications

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RP# Pulse Low Time	2	100		ns
t_{PLRZ}	RP# Low to Reset during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration	1,2		30	µs
t_{2VPH}	V_{CC} 2.7V to RP# High	2,3	100		ns

NOTES:

1. If RP# is asserted while a block erase, full chip erase, word/byte write or lock-bit configuration operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the later of RY/BY#(SR.7) going High Z("1") or RP# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
3. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE, FULL CHIP ERASE, WORD/BYTE WRITE AND LOCK-BIT CONFIGURATION PERFORMANCE(3)

V_{CC}=2.7V-3.6V, T_A=0°C to +70°C

Sym.	Parameter		Notes	V_{CCW}=2.7V-3.6V		V_{CCW}=11.7V-12.3V		Unit
				Typ.(1)	Max.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K word Block	2	33	200	20		µs
		4K word Block	2	36	200	27		µs
	Byte Write Time	64K byte Block	2	31	200	19		µs
		8K byte Block	2	32	200	26		µs
	Block Write Time (In word mode)	32K word Block	2	1.1	4	0.66		s
		4K word Block	2	0.15	0.5	0.12		s
	Block Write Time (In byte mode)	64K byte Block	2	2.2	7	1.4		s
		8K byte Block	2	0.3	1	0.25		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block 64K byte Block	2	1.2	6	0.9		s
		4K word Block 8K byte Block	2	0.6	5	0.5		s
	Full Chip Erase Time		2	84	420	64		s
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time		2	56	200	42		µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time		2	1	5	0.69		s
t_{WHRZ1} t_{EHRZ1}	Word/Byte Write Suspend Latency Time to Read		4	6	15	6	15	µs
t_{WHRZ2} t_{EHRZ2}	Block Erase Suspend Latency Time to Read		4	16	30	16	30	µs

NOTES:

1. Typical values measured at T_A=+25°C and V_{CC}=3.0V, V_{CCW}=3.0V or 12.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.
4. A latency time is required from issuing suspend command(WE# or CE# going high) until RY/BY# going High Z or SR.7 going "1".

7 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1142

2. Markings

2－1. Marking contents

(1) Product name : LH28F320BJE－PTTL90

(2) Company name : SHARP

(3) Date code

(Example) Z YY WW XXX

XXX → Denotes the production ref.code (1~3)

WW → Denotes the production week.
(01,02,03, · · · · ·52,53)

YY → Denotes the production year.
(Lower two digit of the year.)

Z → Denotes the production ref.code
(No marking , A , B , C)

(4) "JAPAN" is marked on the package when both wafer and assembly processes are done in Japan ,indicating the country of origin.

2－2. Marking layout

Refer drawing No.AA1142

(This layout does not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3－1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (50devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (500device/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 72 hours after opening dry packing.

4－4. Baking (drying) before mounting
(1) Baking is necessary
  (A) If the humidity indicator in the desiccant becomes pink
  (B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16~24 hours at 120℃.
Heat resistance tray is used for shipping tray.

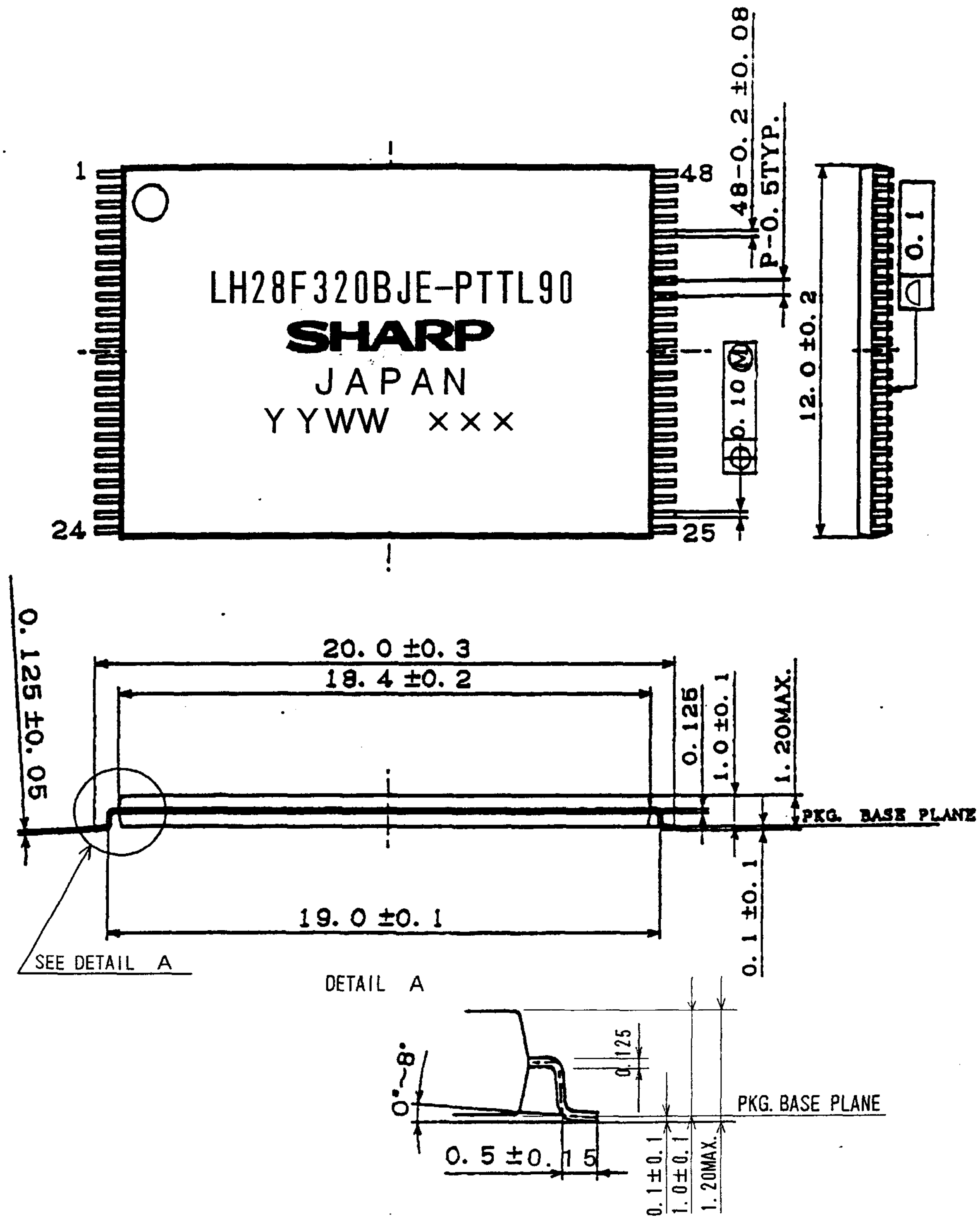
5. Surface Mount Conditions

Please perform the following conditions when mounting ICs not to deteriorate IC quality.

5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

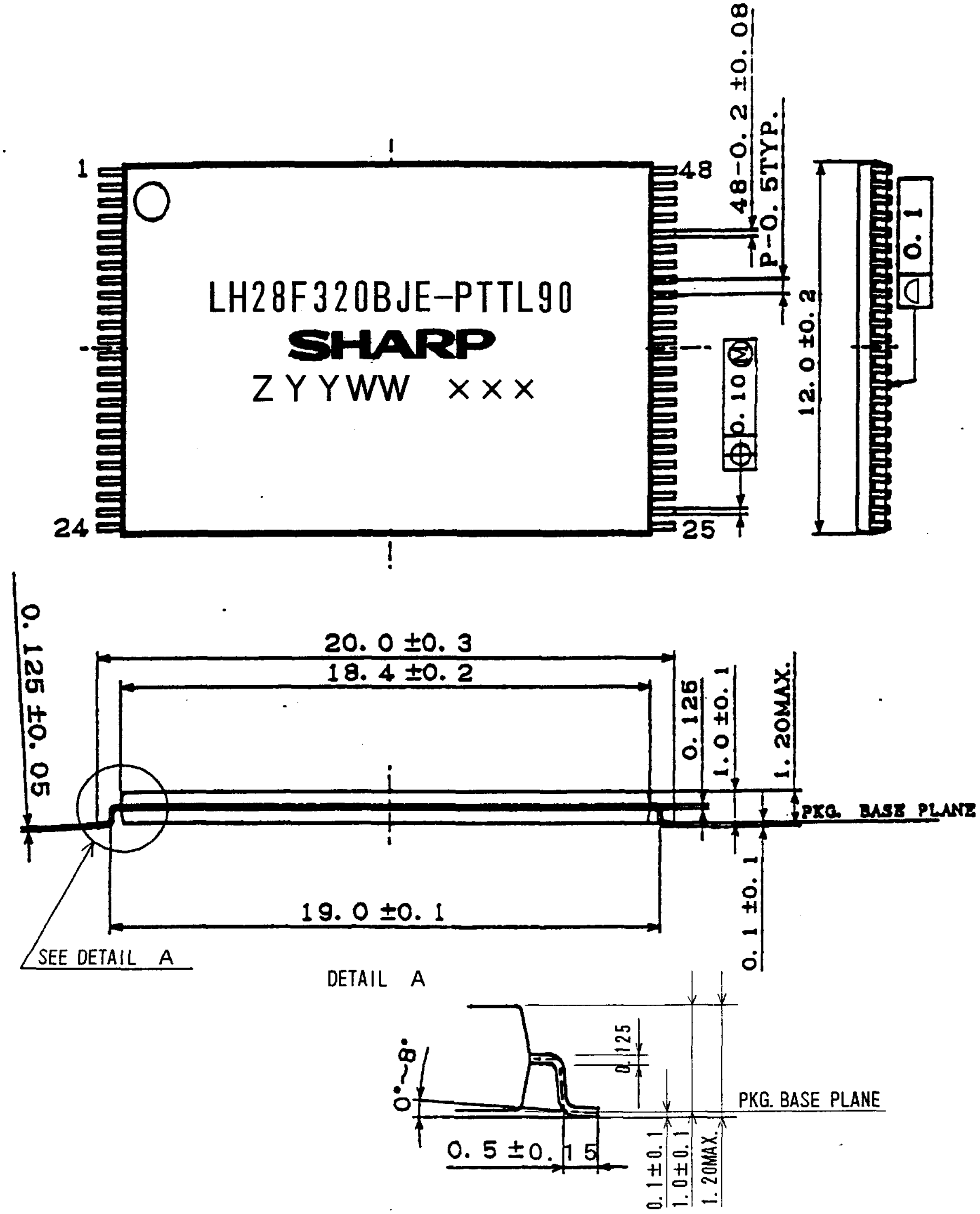
Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 230℃ or less, duration of less than 15 seconds. 200℃ or over,duration of less than 40 seconds. Temperature increase rate of 1～4℃/second	IC package surface
Manual soldering (soldering iron)	260℃ or less, duration of less than 10 seconds.	IC outer lead surface

5－2. Conditions for removal of residual flux
(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃


1
48
24
25
LH28F320BJE-PTTL90
SHARP
JAPAN
YYWW ×××
48-0.2 ±0.08
P-0.5TYP.
0.10 Ⓜ
12.0 ±0.2
0.1
20.0 ±0.3
18.4 ±0.2
19.0 ±0.1
0.125 ±0.05
0.125
1.0 ±0.1
1.20MAX.
0.1 ±0.1
PKG. BASE PLANE
SEE DETAIL A
DETAIL A
0°~8°
0.125
0.5 ±0.15
0.1±0.1
1.0±0.1
1.20MAX.
PKG. BASE PLANE

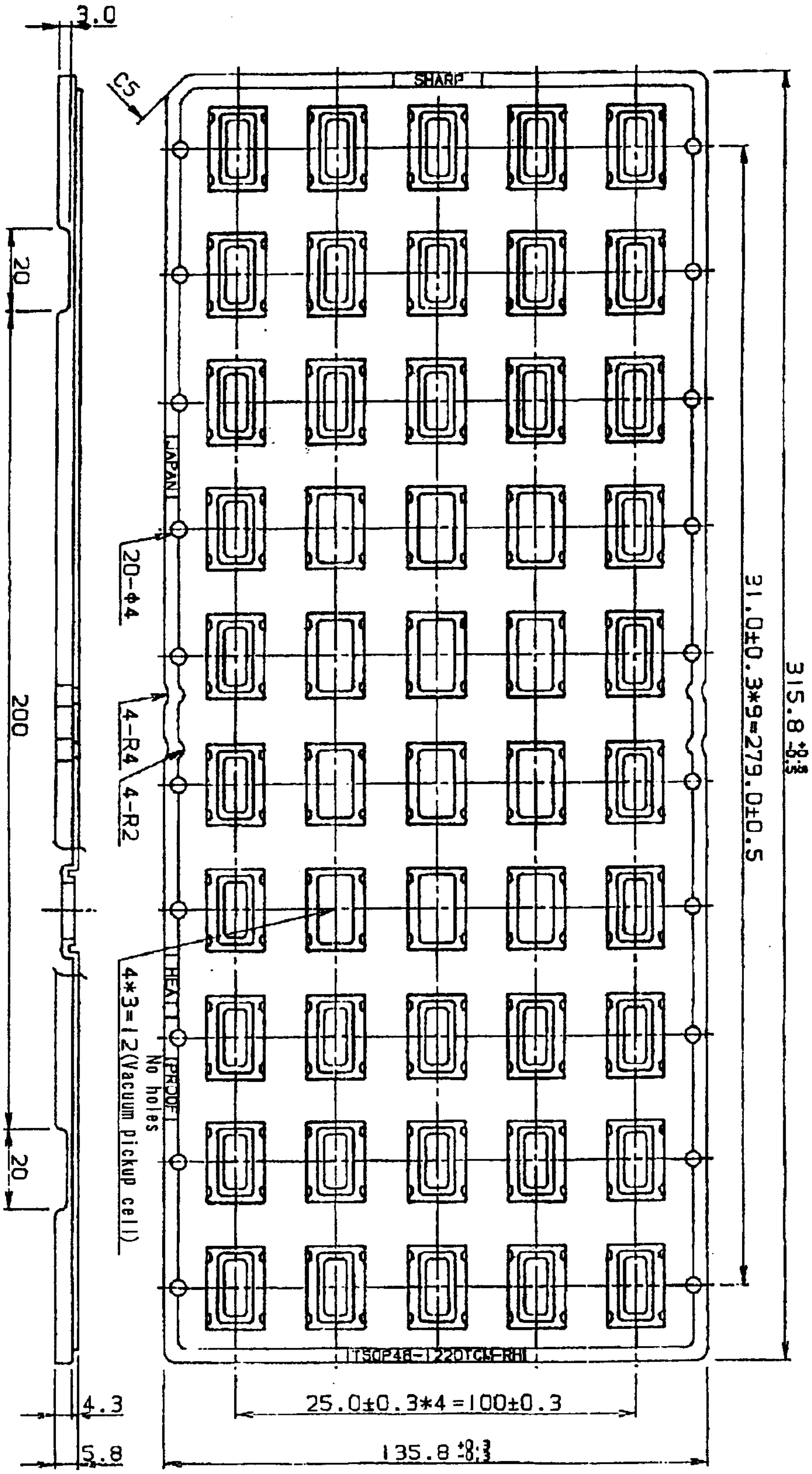
注記 ：『JAPAN』表記がある場合のマーク仕様
NOTES：Marking specification when “JAPAN”is marked.

名称 NAME	TSOP48-P-1220	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE	プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
		単位			


1
48
24
25
LH28F320BJE-PTTL90
SHARP
ZYYWW ×××
48-0.2 ±0.08
P-0.5TYP.
0.10 Ⓜ
0.1
12.0 ±0.2
0.125 ±0.05
20.0 ±0.3
18.4 ±0.2
0.125
1.0 ±0.1
1.20MAX.
PKG. BASE PLANE
0.1 ±0.1
19.0 ±0.1
SEE DETAIL A
DETAIL A
0°~8°
0.125
0.5 ±0.15
PKG. BASE PLANE
0.1±0.1
1.0±0.1
1.20MAX.

注記 ：『ＪＡＰＡＮ』表記がない場合のマーク仕様
NOTES : Marking specification when "JAPAN" is not marked.

名称 NAME	TSOP48-P-1220	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 ﾌﾟﾗｽﾁｯｸﾊﾟｯｹｰｼﾞ外形寸法は、ﾊﾞﾘを含まないものとする。 NOTE Plastic body dimensions do not include burr

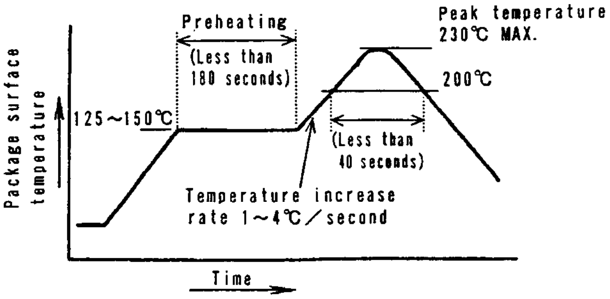

3.0
C5
SHARP
20
200
20
JAPAN
20-φ4
4-R4
4-R2
4*3=12(Vacuum pickup cell)
No holes
HEAT PROOF
31.0±0.3*9=279.0±0.5
315.8 +0.3 -0.3
TSOP48-1220TCM-RH
4.3
5.8
25.0±0.3*4=100±0.3
135.8 +0.3 -0.3

名称 NAME	TSOP48−1220TCM−RH	備考 NOTE
	単位	

《Supplementary data》

LHF32J02 Recommended mounting conditions for two time reflow soldering .	
Product name(Package)	LH28F320BJE-PTTL90(TSOP48-P-1220)
Packing specification	Tray (Dry packing)
Mounting method	Reflow soldering (Air)
Reflow soldering conditions	Peak temperature of 230℃ or less. 200℃ or over, duration of less than 40 seconds. Preheat temperature of 125～150℃, duration of less than 180 seconds. Temperature increase rate of 1～4℃/second.
Measurement point	IC package surface
Storage conditions	After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less. If doing reflow soldering twice, do the first reflow soldering within 72 hours after opening dry packing and do the second reflow soldering within 72 hours after the first reflow soldering.
Note	If the above storage conditions are not applicable, bake it before reflow soldering. The recommended conditions are 16~24 hours at 120℃. (Heat resistance tray is used for shipping tray.)

Recommended Reflow Soldering(Air) Temperature Profile



ADDITIONAL INFORMATION

1 Block Erase Suspend and Resume command

If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than 15ms and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

RELATED DOCUMENT INFORMATION[1]

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE :

1. International customers should contact their local SHARP or distribution sales office.