

LH28F400SU-NC

4M (512K × 8, 256K × 16)
Flash Memory

FEATURES

- User-Configurable x8 or x16 Operation
- 5 V Write/Erase Operation (5 V V_{PP})
 - No Requirement for DC/DC Converter to Write/Erase
- 60 ns Maximum Access Time ($V_{CC} = 5.0 V \pm 0.25 V$)
- 80ns Maximum Access Time ($V_{CC} = 5.0 V \pm 0.5 V$)
- 32 Independently Lockable Blocks (16K)
- 100,000 Erase Cycles per Block
- Automated Byte Write/Block Erase
 - Command User Interface
 - Status Register
 - $\overline{RY}/\overline{BY}$ Status Output
- System Performance Enhancement
 - Erase Suspend for Read
 - Two-Byte Write
 - Full Chip Erase
- Data Protection
 - Hardware Erase/Write Lockout during Power Transitions
 - Software Erase/Write Lockout
- Independently Lockable for Write/Erase on Each Block (Lock Block and Protect Set/Reset)
- 5 μA (Typ.) I_{CC} in CMOS Standby
- 0.2 μA (Typ.) Deep Power-Down
- State-of-the-Art 0.45 μm ETOX™ Flash Technology
- 56-Pin, 1.2 mm × 14 mm × 20 mm TSOP (Type I) Package
- 48-Pin, 1.2 mm × 12 mm × 18 mm TSOP (Type I) Package
- 44-Pin, 600-mil SOP Package

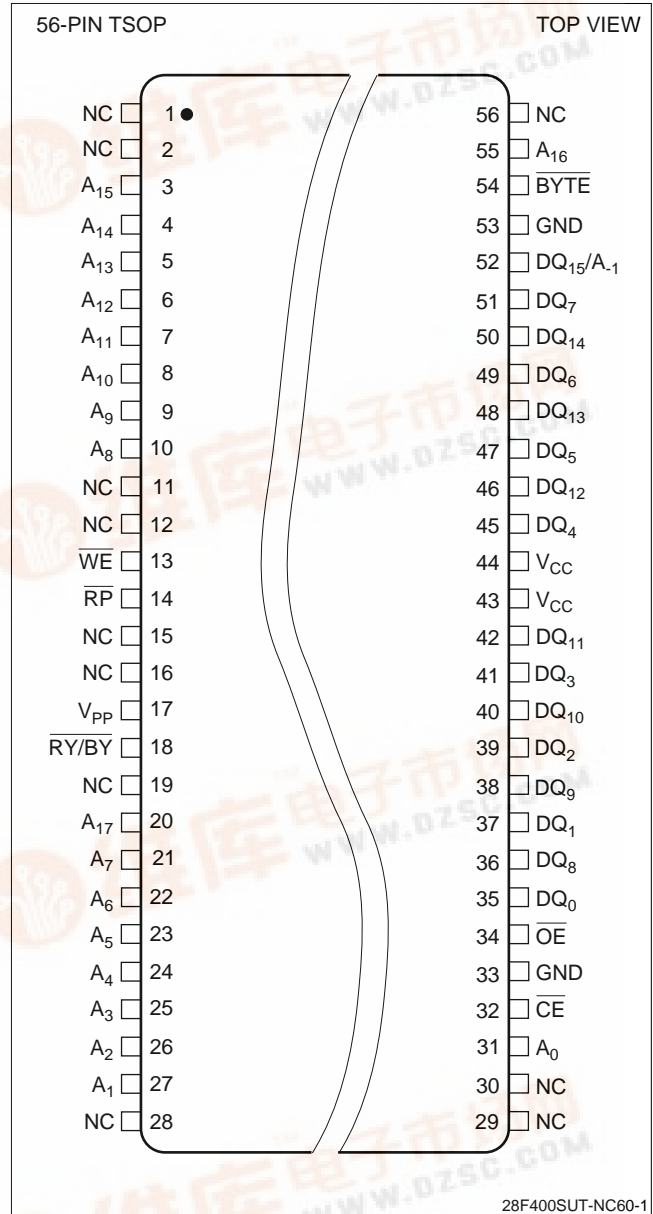


Figure 1. 56-Pin TSOP Configuration

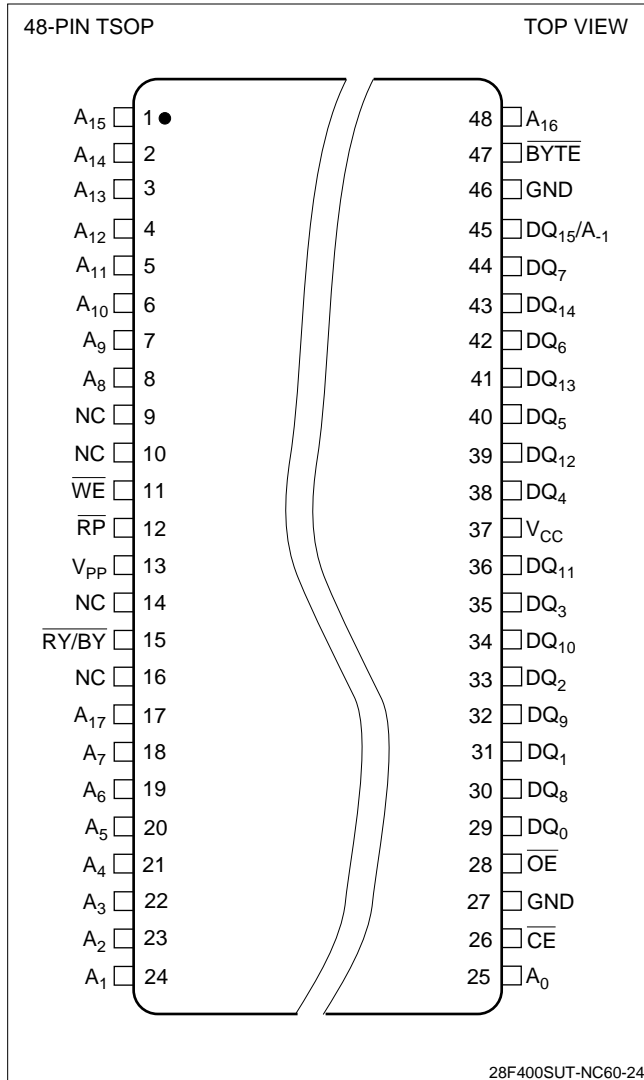


Figure 2. 48-Pin TSOP Configuration

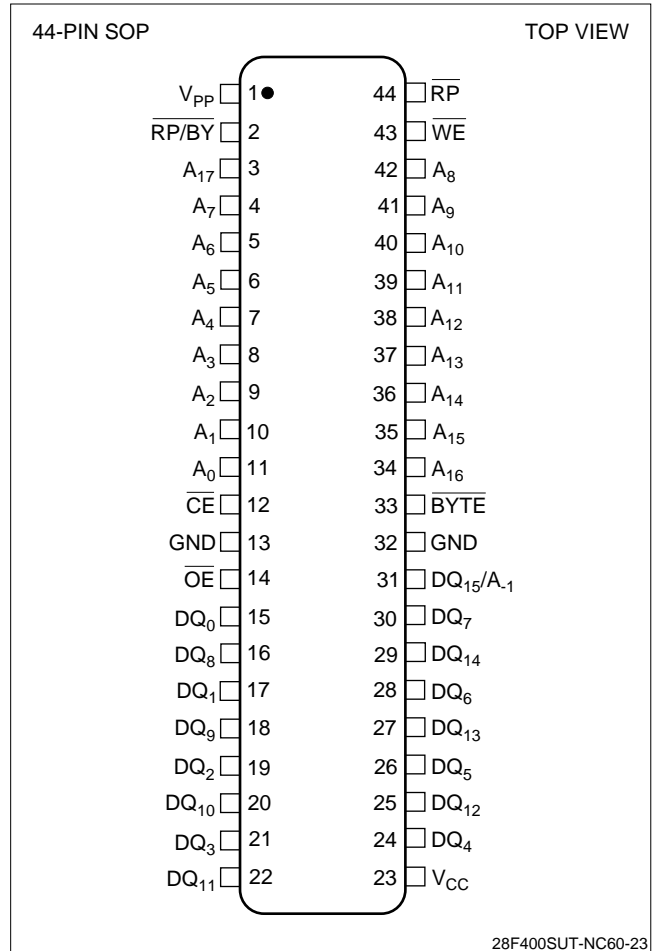
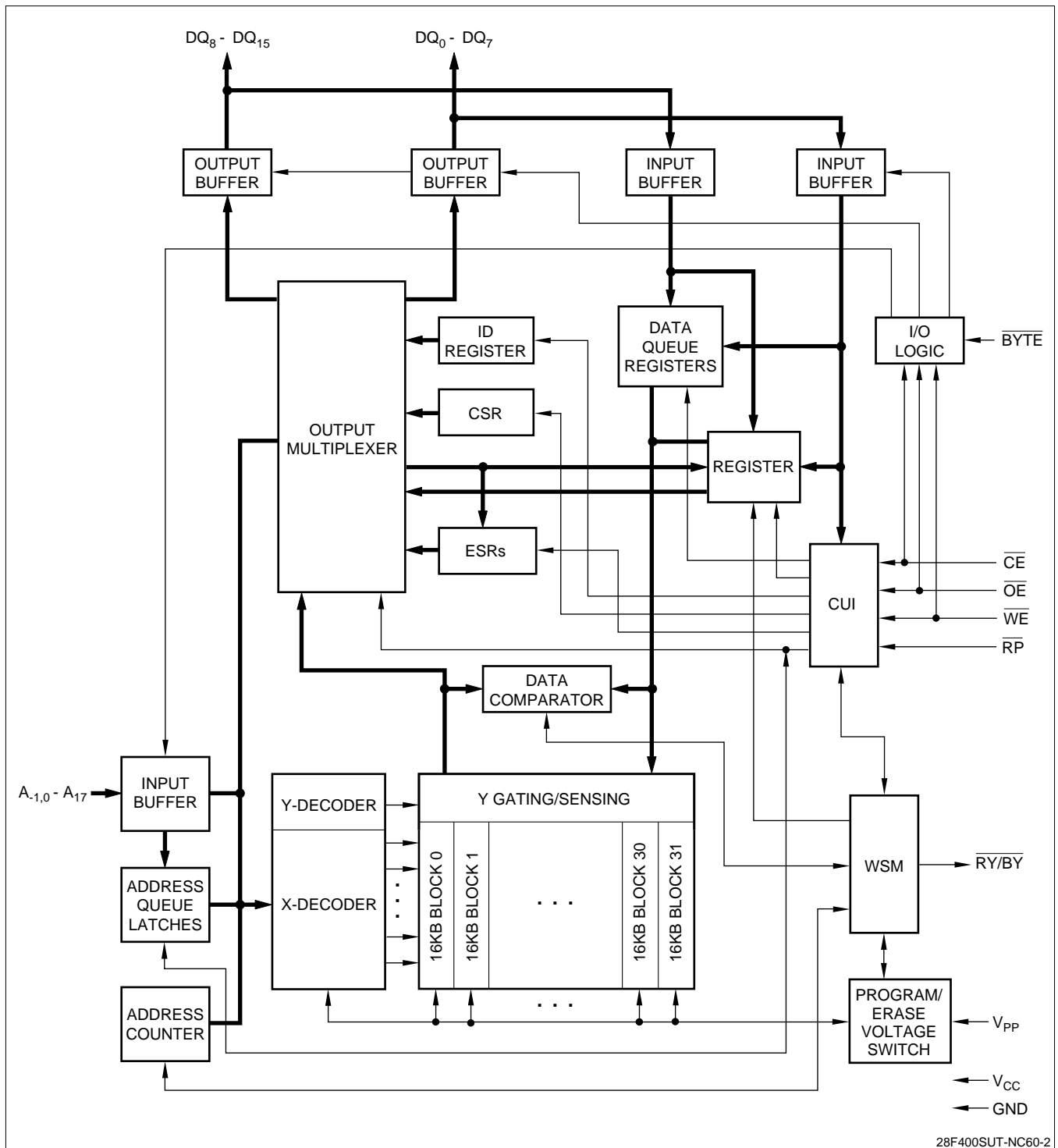


Figure 3. 44-Pin SOP Configuration



28F400SUT-NC60-2

Figure 4. LH28F400SU-NC Block Diagram

PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
DQ ₁₅ - A ₋₁	INPUT	BYTE-SELECT ADDRESSES: Selects between high and low byte when device is in x8 mode. This address is latched in x8 Data Writes. Not used in x16 mode (i.e., the DQ ₁₅ /A ₋₁ input buffer is turned off when BYTE is high).
A ₀ - A ₁₂	INPUT	WORD-SELECT ADDRESSES: Select a word within one 16K block. These addresses are latched during Data Writes.
A ₁₃ - A ₁₇	INPUT	BLOCK-SELECT ADDRESSES: Select 1 of 32 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ ₀ - DQ ₇	INPUT/OUTPUT	LOW-BYTE DATA BUS: Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ ₈ - DQ ₁₅	INPUT/OUTPUT	HIGH-BYTE DATA BUS: Inputs data during x16 Data Write operations. Outputs array, buffer or identifier data in the appropriate Read mode; not used for Status register reads. Floated when the chip is de-selected or the outputs are disabled. DQ ₁₅ /A ₋₁ is address.
$\overline{\text{CE}}$	INPUT	CHIP ENABLE INPUT: Activate the device's control logic, input buffers, decoders and sense amplifiers. $\overline{\text{CE}}$ must be low to select the device.
$\overline{\text{RP}}$	INPUT	RESET/POWER-DOWN: With $\overline{\text{RP}}$ low, the device is reset, any current operation is aborted and device is put into the deep power down mode. When the power is turned on, $\overline{\text{RP}}$ pin is turned to low in order to return the device to default configuration. When the power transition is occurred, or the power on/off, $\overline{\text{RP}}$ is required to stay low in order to protect data from noise. When returning from Deep Power-Down, a recovery time of 430 ns is required to allow these circuits to power up. When $\overline{\text{RP}}$ goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status registers return to ready (with all status flags cleared). After returning, the device is in read array mode.
$\overline{\text{OE}}$	INPUT	OUTPUT ENABLE: Gates device data through the output buffers when low. The outputs float to tri-state off when $\overline{\text{OE}}$ is high.
$\overline{\text{WE}}$	INPUT	WRITE ENABLE: Controls access to the CUI, Data Queue Registers and Address Queue Latches. $\overline{\text{WE}}$ is active low, and latches both address and data (command or array) on its rising edge.
$\overline{\text{RY}}/\overline{\text{BY}}$	OPEN DRAIN OUTPUT	READY/BUSY: Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. When the WSM is ready for new operation or Erase is Suspended, or the device is in deep power-down mode $\overline{\text{RY}}/\overline{\text{BY}}$ pin is floated.
$\overline{\text{BYTE}}$	INPUT	BYTE ENABLE: $\overline{\text{BYTE}}$ low places device in x8 mode. All data is then input or output on DQ ₀ - DQ ₇ , and DQ ₈ - DQ ₁₅ float. Address A ₋₁ selects between the high and low byte. $\overline{\text{BYTE}}$ high places the device in x16 mode, and turns off the A ₋₁ input buffer. Address A ₀ , then becomes the lowest order address.
V _{PP}	SUPPLY	ERASE/WRITE POWER SUPPLY (5.0 V ±0.5 V): For erasing memory array blocks or writing words/bytes into the flash array.
V _{CC}	SUPPLY	DEVICE POWER SUPPLY (3.3 V ±0.3 V): Do not leave any power pins floating.
GND	SUPPLY	GROUND FOR ALL INTERNAL CIRCUITRY: Do not leave any ground pins floating.
NC		NO CONNECT: No internal connection to die, lead may be driven or left floating.

INTRODUCTION

Sharp's LH28F400SU-NC 4M Flash Memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, 5 V single voltage operation and very high read/write performance, the LH28F400SU-NC is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F400SU-NC's independently lockable 32 symmetrical blocked architecture (16K each) extended cycling, low power operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for cellular phone, facsimile, game, PC, printer and handy terminal. The LH28F400SU-NC's single power supply operation enables the design of memory cards which can be read/written in 5.0 V systems. Its x8/x16 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.45 μm ETOX™ process technology, the LH28F400SU-NC is the most cost-effective, high-density 5.0V flash memory.

DESCRIPTION

The LH28F400SU-NC is a high performance 4M (4,194,304) block erasable non-volatile random access memory organized as either 256K × 16 or 512K × 8. The LH28F400SU-NC includes thirty-two 16K (16,384) blocks. A chip memory map is shown in Figure 5.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Among the significant enhancements of the LH28F400SU-NC:

- 5 V Read, Write/Erase Operation (5 V V_{CC} , V_{PP})
- Low Power Capability
- Improved Write Performance
- Dedicated Block Write/Erase Protection
- Command-Controlled Memory Protection Set/Reset Capability

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows Byte Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the LH28F008SA 8M Flash Memory.

A Superset of commands have been added to the basic LH28F008SA command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Software Locking of Memory Blocks
- Memory Protection Set/Reset Capability
- Two-Byte Serial Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed typically within 13 μs per byte or within 20 μs per word. A Block Erase operation erases one of the 32 blocks in typically 0.6 seconds, independent of the other blocks.

LH28F400SU-NC allows to erase all unlocked blocks. It is desirable in case of which you have to implement Erase operation maximum 32 times.

Only in x8 mode, LH28F400SU-NC enables Two-Byte Serial Write which is operated by three times command input. Writing of memory data is performed typically within 20 μs per two-byte. This feature can improve 8-bit system write performance by up to typically 10 μs per byte.

All operations are started by a sequence of Write commands to the device. Status Register (described in detail later) and a RY/BY output pin provide information on the progress of the requested operation.

Same as the LH28F008SA, LH28F400SU-NC requires an operation to complete before the next operation can be requested, also it allows to suspend block erase to read data from any other block, and allow to resume erase operation.

The LH28F400SU-NC provides user-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable OS or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the LH28F400SU-NC has a software controlled master Write Protect circuit which prevents any modifications to memory blocks whose lock-bits are set.

When the device power-up or \overline{RP} turns High, Write Protect Set/Confirm command must be written. Otherwise, all lock bits in the device remain being locked, can't perform the Write to each block and single Block Erase. Write Protect Set/Confirm command must be written to reflect the actual lock status. However, when the device power-on or \overline{RP} turns High, Erase All Unlocked Blocks can be used. If used, Erase is performed with reflecting actual lock status, and after that Write and Block Erase can be used.

The LH28F400SU-NC contains a Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA Flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F004SUT-NC from a LH28F008SA-based design.

The LH28F400SU-NC incorporates an open drain $\overline{RY}/\overline{BY}$ output pin. This feature allows the user to OR-tie many $\overline{RY}/\overline{BY}$ pins together in a multiple memory configuration such as a Resident Flash Array.

The LH28F400SU-NC is specified for a maximum access time of 60 ns (t_{ACC}) at 5 V operation (4.75 to 5.25 V), and 70 ns (t_{ACC}) at 5 V operation (4.5 to 5.5 V) over the commercial temperature range (0 to +70°C).

The LH28F400SU-NC incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I_{CC} Current is 2 mA at 5 V.

A Deep Power-Down mode of operation is invoked when the \overline{RP} (called \overline{PWD} on the LH28F008SA) pin transitions low, any current operation is aborted and the device is put into the deep power down mode. This mode brings the device power consumption to less than 5 μ A and provides additional write protection by acting as a device reset pin during power transitions. When the power is turned on, \overline{RP} pin is turned to low in order to return the device to default configuration. When the power transition is occurred, or at the power on/off \overline{RP} pin is required to stay low in order to protect data from noise. A recovery time of 480 ns is required from \overline{RP} switching high until outputs are again valid. In the Deep Power-Down State, the WSM is reset (any current operation will abort) and the CSR register is cleared.

A CMOS Standby mode of operation is enabled when \overline{CE} transitions high and \overline{RP} stays high with all input control pins at CMOS levels. In this mode, the device draws an I_{CC} standby current of 10 μ A.

MEMORY MAP

7FFFFH		
7C000H	16KB BLOCK	31
7BFFFH		
78000H	16KB BLOCK	30
77FFFH		
74000H	16KB BLOCK	29
73FFFH		
70000H	16KB BLOCK	28
6FFFFH		
6C000H	16KB BLOCK	27
6BFFFH		
68000H	16KB BLOCK	26
67FFFH		
64000H	16KB BLOCK	25
63FFFH		
60000H	16KB BLOCK	24
5FFFFH		
5C000H	16KB BLOCK	23
5BFFFH		
58000H	16KB BLOCK	22
57FFFH		
54000H	16KB BLOCK	21
53FFFH		
50000H	16KB BLOCK	20
4FFFFH		
4C000H	16KB BLOCK	19
4BFFFH		
48000H	16KB BLOCK	18
47FFFH		
44000H	16KB BLOCK	17
43FFFH		
40000H	16KB BLOCK	16
3FFFFH		
3C000H	16KB BLOCK	15
3BFFFH		
38000H	16KB BLOCK	14
37FFFH		
34000H	16KB BLOCK	13
33FFFH		
30000H	16KB BLOCK	12
2FFFFH		
2C000H	16KB BLOCK	11
2BFFFH		
28000H	16KB BLOCK	10
27FFFH		
24000H	16KB BLOCK	9
23FFFH		
20000H	16KB BLOCK	8
1FFFFH		
1C000H	16KB BLOCK	7
1BFFFH		
18000H	16KB BLOCK	6
17FFFH		
14000H	16KB BLOCK	5
13FFFH		
10000H	16KB BLOCK	4
0FFFFH		
0C000H	16KB BLOCK	3
0BFFFH		
08000H	16KB BLOCK	2
07FFFH		
04000H	16KB BLOCK	1
03FFFH		
00000H	16KB BLOCK	0

NOTE:
 In Byte-wide (x8) mode A_1 is the lowest order address.
 In Word-wide (x16) mode A_1 don't care, address values are ignored A_1 .

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Figure 5. Memory Map

BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS**Bus Operations for Word-Wide Mode ($\overline{\text{BYTE}} = V_{\text{IH}}$)**

MODE	$\overline{\text{RP}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A_0	DQ_{0-15}	$\overline{\text{RY}}/\overline{\text{BY}}$	NOTE
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X	1, 2, 7
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	X	1, 6, 7
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	X	1, 6, 7
Deep Power-Down	V_{IL}	X	X	X	X	High-Z	V_{OH}	1, 3
Manufacturer ID	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	00B0H	V_{OH}	4
Device ID	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	ID	V_{OH}	4
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X	1, 5, 6

Bus Operations for Byte-Wide Mode ($\overline{\text{BYTE}} = V_{\text{IL}}$)

MODE	$\overline{\text{RP}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A_0	DQ_{0-7}	$\overline{\text{RY}}/\overline{\text{BY}}$	NOTE
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X	1, 2, 7
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	X	1, 6, 7
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	X	1, 6, 7
Deep Power-Down	V_{IL}	X	X	X	X	High-Z	V_{OH}	1, 3
Manufacturer ID	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	B0H	V_{OH}	4
Device ID	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	ID	V_{OH}	4
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X	1, 5, 6

NOTES:

- X can be V_{IH} or V_{IL} for address or control pins except for $\overline{\text{RY}}/\overline{\text{BY}}$, which is either V_{OL} or V_{OH} .
- $\overline{\text{RY}}/\overline{\text{BY}}$ output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, $\overline{\text{RY}}/\overline{\text{BY}}$ will be at V_{OL} if it is tied to V_{CC} through a resistor. When the $\overline{\text{RY}}/\overline{\text{BY}}$ at V_{OL} is independent of $\overline{\text{OE}}$ while a WSM operation is in progress.
- $\overline{\text{RP}}$ at $\text{GND} \pm 0.2 \text{ V}$ ensures the lowest deep power-down current.
- A_0 at V_{IL} provide manufacturer ID codes. A_0 at V_{IH} provide device ID codes. Device ID code= 21H (x8). Device ID Code = 6621H (x16). All other addresses are set to zero.
- Commands for different Erase operations, Data Write operations, and Lock-Block operations can only be successfully completed when $V_{\text{PP}} = V_{\text{PPH}}$.
- While the WSM is running, $\overline{\text{RY}}/\overline{\text{BY}}$ in Level-Mode (default) stays at V_{OL} until all operations are complete. $\overline{\text{RY}}/\overline{\text{BY}}$ goes to V_{OH} when the WSM is not busy or in erase suspend mode.
- $\overline{\text{RY}}/\overline{\text{BY}}$ may be at V_{OL} while the WSM is busy performing various operations. For example, a status register read during a write operation.
- Only to $\overline{\text{RP}}$, $V_{\text{IH}} (\text{MIN.}) = 2.4 \text{ V}$ at TTL-level input.

LH28F008SA-Compatible Mode Command Bus Definitions

COMMAND	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTE
	OPER.	ADDRESS	DATA	OPER.	ADDRESS	DATA	
Read Array	Write	X	FFH	Read	AA	AD	
Intelligent Identifier	Write	X	90H	Read	IA	ID	1
Read Compatible Status Register	Write	X	70H	Read	X	CSRD	2
Clear Status Register	Write	X	50H				3
Word Write	Write	X	40H	Write	WA	WD	
Alternate Word Write	Write	X	10H	Write	WA	WD	
Block Erase/Confirm	Write	X	20H	Write	BA	D0H	4
Erase Suspend/Resume	Write	X	B0H	Write	X	D0H	4

ADDRESS

AA = Array Address
 BA = Block Address
 IA = Identifier Address
 WA = Write Address
 X = Don't Care

DATA

AD = Array Data
 CSRD = CSR Data
 ID = Identifier Data
 WD = Write Data

NOTES:

- Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.
- The CSR is automatically available after device enters Data Write, Erase or Suspend operations.
- Clears CSR.3, CSR.4, and CSR.5. See Status register definitions.
- While device performs Block Erase, if you issue Erase Suspend command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase (ESS = 0, WSMS = 1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase Suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase complete.

LH28F400SU-NC Performance Enhancement Command Bus Definitions

COMMAND	MODE	FIRST BUS CYCLE			SECOND BUS CYCLE			THIRD BUS CYCLE			NOTE
		OPER.	ADD.	DATA	OPER.	ADD.	DATA	OPER.	ADD.	DATA	
Protect Set/Confirm		Write	X	57H	Write	0FFH	D0H				1, 2
Protect Reset/Confirm		Write	X	47H	Write	0FFH	D0H				3
Lock Block/Confirm		Write	X	77H	Write	BA	D0H				1, 2, 4
Erase All Unlocked Blocks		Write	X	A7H	Write	X	D0H				1, 2
Two-Byte Write	x8	Write	X	FBH	Write	A ₁	WD (L, H)	Write	WA	WD (H, L)	1, 2, 5

ADDRESS

BA = Block Address
 WA = Write Address
 X = Don't Care

DATA

AD = Array Data
 WD (L, H) = Write Data (Low, High)
 WD (H, L) = Write Data (High, Low)

NOTES:

- After initial device power-up, or return from deep power-down mode, the block lock status bits default to the locked state independent of the data in the corresponding lock bits. In order to upload the lock bit status, it requires to write Protect Set/Confirm command.
- To reflect the actual lock-bit status, the Protect Set/Confirm command must be written after Lock Block/Confirm command.
- When Protect Reset/Confirm command is written, all blocks can be written and erased regardless of the state of the lock-bits.
- The Lock Block/Confirm command must be written after Protect Reset/Confirm command was written.
- A₁ is automatically complemented to load second byte of data. A₁ value determines which WD is supplied first: A₁ = 0 looks at the WDL, A₁ = 1 looks at the WDH. In word-wide (x16) mode A₁, don't care.
- Second bus cycle address of Protect Set/Confirm and Protect Reset/Confirm command is 0FFH. Specifically A₉ - A₈ = 0, A₇ - A₀ = 1, others are don't care.

Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

<p>CSR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>CSR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase in Progress/Completed</p> <p>CSR.5 = ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful Block Erase</p> <p>CSR.4 = DATA-WRITE STATUS (DWS) 1 = Error in Data Write 0 = Data Write Successful</p> <p>CSR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK</p>	<p>NOTES:</p> <ol style="list-style-type: none"> 1. $\overline{RY}/\overline{BY}$ output or WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success. 2. If DWS and ES are set to '1' during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again. 3. The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data-Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PP}L and V_{PP}H. 4. CSR.2 - CSR.0 = Reserved for further enhancements. These bits are reserved for future use and should be masked out when polling the CSR.
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4M FLASH MEMORY SOFTWARE ALGORITHMS

Overview

With the advanced Command User Interface, its Performance Enhancement commands and Status Registers, the software code required to perform a given operation may become more intensive but it will result in much higher write/erase performance compared with current flash memory architectures.

The software flowcharts describing how a given operation proceeds are shown here. Figures 4 through 6 depict flowcharts using the 2nd generation flash device in the LH28F008SA-compatible mode. Figures 7 through 12 depict flowcharts using the 2nd generation flash device's performance enhancement commands mode.

When the device power-up or the device is reset by \overline{RP} pin, all blocks come up locked. Therefore, Word/Byte Write, Two Byte Serial Write and Block Erase can not be performed in each block. However, at that time, Erase All Unlocked Block is performed normally, if used, and reflect actual lock status, also the unlocked block data is erased. When the device power-up or the device is reset by \overline{RP} pin, SetWrite Protect command must be written to reflect actual block lock status.

Reset Write Protect command must be written before Write Block Lock command. To reflect actual block lock status, Set Write Protect command is succeeded.

The Compatible Status Register (CSR) is used to determine which blocks are locked. In order to see Lock Status of a certain block, a Word/Byte Write command (WA = Block Address, WD = FHH) is written to the CUI, after issuing Set Write Protect command. If CSR.7, CSR.5 and CSR.4 (WSMS, ES and DWS) are set to '1's, the block is locked. If CSR.7 is set to '1', the block is not locked.

Reset Write Protect command enables Write/Erase operation to each block.

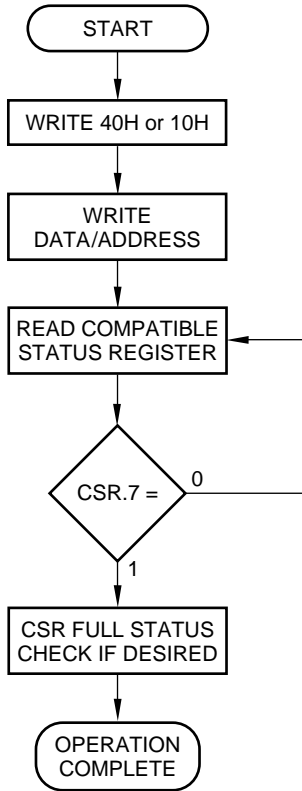
In the case of Block Erase is performed, the block lock information is also erased. Block Lock command and SetWrite Protect command must be written to prohibit Write/Erase operation to each block.

There are unassigned commands. It is not recommended that the customer use any command other than the valid commands specified in "Command Bus Definitions". Sharp reserved the right to redefine these codes for future functions.

Please do not execute reprogramming 0 for the bit which has already been programmed 0. Overwrite operation may generate unerasable bit. In case of reprogramming 0 to the Byte data which has been programmed 1.

- Program 0 for the bit in which you want to change data from 1 to 0.
- Program 1 for the bit which has already been programmed 0.

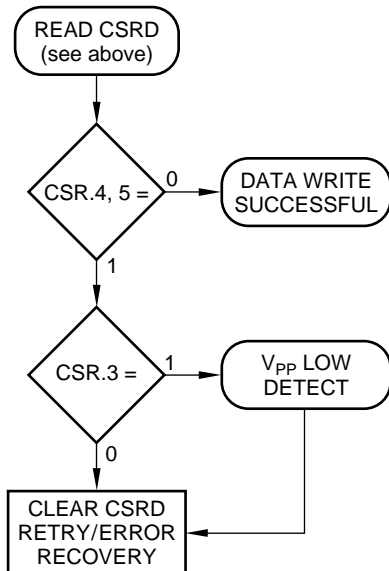
For example, changing Byte data from 10111101 to 10111100 requires 11111110 programming.



BUS OPERATION	COMMAND	COMMENTS
Write	Word/Byte Write	D = 40H or 10H A = X
Write		D = WD A = WA
Read		Q = CSRD Toggle \overline{CE} or \overline{OE} to update CSR.D. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Word/Byte Writes.
 CSR Full Status Check can be done after each Word/Byte Write, or after a sequence of Word/Byte Writes.
 Write FFH after the last operation to reset device to read array mode.
 See Command Bus Cycle notes for description of codes.

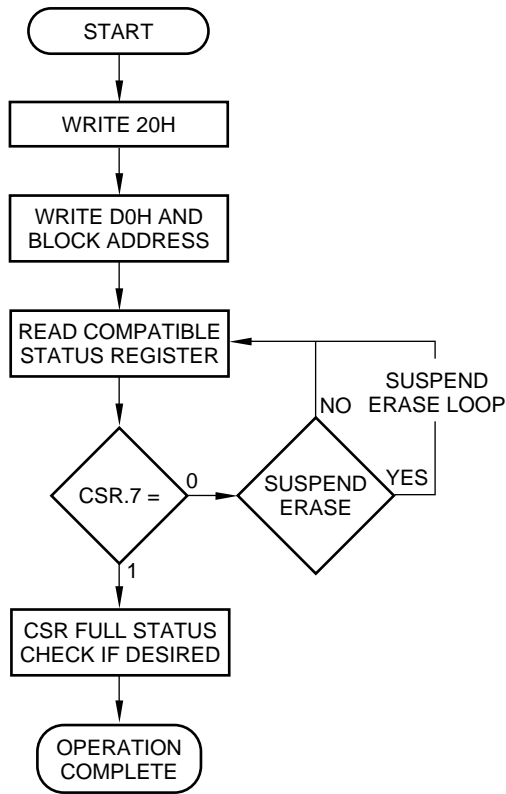
CSR FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check CSR.4, 5 1 = Data Write Unsuccessful 0 = Data Write Successful
Standby		Check CSR.3 1 = V _{PP} Low Detect 0 = V _{PP} OK

CSR.3, 4, 5 should be cleared, if set, before further attempts are initiated.

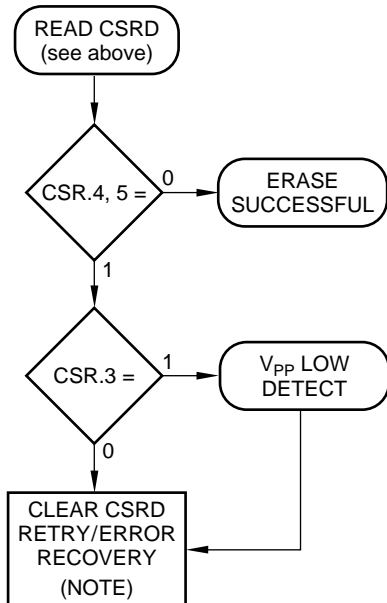
Figure 6. Word/Byte Writes with Compatible Status Register



BUS OPERATION	COMMAND	COMMENTS
Write	Block Erase	D = 20H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSR.D Toggle \overline{CE} or \overline{OE} to update CSR.D. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Block Erasures.
 CSR Full Status Check can be done after each Block Erase, or after a sequence of Block Erasures.
 Write FFH after the last operation to reset device to read array mode.
 See Command Bus Cycle notes for description of codes.

CSR FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check CSR.4, 5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V _{PP} Low Detect 0 = V _{PP} OK

CSR.3, 4, 5 should be cleared, if set, before further attempts are initiated.

NOTE:

- If CSR.3 (VPPS) is set to '1', after clearing CSR.3/4/5,
- Issue Reset WP command.
 - Retry Single Block Erase command.
 - Set WP command is issued, if necessary.
- If CSR.3 (VPPS) is set to '0', after clearing CSR.3/4/5,
- Retry Single Block Erase command.
- If power is off or RP is low during erase operation,
- Clear CSR.3/4/5 and issue Reset WP command,
 - Retry Single Block Erase command.
 - Set WP command is issued, if necessary.

Figure 7. Block Erase with Compatible Status Register

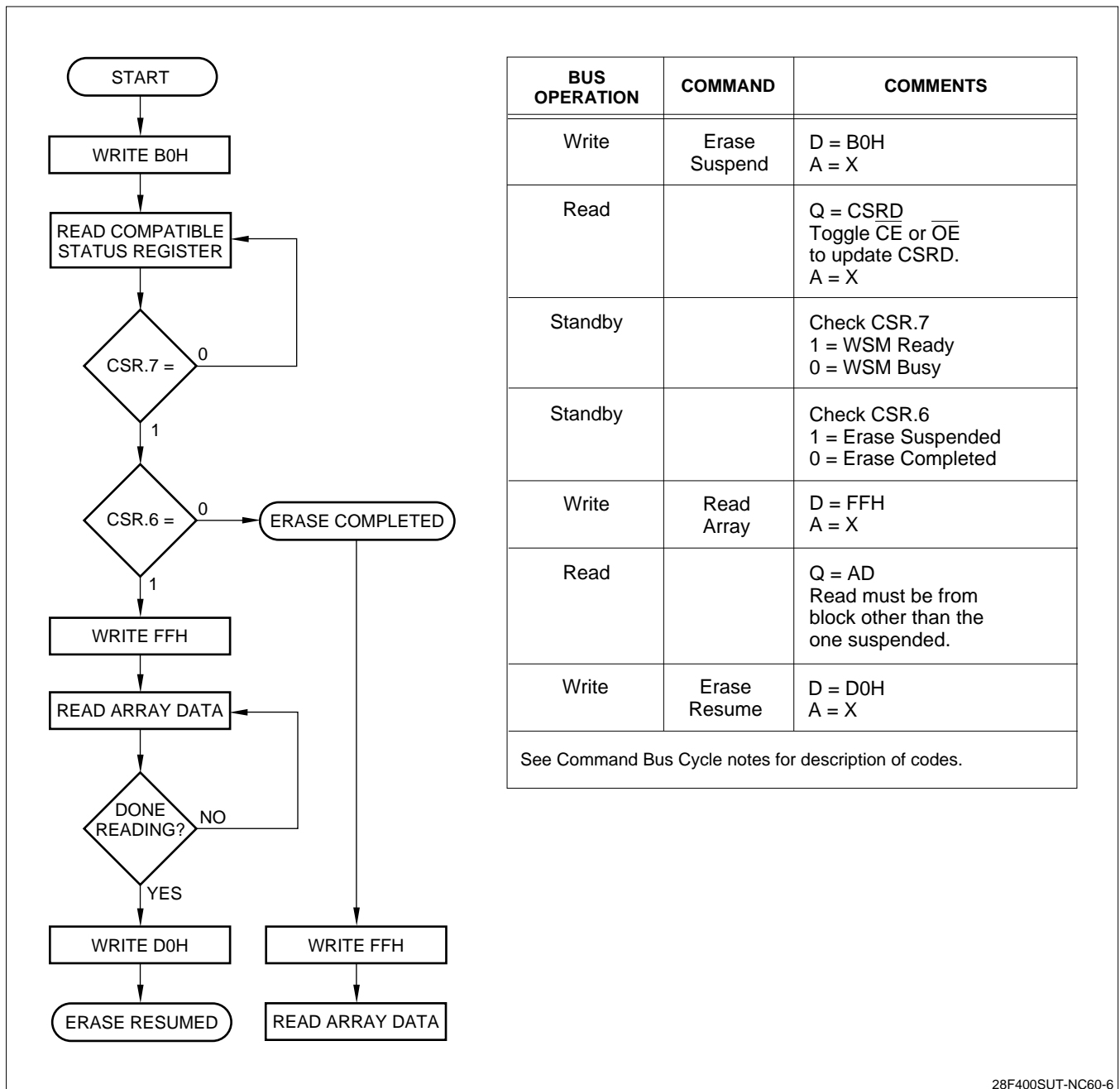


Figure 8. Erase Suspend to Read Array with Compatible Status Register

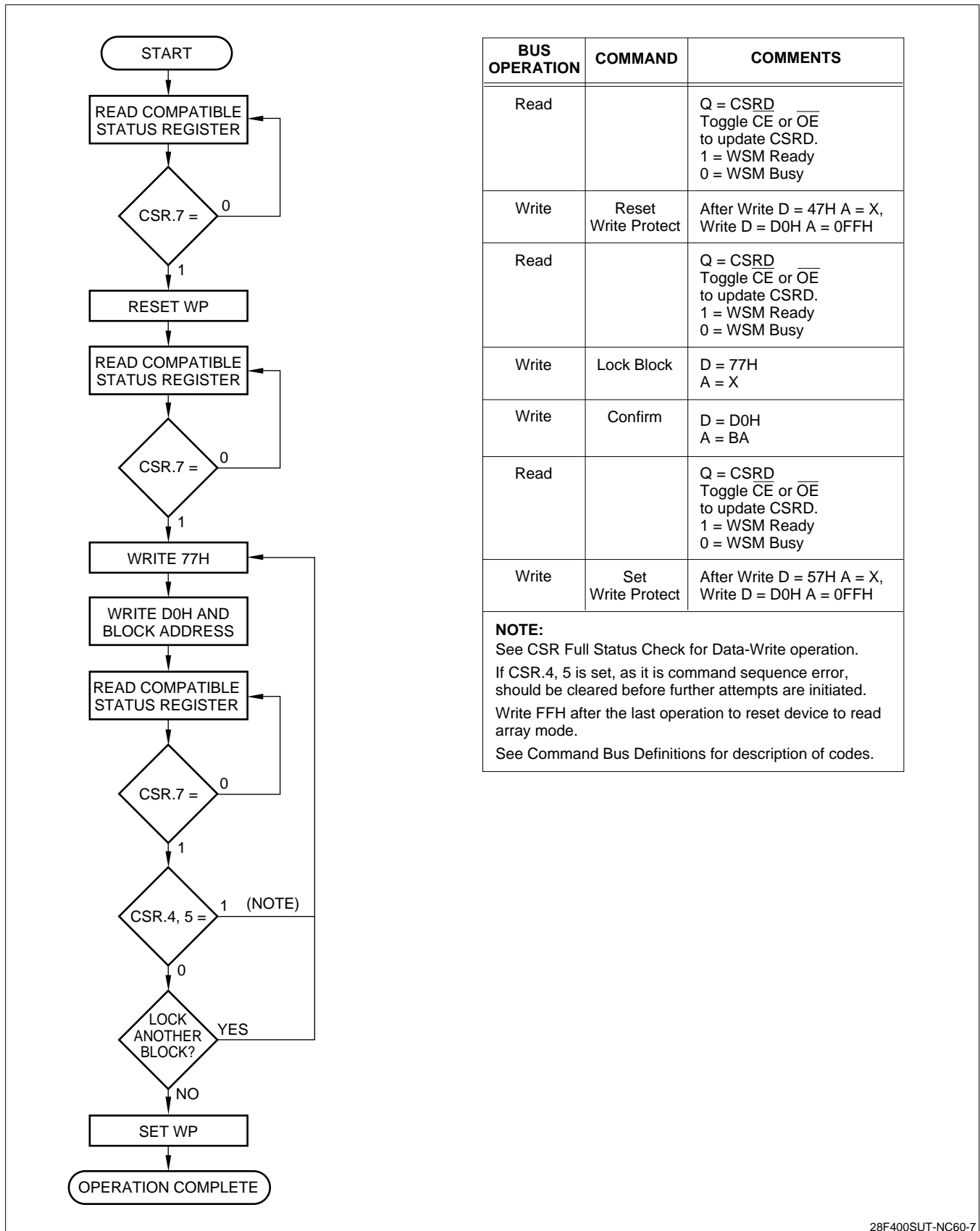


Figure 9. Block Locking Scheme

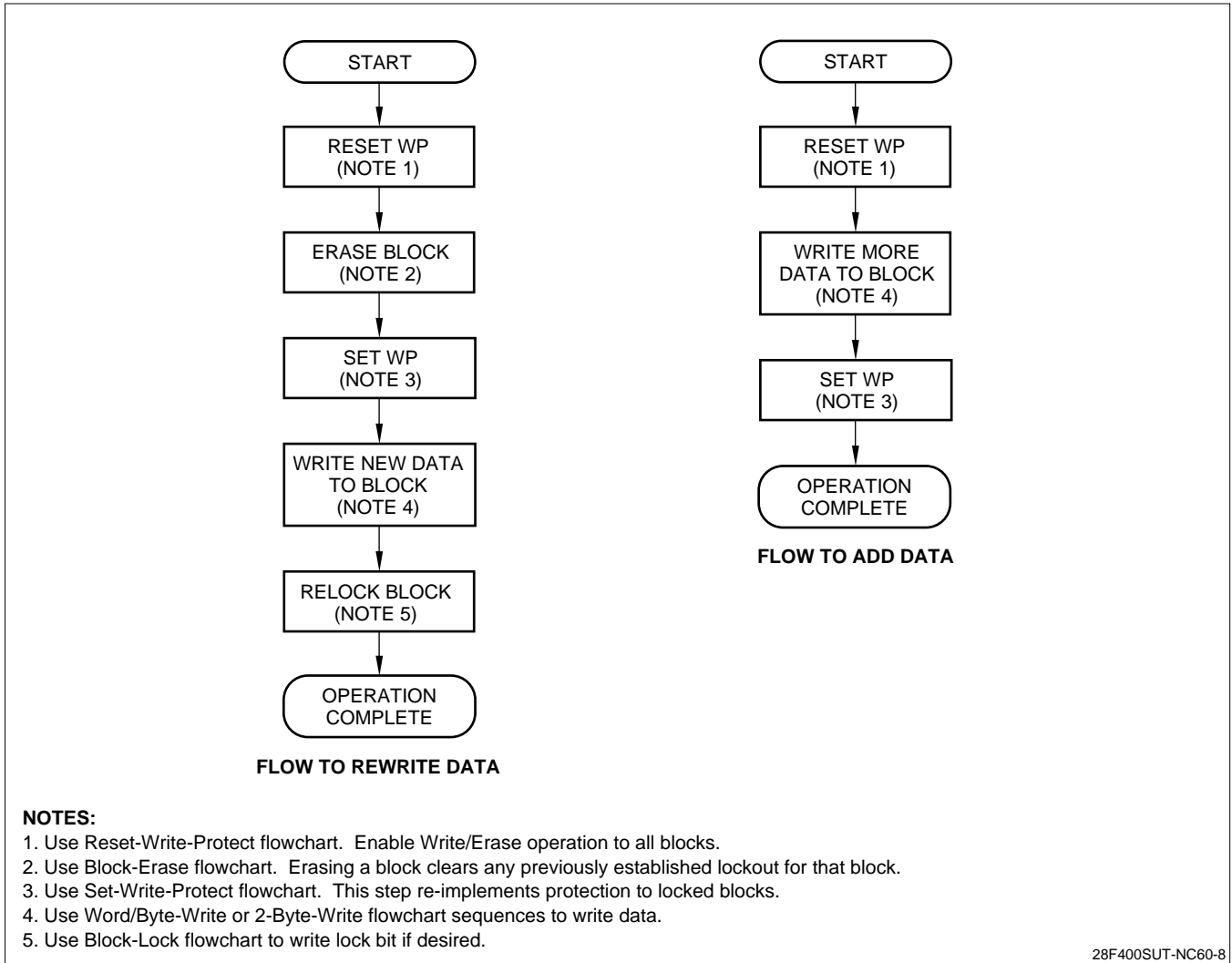


Figure 10. Updating Data in a Locked Block

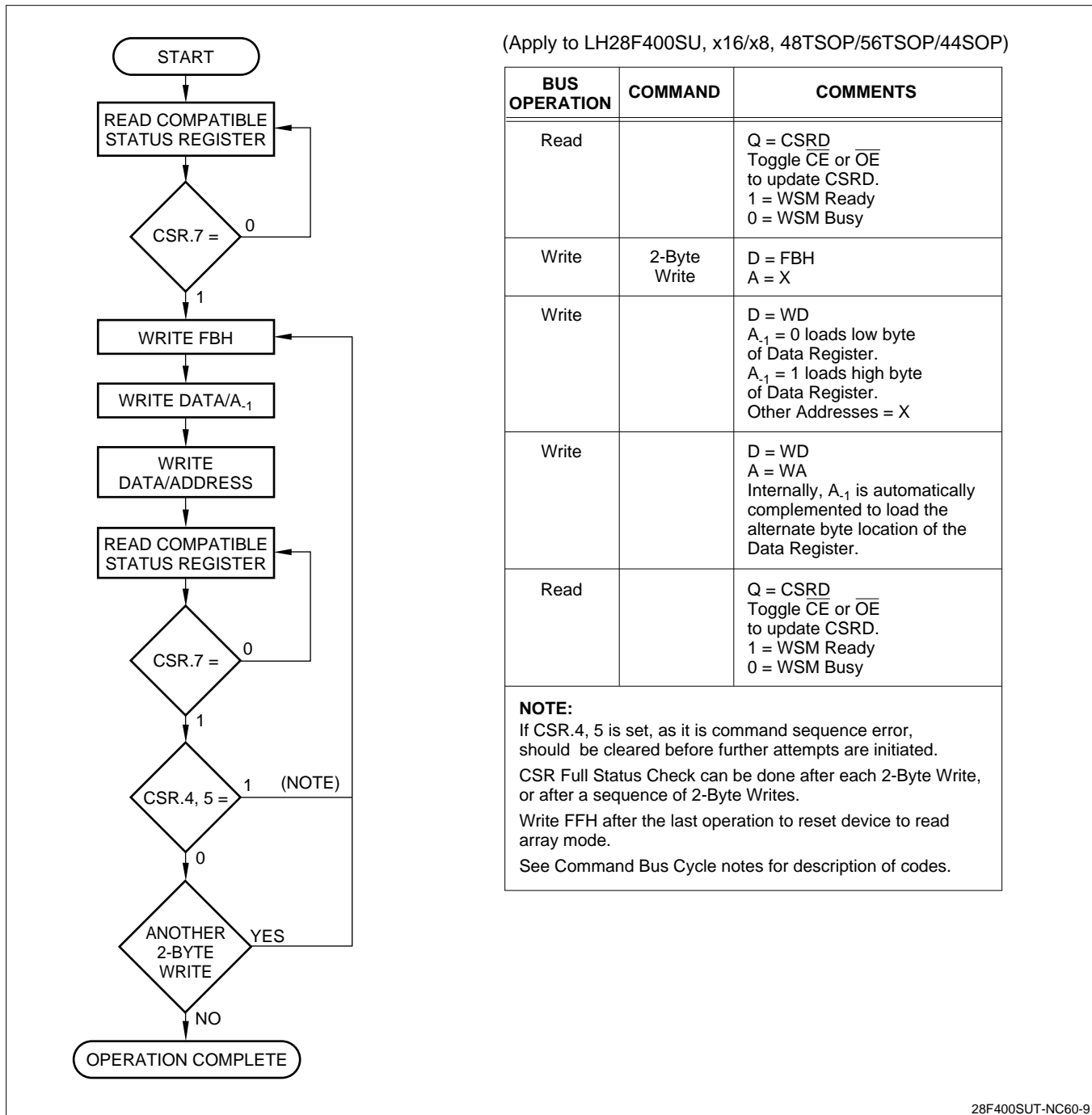
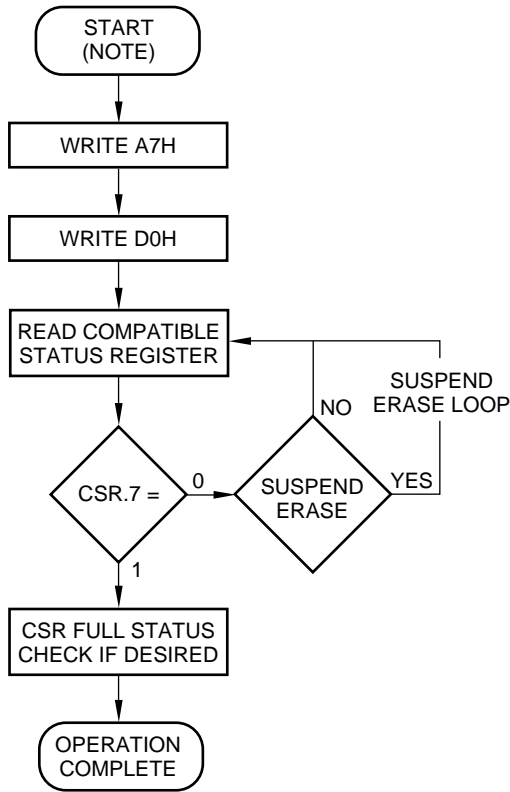


Figure 11. Two-Byte Serial Writes with Compatible Status Registers (LH28F400SU)



BUS OPERATION	COMMAND	COMMENTS
Write	Erase All Unlocked Blocks	D = A7H A = X
Write	Confirm	D = D0H A = X
Read		Q = CSRD Toggle CE or OE to update CSRD A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

CSR Full Status Check can be done after Erase All Unlocked Block, or after a sequence of Erasures.

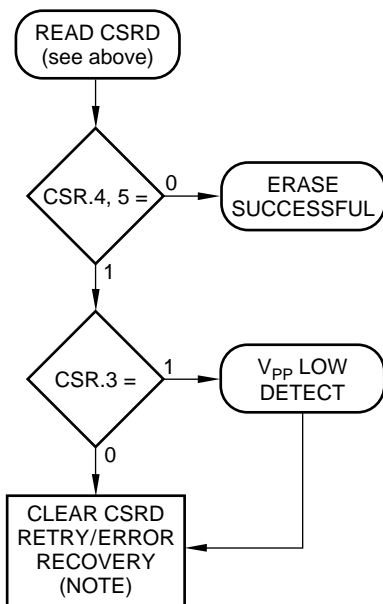
Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

NOTE:

- Where power off or \overline{RP} is set low during erase operation,
1. Clear CSR.3/4/5 and issue Reset WP command,
 2. Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence.
 3. Set WP command is issued, if necessary.

CSR FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check CSR.4, 5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V _{PP} Low Detect 0 = V _{PP} OK

CSR.3, 4, 5 should be cleared, if set, before further attempts are initiated.

NOTE:

- If CSR.3 (VPPS) is set to '1', after clearing CSR.3/4/5,
1. Issue Reset WP command,
 2. Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence.
 3. Set WP command is issued, if necessary.
- If CSR.3 (VPPS) is set to '0', after clearing CSR.3/4/5,
1. Retry Erase All Unlocked Block Erase command.

Figure 12. Erase All Unlocked Blocks with Compatible Status Registers

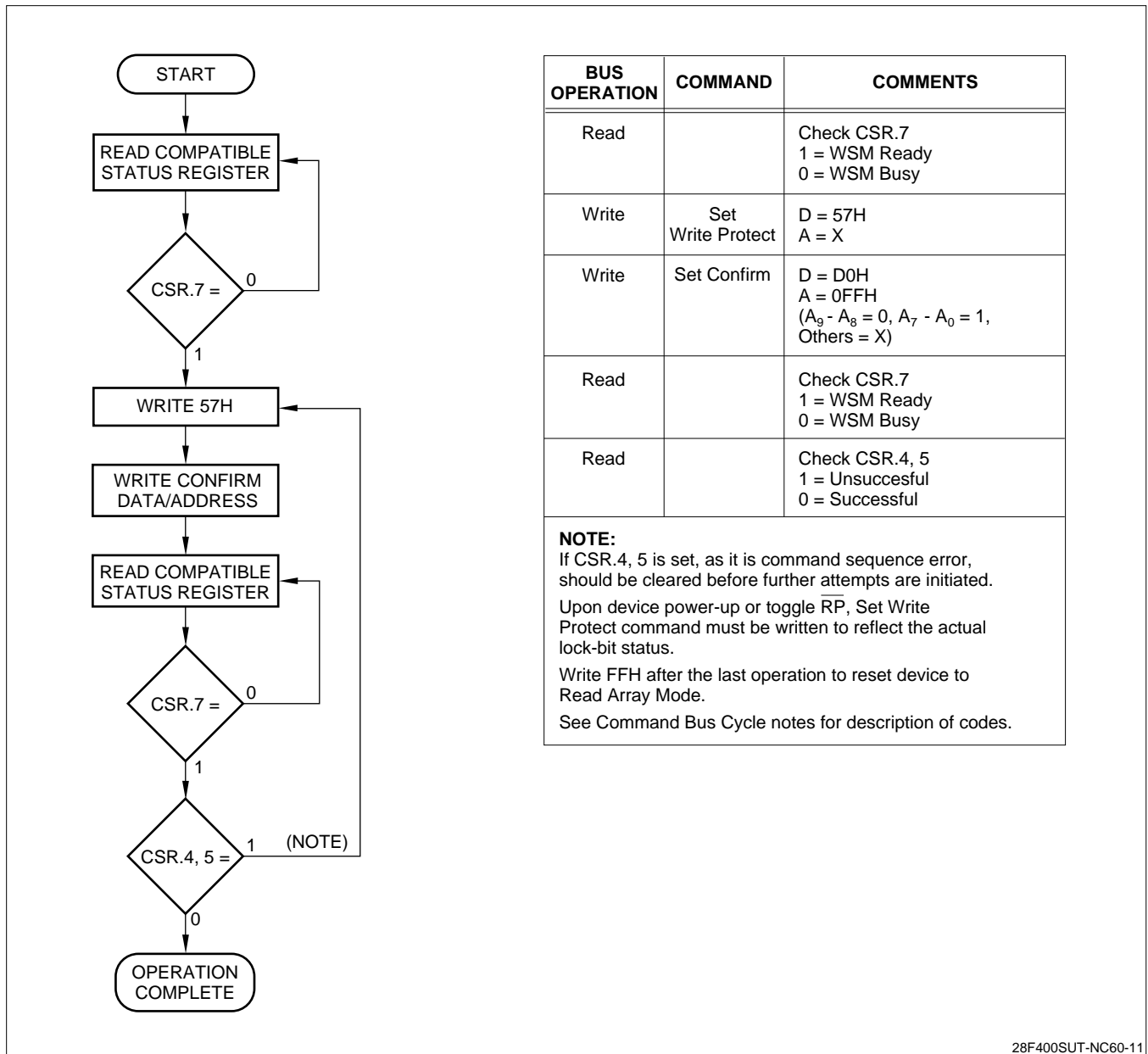


Figure 13. Set Write Protect

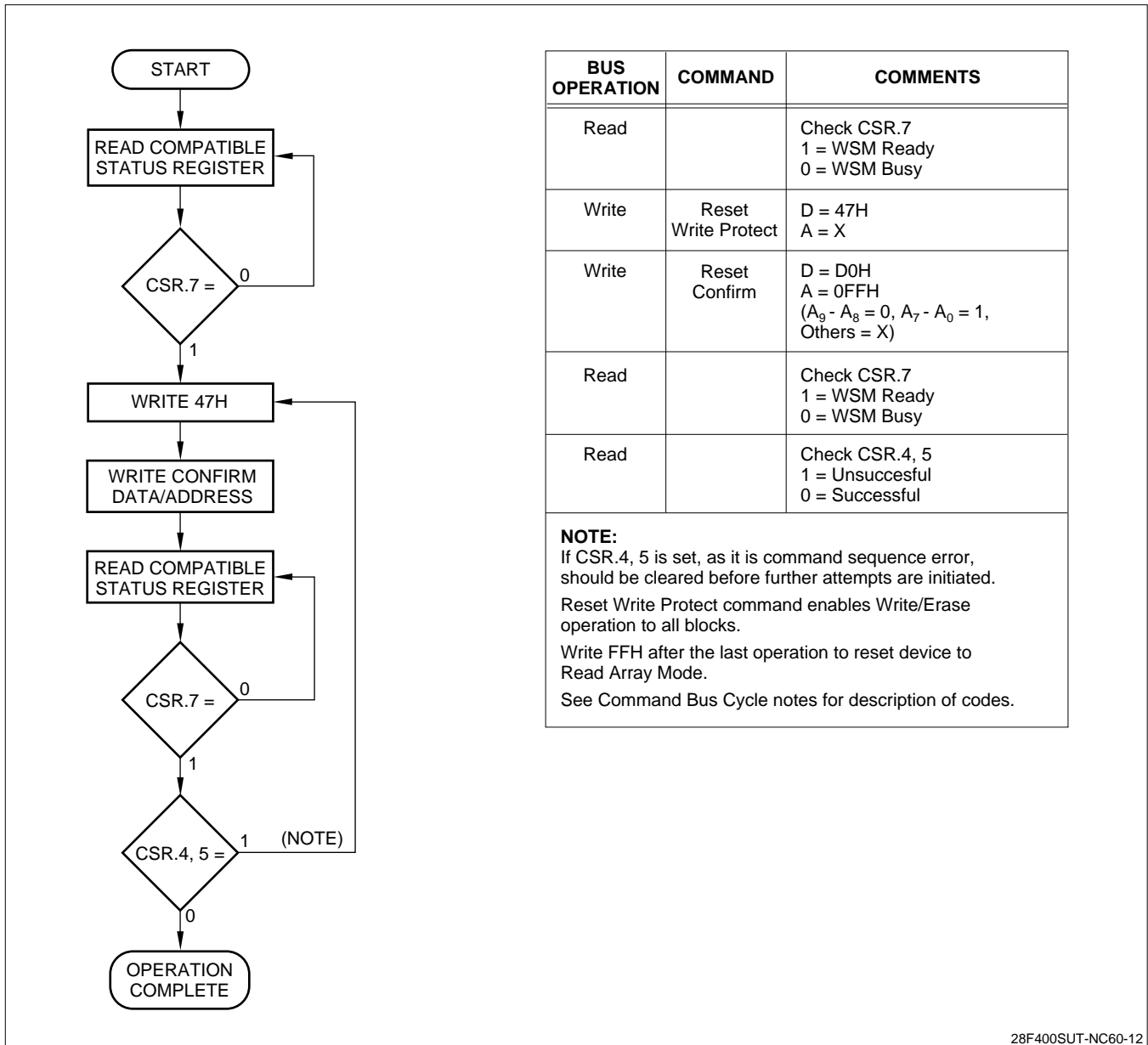


Figure 14. Reset Write Protect

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Temperature under bias 0°C to +80°C
 Storage temperature -65°C to +125°C

**WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.*

V_{CC} = 5.0 V ± 0.5 V Systems

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
T _A	Operating Temperature, Commercial	0	70.0	°C	Ambient Temperature	1
V _{CC}	V _{CC} with Respect to GND	-0.2	7.0	V		2
V _{PP}	V _{PP} Supply Voltage with Respect to GND	-0.2	7.0	V		2
V	Voltage on any Pin (Except V _{CC} , V _{PP}) with Respect to GND	-0.5	7.0	V		2
I	Current into any Non-Supply Pin		±30	mA		
I _{OUT}	Output Short Circuit Current		100.0	mA		3

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is -0.5 V on input/output pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Capacitance

For 5.0 V Systems

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTE
C _{IN}	Capacitance Looking into an Address/Control Pin	7	10	pF	T _A = 25°C, f = 1.0 MHz	1
	Capacitance Looking into an Address/Control Pin A ₁	9	12	pF	T _A = 25°C, f = 1.0 MHz	1
C _{OUT}	Capacitance Looking into an Output Pin	9	12	pF	T _A = 25°C, f = 1.0 MHz	1
C _{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications		100	pF	For V _{CC} = 5.0 V ±0.5 V	1
	Equivalent Testing Load Circuit V _{CC} ± 10%		2.5	ns	25 Ω transmission line delay	

NOTE:

1. Sampled, not 100% tested.

Timing Nomenclature

For 5.0 V systems use the standard JEDEC cross point definitions.

Each timing parameter consists of 5 characters. Some common examples are defined below:

- t_{CE} t_{ELQV} time (t) from \overline{CE} (E) going low (L) to the outputs (Q) becoming valid (V)
- t_{OE} t_{GLQV} time (t) from \overline{OE} (G) going low (L) to the outputs (Q) becoming valid (V)
- t_{ACC} t_{AVQV} time (t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
- t_{AS} t_{AVWH} time (t) from address (A) valid (V) to \overline{WE} (W) going high (H)
- t_{DH} t_{WHDx} time (t) from \overline{WE} (W) going high (H) to when the data (D) can become undefined (X)

	PIN CHARACTERS		PIN STATES
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	\overline{CE} (Chip Enable)	X	Driven, but not necessarily valid
G	\overline{OE} (Output Enable)	Z	High Impedance
W	\overline{WE} (Write Enable)		
P	\overline{RP} (Deep Power-Down Pin)		
R	$\overline{RY}/\overline{BY}$ (Ready/Busy)		
V	Any Voltage Level		
5 V	V_{CC} at 4.5 V Min.		

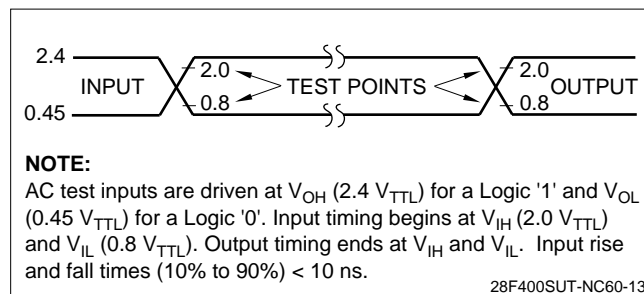


Figure 15. Transient Input/Output Reference Waveform ($V_{CC} = 5.0 V \pm 0.5 V$)

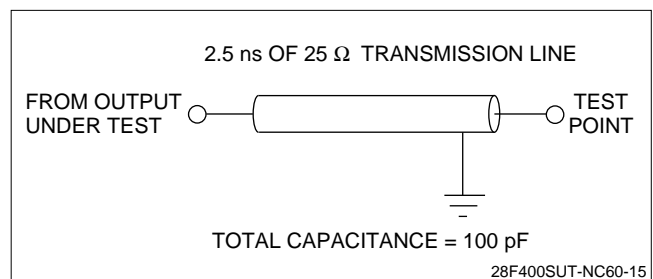


Figure 17. Transient Equivalent Testing Load Circuit ($V_{CC} = 5.0 V \pm 0.5 V$)

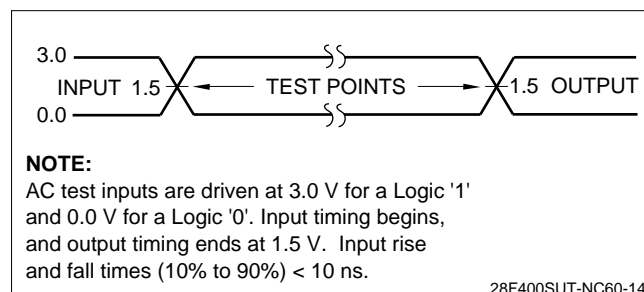


Figure 16. Transient Input/Output Reference Waveform ($V_{CC} = 5.0 V \pm .25 V$)

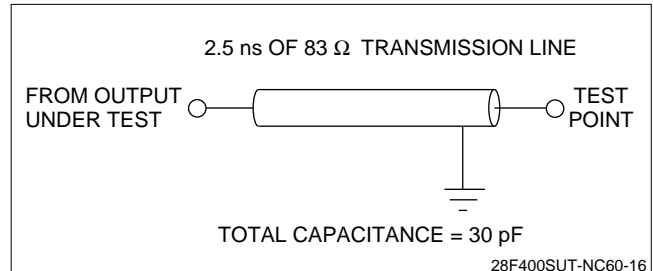


Figure 18. Transient Equivalent Testing Load Circuit ($V_{CC} = 5.0 V \pm .25 V$)

DC Characteristics

$$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}, T_A = 0^\circ\text{C to } +70^\circ\text{C}$$

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{IL}	Input Load Current			±1	μA	$V_{CC} = V_{CC\text{ MAX.}}, V_{IN} = V_{CC}$ or GND	1
I_{LO}	Output Leakage Current			±10	μA	$V_{CC} = V_{CC\text{ MAX.}}, V_{IN} = V_{CC}$ or GND	1
I_{CCS}	V_{CC} Standby Current	5		10	μA	$V_{CC} = V_{CC\text{ MAX.}},$ $\overline{CE}, \overline{RP} = V_{CC} \pm 0.2\text{ V}$ $\overline{BYTE} = V_{CC} \pm 0.2\text{ V}$ or GND ±0.2 V	1, 4
		1		4	mA	$V_{CC} = V_{CC\text{ MAX.}},$ $\overline{CE}, \overline{RP} = V_{IH}$ $\overline{BYTE} = V_{IH}$ or V_{IL}	
I_{CCD}	V_{CC} Deep Power-Down Current	0.2		5	μA	$\overline{RP} = \text{GND} \pm 0.2\text{ V}$	1
I_{CCR}^1	V_{CC} Read Current			60	mA	$V_{CC} = V_{CC\text{ MAX.}},$ CMOS: $\overline{CE} = \text{GND} \pm 0.2\text{ V}$ $\overline{BYTE} = \text{GND} \pm 0.2\text{ V}$ or $V_{CC} \pm 0.2\text{ V}$ Inputs = GND ±0.2 V or $V_{CC} \pm 0.2\text{ V}$ TTL: $\overline{CE} = V_{IL},$ $\overline{BYTE} = V_{IL}$ or V_{IH} Inputs = V_{IL} or V_{IH} $f = 10\text{ MHz}, I_{OUT} = 0\text{ mA}$	1, 3, 4
I_{CCR}^2	V_{CC} Read Current	16		30	mA	$V_{CC} = V_{CC\text{ MAX.}},$ CMOS: $\overline{CE} = \text{GND} \pm 0.2\text{ V}$ $\overline{BYTE} = V_{CC} \pm 0.2\text{ V}$ or GND ±0.2 V Inputs = GND ±0.2 V or $V_{CC} \pm 0.2\text{ V}$ TTL: $\overline{CE} = V_{IL},$ $\overline{BYTE} = V_{IH}$ or V_{IL} Inputs = V_{IL} or V_{IH} $f = 5\text{ MHz}, I_{OUT} = 0\text{ mA}$	1, 3, 4
I_{CCW}	V_{CC} Write Current	18		35	mA	Word/Byte Write in Progress	1
I_{CCE}	V_{CC} Block Erase Current	18		25	mA	Block Erase in Progress	1
I_{CCES}	V_{CC} Erase Suspend Current	5		10	mA	$\overline{CE} = V_{IH}$ Block Erase Suspended	1, 2
I_{PPS}	V_{PP} Standby Current	±1		±10	μA	$V_{PP} \leq V_{CC}$	1
I_{PPD}	V_{PP} Deep Power-Down Current	0.2		5	μA	$\overline{RP} = \text{GND} \pm 0.2\text{ V}$	1

DC Characteristics (Continued)

$$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}, T_A = 0^\circ\text{C to } +70^\circ\text{C}$$

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{PPR}	V_{PP} Read Current			200	μA	$V_{PP} > V_{CC}$	1
I_{PPW}	V_{PP} Write Current	15		35	mA	$V_{PP} = V_{PPH}$, Word/Byte Write in Progress	1
I_{PPE}	V_{PP} Erase Current	20		40	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress	1
I_{PPES}	V_{PP} Erase Suspend Current	65		200	μA	$V_{PP} = V_{PPH}$, Block Erase Suspended	1
V_{IL}	Input Low Voltage		-0.5	0.8	V		
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.5$	V		5
V_{OL}	Output Low Voltage			0.45	V	$V_{CC} = V_{CC}$ MIN. and $I_{OL} = 5.8 \text{ mA}$	
V_{OH}^1	Output High Voltage		$0.85 V_{CC}$		V	$I_{OH} = 2.5 \text{ mA}$ $V_{CC} = V_{CC}$ MIN.	
V_{OH}^2			$V_{CC} - 0.4$		V	$I_{OH} = 100 \mu\text{A}$ $V_{CC} = V_{CC}$ MIN.	
V_{PPL}	V_{PP} during Normal Operations		0.0	5.5	V		
V_{PPH}	V_{PP} during Write/Erase Operations	5.0	4.5	5.5	V		
V_{LKO}	V_{CC} Erase/Write Lock Voltage		1.4		V		

NOTES:

- All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0 \text{ V}$, $V_{PP} = 5.0 \text{ V}$, $T = 25^\circ\text{C}$. These currents are valid for all product versions (package and speeds).
- I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR} .
- Automatic Power Saving (APS) reduces I_{CCR} to less than 2 mA in Static operation.
- CMOS inputs are either $V_{CC} \pm 0.2 \text{ V}$ or $\text{GND} \pm 0.2 \text{ V}$. TTL Inputs are either V_{IL} or V_{IH} .
- Only to RP , V_{IH} (MIN.) = 2.4 V at VTTL-level input.

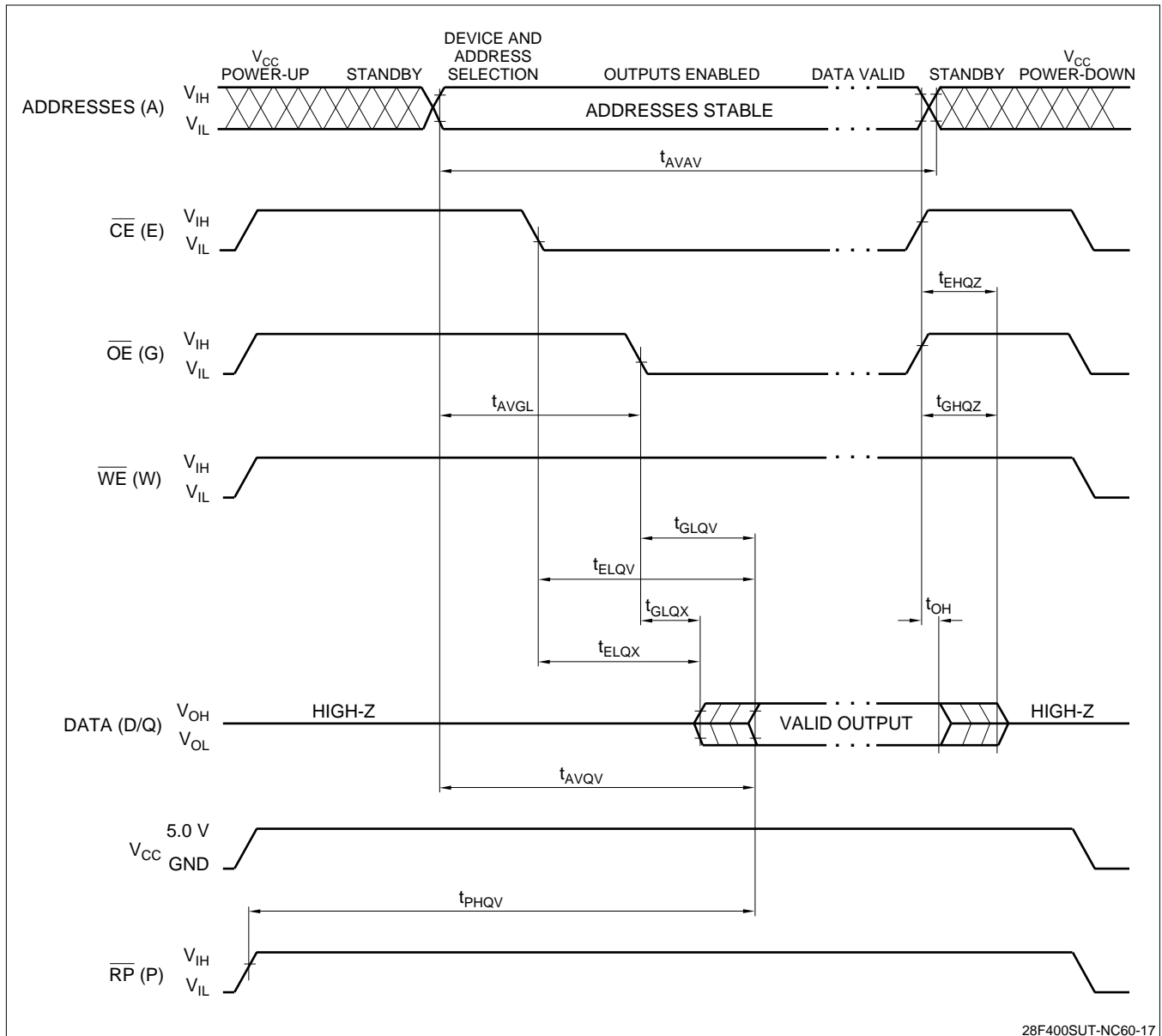
AC Characteristics - Read Only Operations¹

$$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}, T_A = 0^\circ\text{C to } +70^\circ\text{C}$$

SYMBOL	PARAMETER	$V_{CC} = 5.0 \text{ V} \pm 0.25 \text{ V}$		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		UNITS	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Read Cycle Time	60		70		ns	
t_{AVGL}	Address Setup to \overline{OE} Going Low	0		0		ns	3
t_{AVQV}	Address to Output Delay		60		70	ns	
t_{ELQV}	\overline{CE} to Output Delay		60		70	ns	2
t_{PHQV}	\overline{RP} High to Output Delay		400		430	ns	
t_{GLQV}	\overline{OE} to Output Delay		30		35	ns	2
t_{ELQX}	\overline{CE} to Output in Low Z	0		0		ns	3
t_{EHQZ}	\overline{CE} to Output in High Z		25		30	ns	3
t_{GLQX}	\overline{OE} to Output in Low Z	0		0		ns	3
t_{GHQZ}	\overline{OE} to Output in High Z		25		30	ns	3
t_{OH}	Output Hold from Address, \overline{CE} or \overline{OE} change, whichever occurs first	0		0		ns	3
t_{FLGZ}	\overline{BYTE} Low to Output in High Z		40		45	ns	3
t_{FLEL} t_{FHEL}	\overline{BYTE} High or Low to \overline{CE} Low	15		15		ns	3

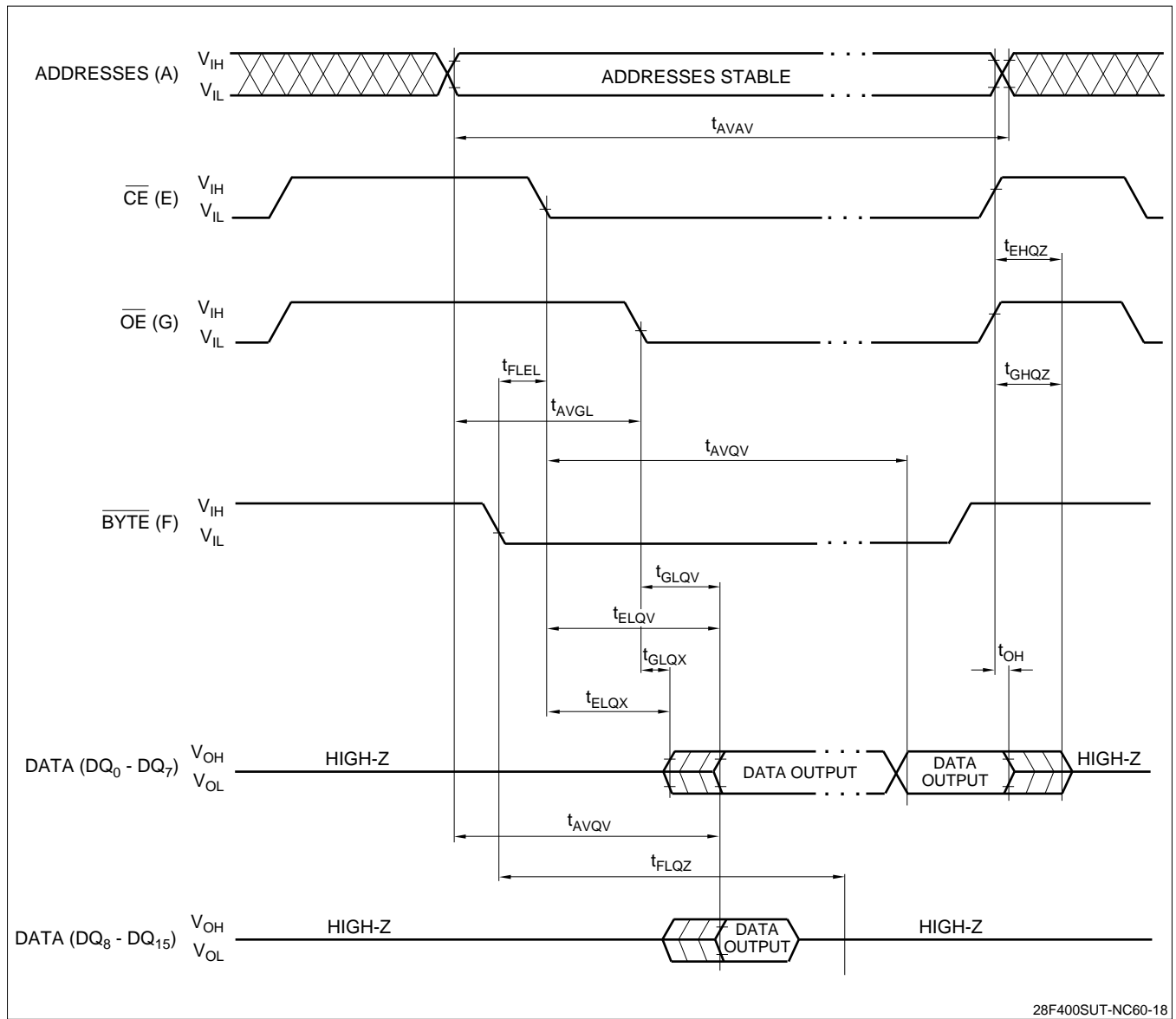
NOTES:

1. See AC Input/Output Reference Waveforms for timing measurements.
2. \overline{OE} may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of \overline{CE} without impact on t_{ELQV} .
3. Sampled, not 100% tested.
4. Only to \overline{RP} , $V_{IH}(\text{MIN.}) = 2.4 \text{ V}$.



28F400SUT-NC60-17

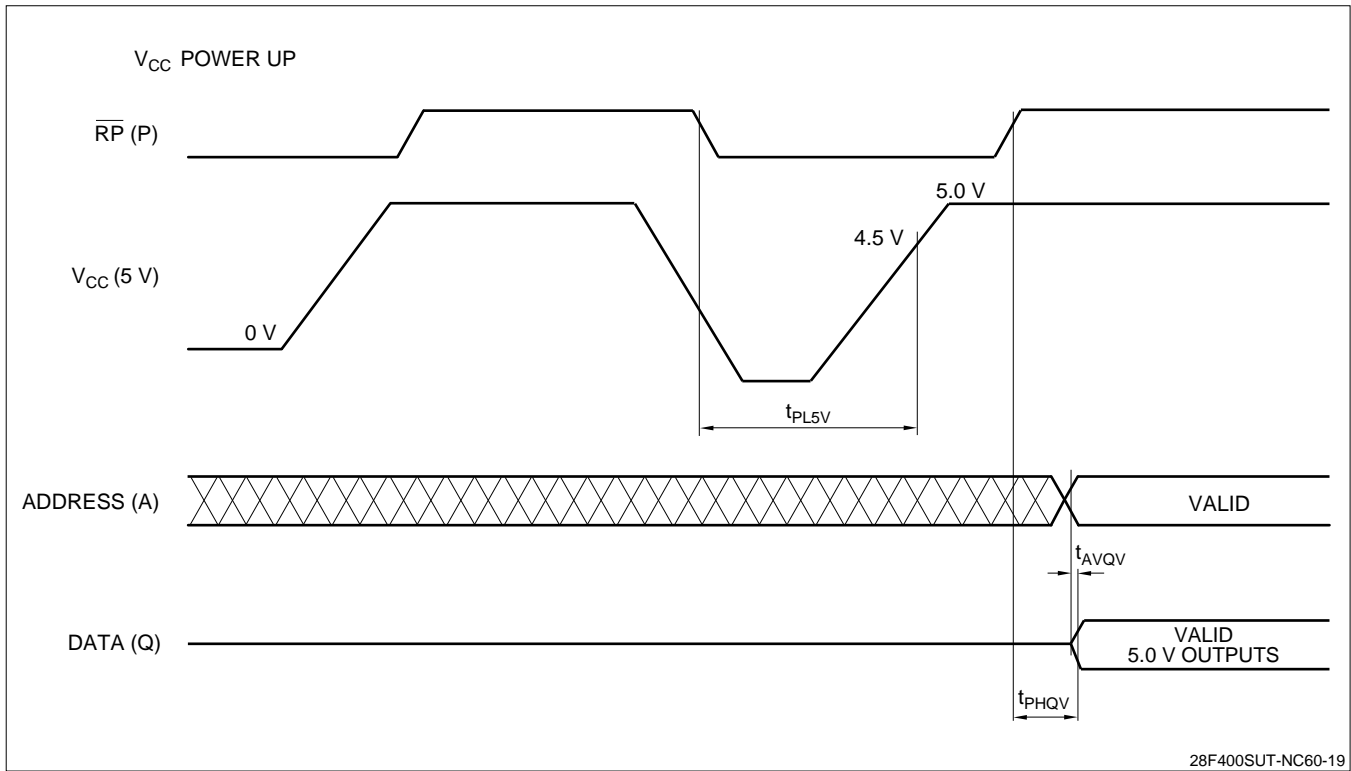
Figure 19. Read Timing Waveforms



28F400SUT-NC60-18

Figure 20. $\overline{\text{BYTE}}$ Timing Waveforms

POWER-UP AND RESET TIMINGS



28F400SUT-NC60-19

Figure 21. V_{CC} Power-Up and \overline{RP} Reset Waveforms

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{PL5V}	\overline{RP} Low to V_{CC} at 4.5 V MIN.	0		μ s	1
t_{AVQV}	Address Valid to Data Valid for $V_{CC} = 5\text{ V} \pm 10\%$		75	ns	2
t_{PHQV}	\overline{RP} High to Data Valid for $V_{CC} = 5\text{ V} \pm 10\%$		430	ns	2

NOTES:

\overline{CE} and \overline{OE} are switched low after Power-Up.

1. The power supply may start to switch concurrently with \overline{RP} going Low. \overline{RP} is required to stay low, until V_{CC} stays at recommended operating voltage.
2. The address access time and \overline{RP} high to data valid time are shown for 5.0 V V_{CC} operation. Refer to the AC Characteristics Read Only Operations also.

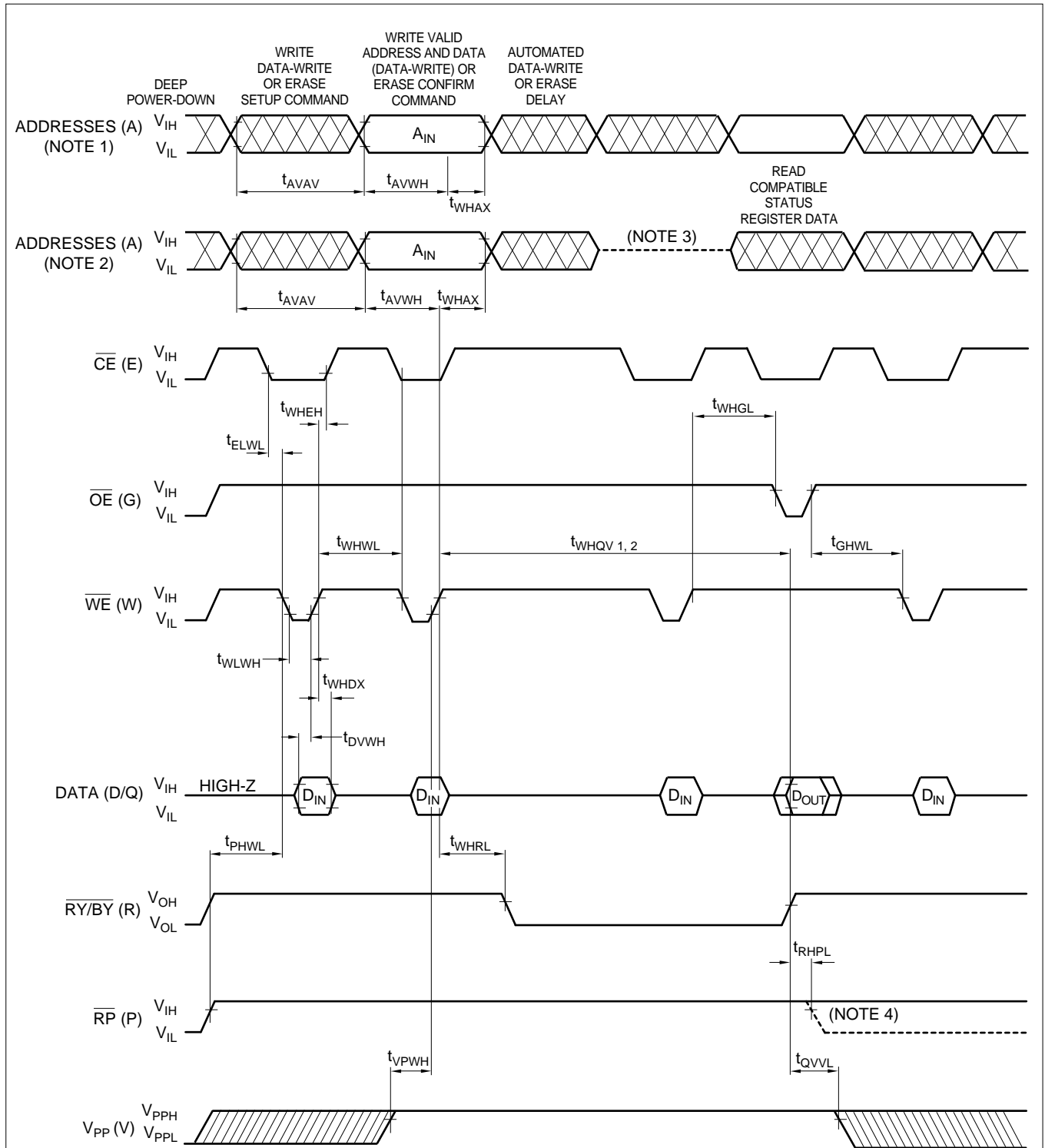
AC Characteristics for \overline{WE} - Controlled Command Write Operations¹

$$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}, T_A = 0^\circ\text{C to } +70^\circ\text{C}$$

SYMBOL	PARAMETER	TYP.	$V_{CC} = 5.0 \text{ V} \pm 0.25 \text{ V}$		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		UNITS	NOTE
			MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time		60		70		ns	
t_{VPWH}	V_{PP} Set up to \overline{WE} Going High		100		100		ns	3
t_{PHEL}	\overline{RP} Setup to \overline{CE} Going Low		400		430		ns	
t_{ELWL}	\overline{CE} Setup to \overline{WE} Going Low		0		0		ns	
t_{AVWH}	Address Setup to \overline{WE} Going High		55		60		ns	2, 6
t_{DVWH}	Data Setup to \overline{WE} Going High		55		60		ns	2, 6
t_{WLWH}	\overline{WE} Pulse Width		55		60		ns	
t_{WHDX}	Data Hold from \overline{WE} High		0		0		ns	2
t_{WHAX}	Address Hold from \overline{WE} High		10		10		ns	2
t_{WHEH}	\overline{CE} Hold from \overline{WE} High		10		10		ns	
t_{WHWL}	\overline{WE} Pulse Width High		30		30		ns	
t_{GHWL}	Read Recovery before Write		0		0		ns	
t_{WHRL}	\overline{WE} High to $\overline{RY}/\overline{BY}$ Going Low			100		100	ns	
t_{RHPL}	\overline{RP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		0		ns	3
t_{PHWL}	\overline{RP} High Recovery to \overline{WE} Going Low		1		1		μs	
t_{WHGL}	Write Recovery before Read		60		65		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		0		μs	
t_{WHQV}^1	Duration of Byte Write Operation	13	4.5		4.5		μs	4, 5
t_{WHQV}^2	Duration of Block Erase Operation		0.3		0.3		s	4

NOTES:

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of \overline{WE} for all Command Write operations.



NOTES:

1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
4. \overline{RP} low transition is only to show t_{RHPL} ; not valid for above Read and Write cycles.

Figure 22. AC Waveforms for Command Write Operations

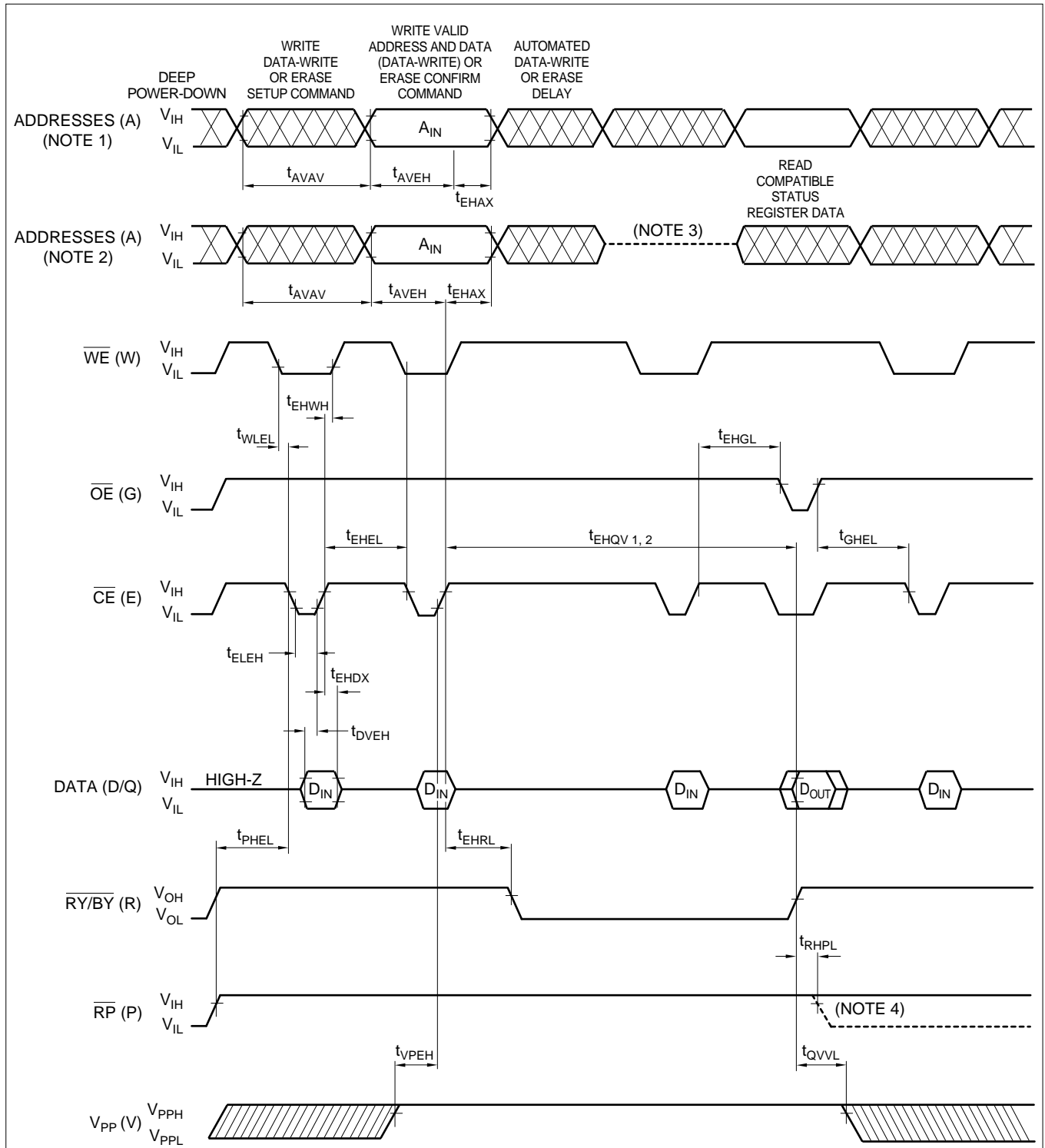
AC Characteristics for \overline{CE} - Controlled Command Write Operations¹

$$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}, T_A = 0^\circ\text{C to } +70^\circ\text{C}$$

SYMBOL	PARAMETER	TYP.	$V_{CC} = 5.0 \text{ V} \pm 0.25 \text{ V}$		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		UNITS	NOTE
			MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time		60		70		ns	
t_{PHWL}	\overline{RP} Setup to \overline{WE} Going Low		400		430		ns	3
t_{VPEH}	V_{PP} Set up to \overline{CE} Going High		100		100		ns	3
t_{WLEL}	\overline{WE} Setup to \overline{CE} Going Low		0		0		ns	
t_{AVEH}	Address Setup to \overline{CE} Going High		55		60		ns	2, 6
t_{DVEH}	Data Setup to \overline{CE} Going High		55		60		ns	2, 6
t_{ELEH}	\overline{CE} Pulse Width		55		60		ns	
t_{EHDX}	Data Hold from \overline{CE} High		0		0		ns	2
t_{EHAX}	Address Hold from \overline{CE} High		10		10		ns	2
t_{EHWH}	\overline{WE} Hold from \overline{CE} High		10		10		ns	
t_{EHEL}	\overline{CE} Pulse Width High		30		30		ns	
t_{GHLE}	Read Recovery before Write		0		0		ns	
t_{EHRL}	\overline{CE} High to $\overline{RY}/\overline{BY}$ Going Low			100		100	ns	
t_{RHPL}	\overline{RP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		0		ns	3
t_{PHEL}	\overline{RP} High Recovery to \overline{CE} Going Low		1		1		μs	
t_{EHGL}	Write Recovery before Read		60		65		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		0		μs	
t_{EHQV1}	Duration of Byte Write Operation	13	4.5		4.5		μs	4, 5
t_{EHQV2}	Duration of Block Erase Operation		0.3		0.3		s	4

NOTES:

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Byte Write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of \overline{CE} for all Command Write operations.



NOTES:

1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
4. RP low transition is only to show t_{RHPL} ; not valid for above Read and Write cycles.

Figure 23. Alternate AC Waveforms for Command Write Operations

Erase and Byte Write Performance

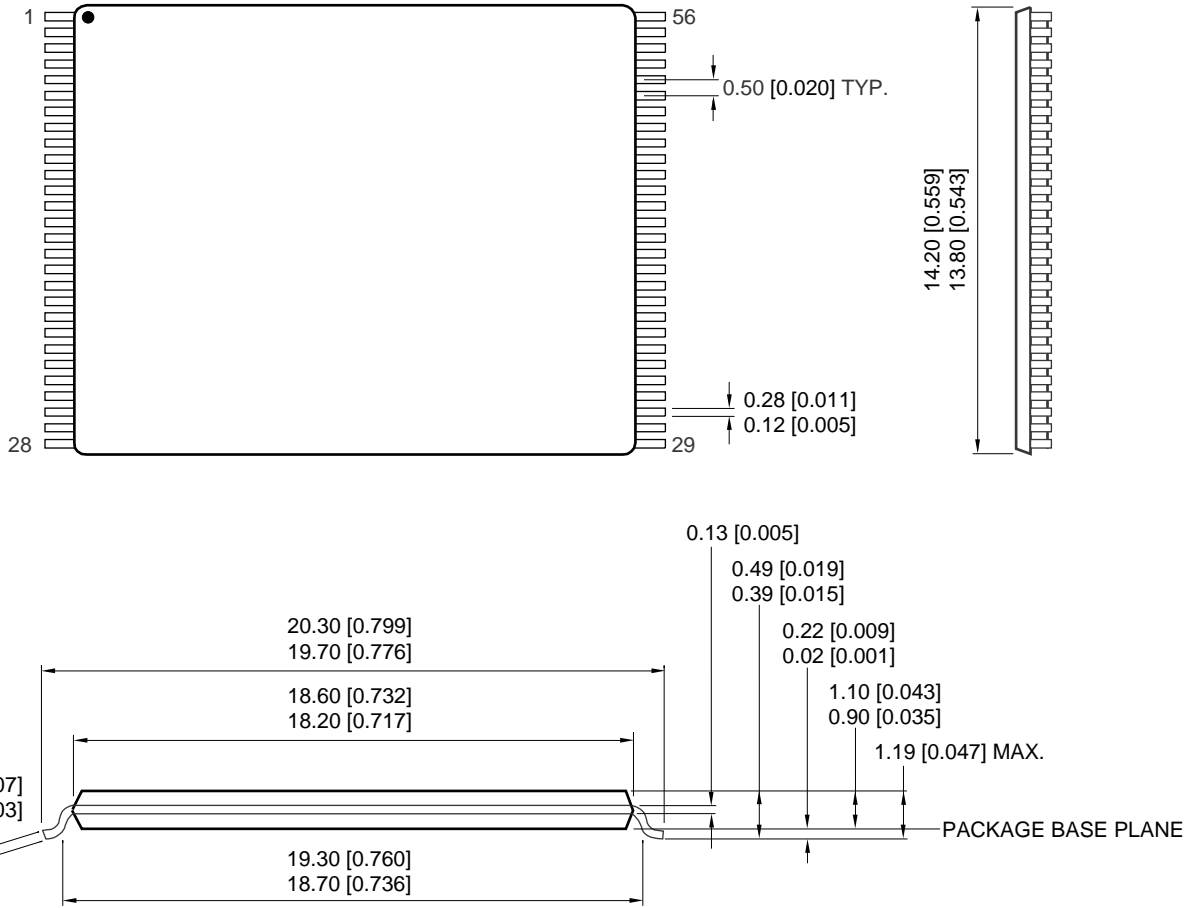
$$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}, T_A = 0^\circ\text{C to } +70^\circ\text{C}$$

SYMBOL	PARAMETER	TYP. ⁽¹⁾	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
t _{WHRH} ¹	Byte Write Time	13			μs		2
t _{WHRH} ²	Two-Byte Serial Write Time	20			μs		2, 3
t _{WHRH} ³	Word Write Time	20			μs		2, 4
t _{WHRH} ⁴	16KB Block Write Time	0.22		1.0	s	Byte Write Mode	2
t _{WHRH} ⁵	16KB Block Write Time	0.17		1.0	s	Two-Byte Serial Write Mode	2, 3
t _{WHRH} ⁵	16KB Block Write Time	0.17		1.0	s	Word Write Mode	2, 4
	Block Erase Time (16KB)	0.6		10	s		2
	Full Chip Erase Time	8.8 - 14.4			s		2, 5

NOTES:

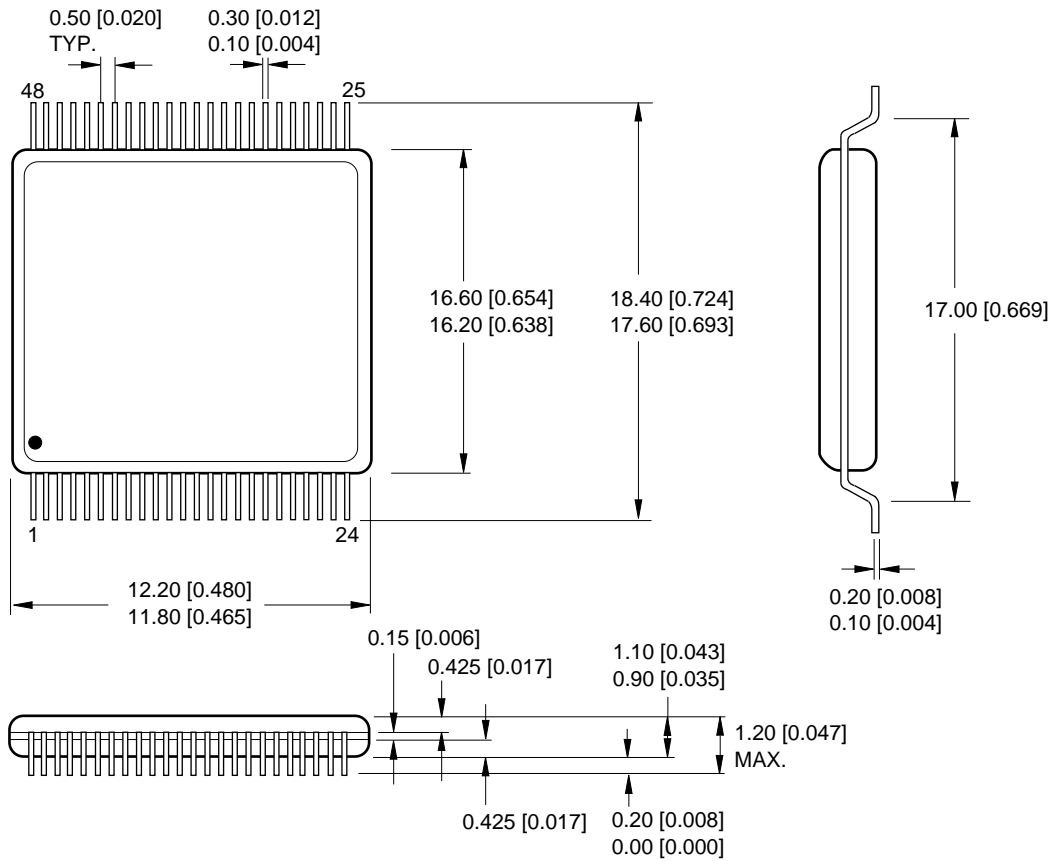
1. 25°C, V_{PP} = 5.0 V Sampled.
2. Excludes System-Level Overhead.
3. Two-Byte Serial Write mode is valid at x8-bit configuration only.
4. Word Write mode is valid at x16-bit configuration only.
5. Depends on the number of protected blocks.

56TSOP (TSOP056-P-1420)



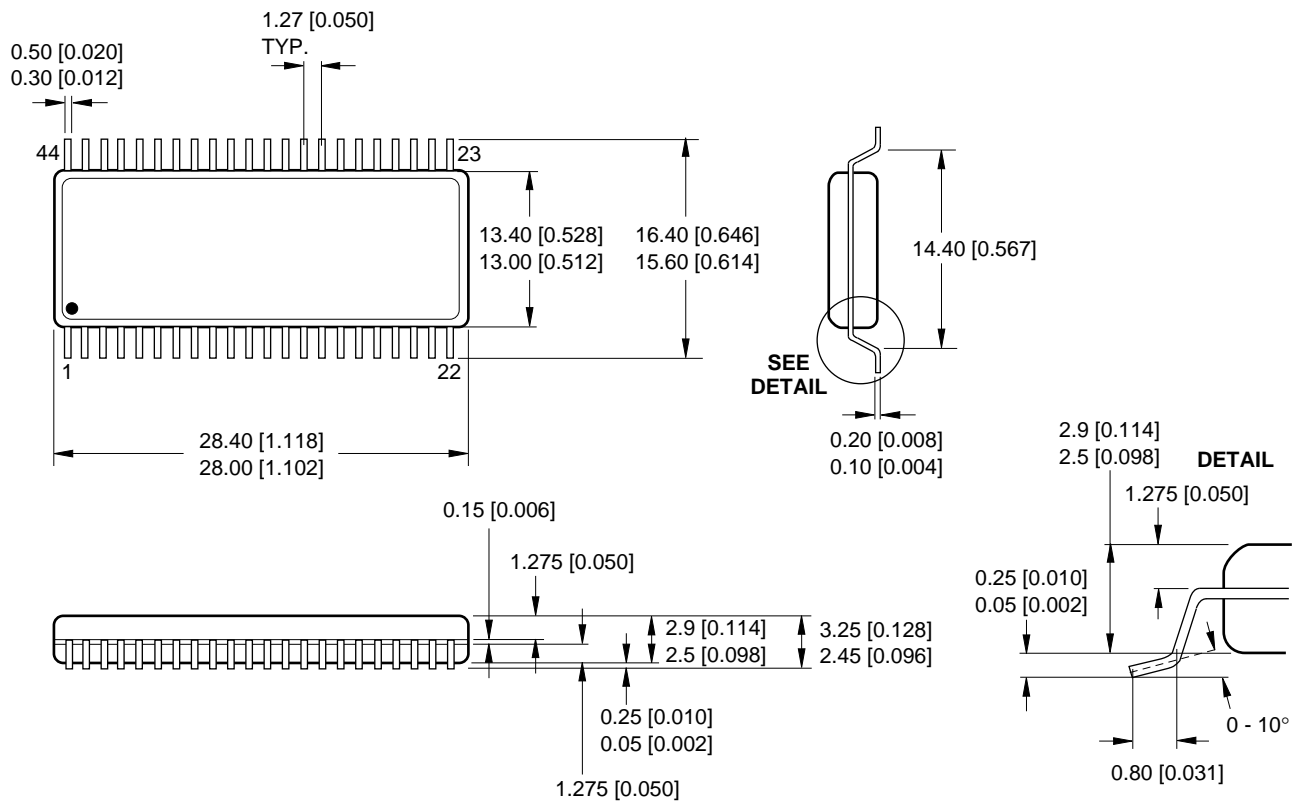
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

48TSOP (TSOP048-P-1218)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

44SOP (SOP044-P-0600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

44SOP

ORDERING INFORMATION

LH28F400SU	X	-NC##	
Device Type	Package	Speed	
			{ 60 (V _{CC} = 5.0 V ± 0.25 V) 80 (V _{CC} = 5.0 V ± 0.50 V) Access Time (ns)
			{ T 56-pin, 1.2 mm x 14 mm x 20 mm TSOP (Type I) (TSOP056-P-1420) E 48-pin, 1.2 mm x 12 mm x 18 mm TSOP (Type I) (TSOP048-P-1218) N 44-pin, 600-mil SOP (SOP044-P-0600)
		4M (512K x 8, 256K x 16) Flash Memory	

Example: LH28F400SUT-NC60 (4M (512K x 8, 256K x 16) Flash Memory, 60 ns, 56-pin TSOP)

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SHARP[®]**NORTH AMERICA**

SHARP Electronics Corporation
Microelectronics Group
5700 NW Pacific Rim Blvd., M/S 20
Camas, WA 98607, U.S.A.
Phone: (360) 834-2500
Telex: 49608472 (SHARPCAM)
Facsimile: (360) 834-8903
<http://www.sharpmeg.com>

EUROPE

SHARP Electronics (Europe) GmbH
Microelectronics Division
SonninstraÙe 3
20097 Hamburg, Germany
Phone: (49) 40 2376-2286
Telex: 2161867 (HEEG D)
Facsimile: (49) 40 2376-2232

ASIA

SHARP Corporation
Integrated Circuits Group
2613-1 Ichinomoto-Cho
Tenri-City, Nara, 632, Japan
Phone: (07436) 5-1321
Telex: LABOMETA-B J63428
Facsimile: (07436) 5-1532